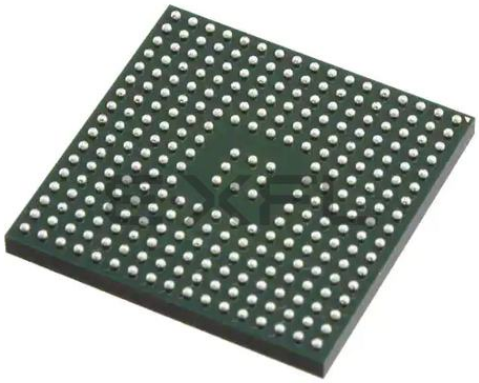


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	272-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9307-ir

OVERVIEW

The EP9307 is an ARM920T-based system-on-a-chip (SOC) design with a large peripheral set targeted to a variety of applications:

- Thin client computers for business and home
- Internet radio
- Internet access devices
- Industrial computers
- Specialized terminals
- Point of sale terminals
- Test and measurement equipment

The ARM920T microprocessor core with separate 16-kbyte, 64-way set-associative instruction and data caches is augmented by the MaverickCrunch™ co-processor, enabling high-speed floating point calculations.

MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100 Mbps Ethernet media access controller (MAC) is included along with external interfaces to SPI, I^2S audio, Raster/LCD, keypad and touchscreen. A three-port USB 2.0 Full-speed Host (OHCI) (12 Mbits per second) and three UARTs are included as well.

The EP9307 is a high-performance, low-power, RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 200 MHz (184 MHz for industrial conditions). The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 750 mW (dependent on speed).

Table A. Change History

Revision	Date	Changes
PP1	July 2004	Initial Release.
PP2	August 2004	Correct error in pin out table, pages 42 & 43.
PP3	August 2004	Minor correction.
PP4	March 2005	Update electrical characteristics with most-current characterization data.
F1	February 2010	Removed “Preliminary Data” statement from legal disclaimer. Removed lead-containing device part numbers. Increased minimum CVDD & VDD_PLL voltages from 1.65 V min. to 1.71 V min. Changed operating temperatures to 0 to 60°C commercial, -40 to 70°C industrial.
F2	March 2010	Increased commercial/industrial temperatures to 70/85 deg. C max.

Processor Core - ARM920T

The ARM920T is a Harvard architecture processor with separate 16 kbyte instruction and data caches with an 8-word line length but a unified memory. The processor utilizes a five-stage pipeline consisting of fetch, decode, execute, memory and write stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16 kbyte Instruction Cache with lockdown
- 16 kbyte Data Cache (programmable write-through or write-back) with lockdown
- MMU for Linux®, Microsoft® Windows® CE and other operating systems
- Translation Look Aside Buffers with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 1 Mbyte, 64 kbyte, 4 kbyte, and 1 kbyte
- Independent lockdown of TLB Entries

MaverickCrunch™ Math Engine

The MaverickCrunch Engine is a mixed-mode coprocessor designed primarily to accelerate the math processing required to rapidly encode digital audio formats. It accelerates single- and double-precision integer and floating point operations plus an integer multiply-accumulate (MAC) instruction that is considerably faster than the ARM920T's native MAC instruction. The ARM920T coprocessor interface is utilized thereby sharing its memory interface and instruction stream. Hardware forwarding and interlock allows the ARM to handle looping and addressing while MaverickCrunch handles computation. Features include:

- IEEE-754 single and double precision floating point
- 32/64-bit integer
- Add/multiply/compare
- Integer MAC 32-bit input with 72-bit accumulate
- Integer Shifts
- Floating point to/from integer conversion
- Sixteen 64-bit register files
- Four 72-bit accumulators

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID are programmed into the EP9307 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP9307 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

General Purpose Memory Interface (SDRAM, SRAM, ROM, FLASH)

The EP9307 features a unified memory address model where all memory devices are accessed over a common address/data bus. A separate internal port is dedicated to the read-only Raster/LCD refresh engine, while the rest of the memory accesses are performed via the Processor bus. The SRAM memory controller supports 8, 16 and 32-bit devices and accommodates an internal boot ROM concurrently with 32-bit SDRAM memory.

- 1 to 4 banks of 32-bit, 100 MHz SDRAM
- One internal port dedicated to the Raster/LCD Refresh Engine (Read Only)
- Address and data bus shared between SDRAM, SRAM, ROM, and FLASH memory
- NOR FLASH memory supported

Table B. General Purpose Memory Interface Pin Assignments

Pin Mnemonic	Pin Description
SDCLK	SDRAM Clock
SDCLKEN	SDRAM Clock Enable
SDCSn[3:0]	SDRAM Chip Selects 3-0
RASn	SDRAM RAS
CASn	SDRAM CAS
SDWEn	SDRAM Write Enable
CSn[7:6] and CSn[3:0]	Chip Selects 7, 6, 3, 2, 1, 0
AD[25:0]	Address Bus 25-0
DA[31:0]	Data Bus 31-0
DQMn[3:0]	SDRAM Output Enables / Data Masks
WRn	SRAM Write Strobe
RDn	SRAM Read/OE Strobe
WAITn	SRAM Wait Input

Universal Asynchronous Receiver/Transmitters (UARTs)

Three 16550-compatible UARTs are supplied. Two provide asynchronous HDLC (High-level Data Link Control) protocol support for full duplex transmit and receive. The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency, and optionally passes the CRC to the host at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency. The host must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams. A third IrDA® compatible UART is also supplied.

- UART1 supports modem bit rates up to 115.2 kbps, supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.
- UART3 supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx and Tx.

Table H. Universal Asynchronous Receiver / Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTSn	UART1 Clear To Send / Transmit Enable
DSRn/DCDn	UART1 Data Set Ready / Data Carrier Detect
DTRn	UART1 Data Terminal Ready
RTSn	UART1 Ready To Send
EGPIO[0]/RI	UART1 Ring Indicator
TXD1/SIROUT	UART2 Transmit / IrDA Output
RXD1/SIRIN	UART2 Receive / IrDA Input
TXD2	UART3 Transmit
RXD2	UART3 Receive
TENn	HDLC3 Transmit Enable

Internal Boot ROM

The Internal 16-kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP9307 User's Guide for operational details.

Triple-port USB Host

The USB Open Host Controller Interface (Open HCI) provides full-speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB "tiered-star" topology.

This includes the following features:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB device connections
- Root HUB integrated with 3 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table I. Triple Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2:0]	USB Positive signals
USBm[2:0]	USB Negative Signals

Two-wire Interface Support

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table J. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Real-Time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ±1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9307 device will not boot.

Table K. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Table L. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer ensures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free running down-counters or as periodic timers for fixed interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 µs to 73.3 hours.

One 40-bit debug timer, plus a 6-bit prescale counter, has a range of 1.0 µs to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 62 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active high or active low level sensitive inputs. GPIO pins programmed as interrupts may be programmed as active high level sensitive, active low level sensitive, rising edge triggered, falling edge triggered, or combined rising/falling edge triggered.

- Supports 64 interrupts from a variety of sources (such as UARTs, GPIO, and key matrix)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Three dedicated off-chip interrupt lines operate as active high level sensitive interrupts
- Any of the 16 GPIO lines maybe configured to generate interrupts
- Software supported priority mask for all FIQs and IRQs

Table M. External Interrupt Controller Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[2:0]	External Interrupts 2, 1, 0

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table N. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 14 EGPIO pins may each be configured individually as an output, an input, or an interrupt input.

There are 22 pins that may alternatively be used as input, output, or open-drain pins, but do not support interrupts. These pins are:

- Key Matrix ROW[7:0], COL[7:0]
- Ethernet MDIO
- Both LED Outputs
- Two-wire Clock and Data
- GGPIO[2]
- HGPIO[7:2]

6 pins may alternatively be used as inputs only:

- CTSn, DSRn/DCDn
- 4 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTSn
- ARSTn

Table O. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15] EGPIO[13:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[7] FGPIO[5] FGPIO[0]	Expanded General Purpose Input / Output Pins with Interrupts

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 200 MHz (184 MHz for industrial conditions).

Table P. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table Q. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-Channel DMA Controller

The DMA module contains 12 separate DMA channels. These may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated due to AC and/or DC output loading.
2. The power supply pins are at maximum values listed in "Recommended Operating Conditions", below.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	3.0 1.71 1.71 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	200	MHz
Processor Clock Speed - Industrial	FCLK	-	-	184	MHz
System Clock Speed - Commercial	HCLK	-	-	100	MHz
System Clock Speed - Industrial	HCLK	-	-	92	MHz

DC Characteristics

(T_A = 0 to 70° C; CVDD = VDD_PLL = 1.8; RVDD = 3.3 V;
All grounds = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Max	Unit
High level output voltage	Iout = -4 mA	(Note 3)	V_{oh}	0.85 × RVDD	-	V
Low level output voltage	Iout = 4 mA		V_{ol}	-	0.15 × RVDD	V
High level input voltage		(Note 4)	V_{ih}	0.65 × RVDD	VDD + 0.3	V
Low level input voltage		(Note 4)	V_{il}	–0.3	0.35 × RVDD	V
High level leakage current	Vin = 3.3 V	(Note 4)	I_{ih}	-	10	µA
Low level leakage current	Vin = 0	(Note 4)	I_{il}	-	-10	µA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded)					
Power Supply Current:	CVDD/VDD_PLL Total RVDD	- -	190 45	240 80	mA mA
Low-Power Mode Supply Current	CVDD/VDD_PLL Total RVDD	- -	2 1.0	3.5 2	mA mA

Note: 3. For open drain pins, high level output voltage is dependent on the external load.
4. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation (See Table S on page 46). If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

SDRAM Burst Read Cycle

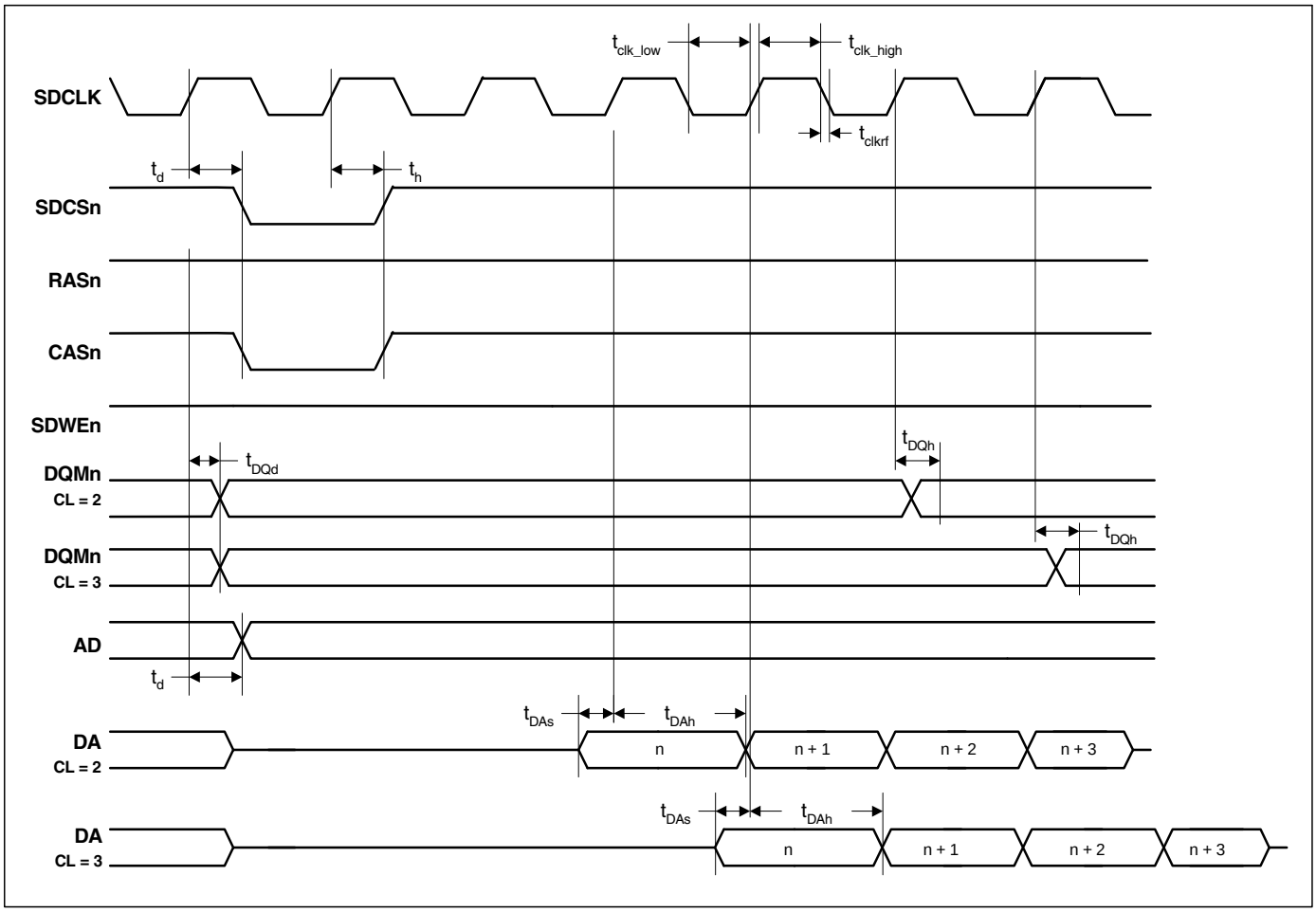


Figure 3. SDRAM Burst Read Cycle Timing Measurement

SDRAM Burst Write Cycle

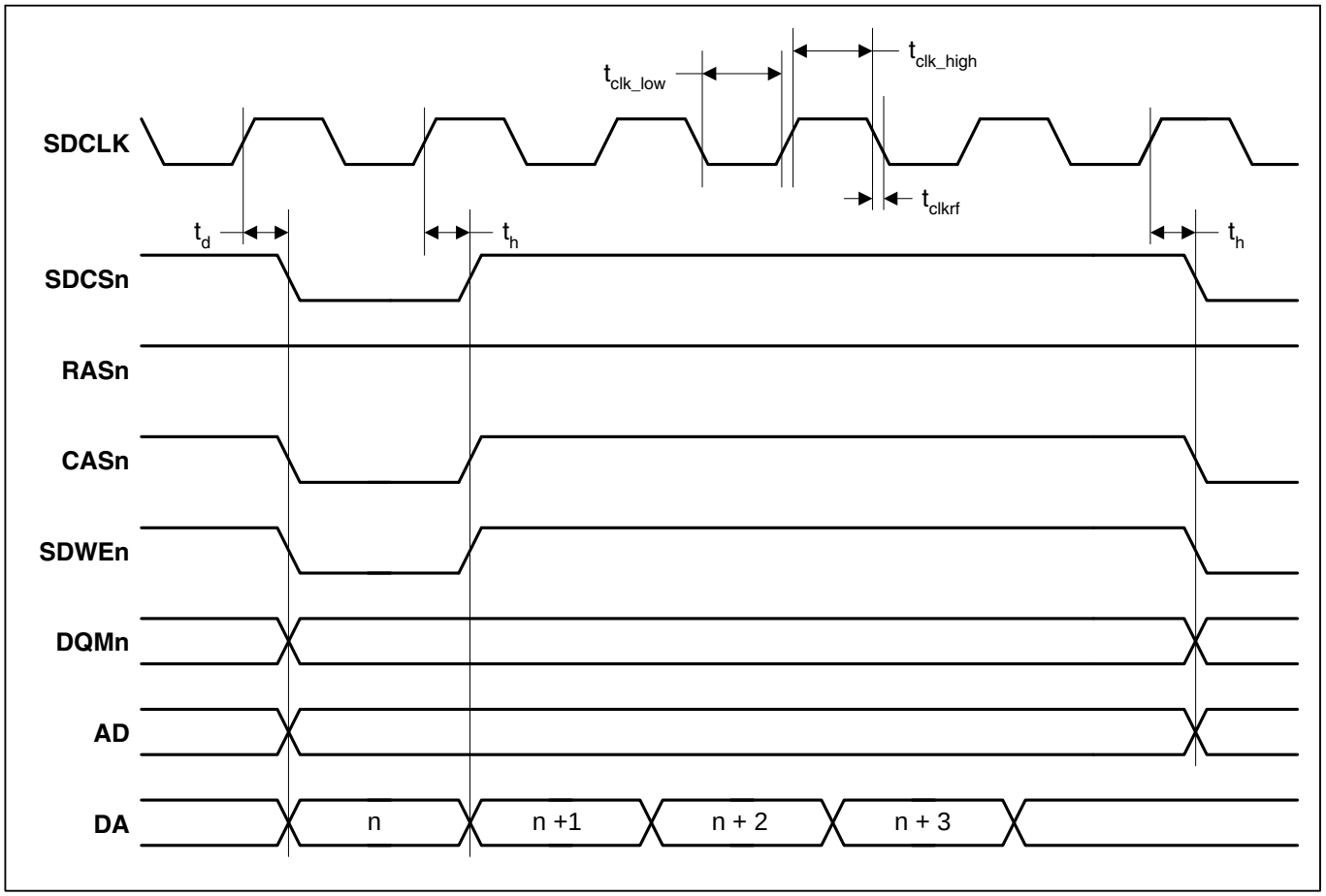
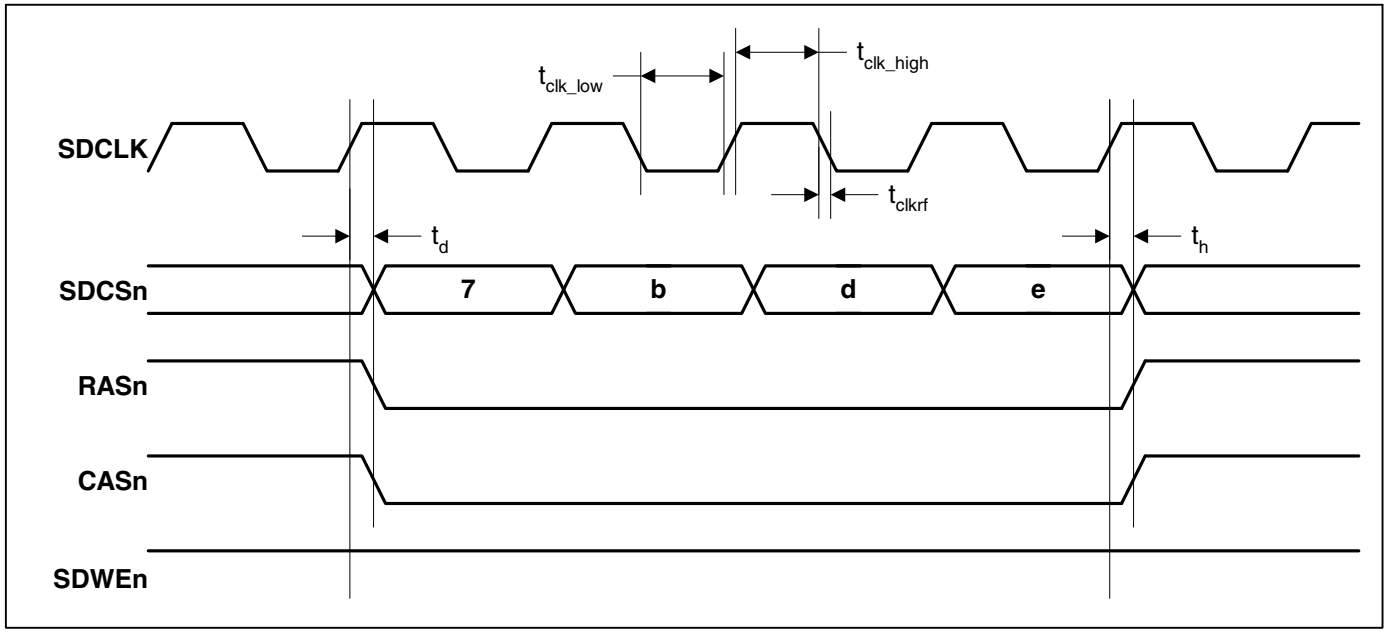


Figure 4. SDRAM Burst Write Cycle Timing Measurement

SDRAM Auto Refresh Cycle



Note: Chip select shown as bus to illustrate multiple devices being put into auto refresh in one access

Figure 5. SDRAM Auto Refresh Cycle Timing Measurement

Static Memory Single Word Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	t_{HCLK} - 3	-	-	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
WRn deassert to CSn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpw}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
WRn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn assert to DA valid	t_{DAV}	-	-	8	ns

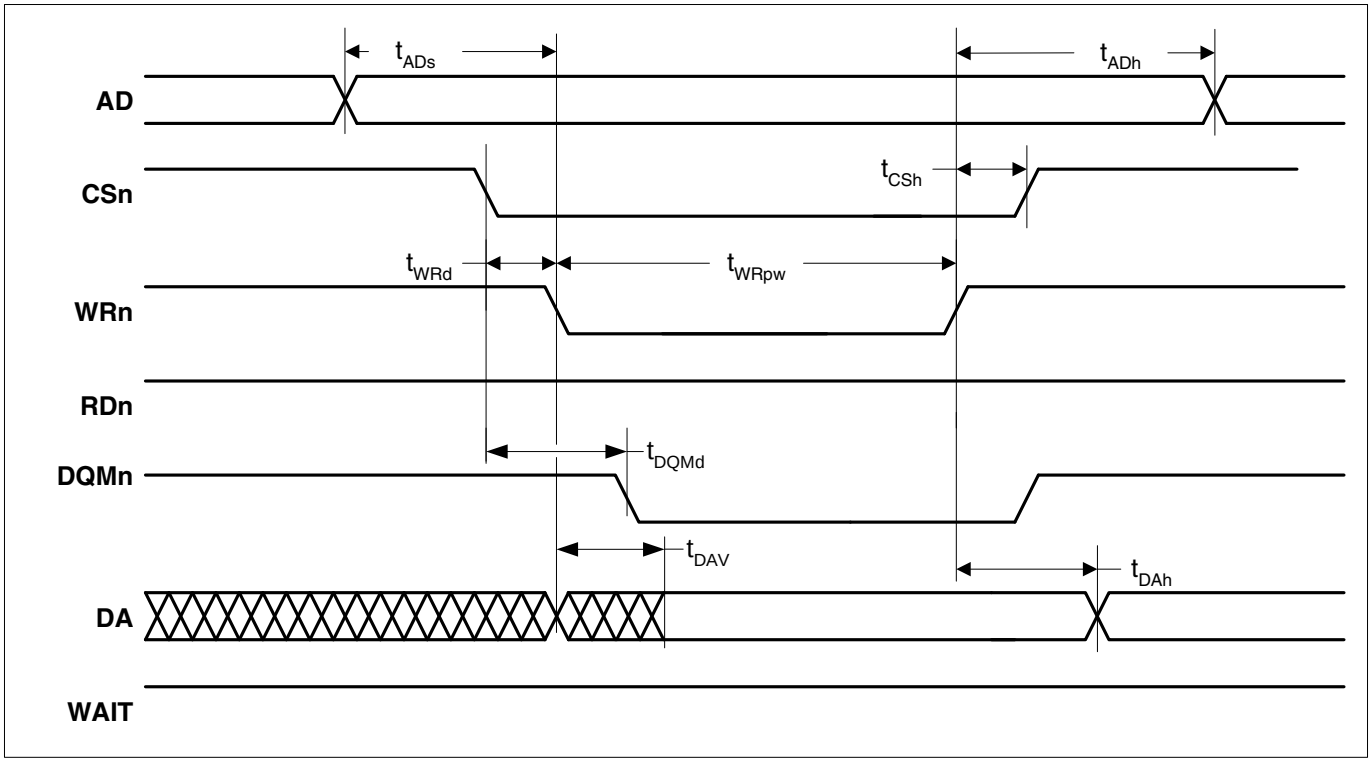


Figure 7. Static Memory Single Word Write Cycle Timing Measurement

Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

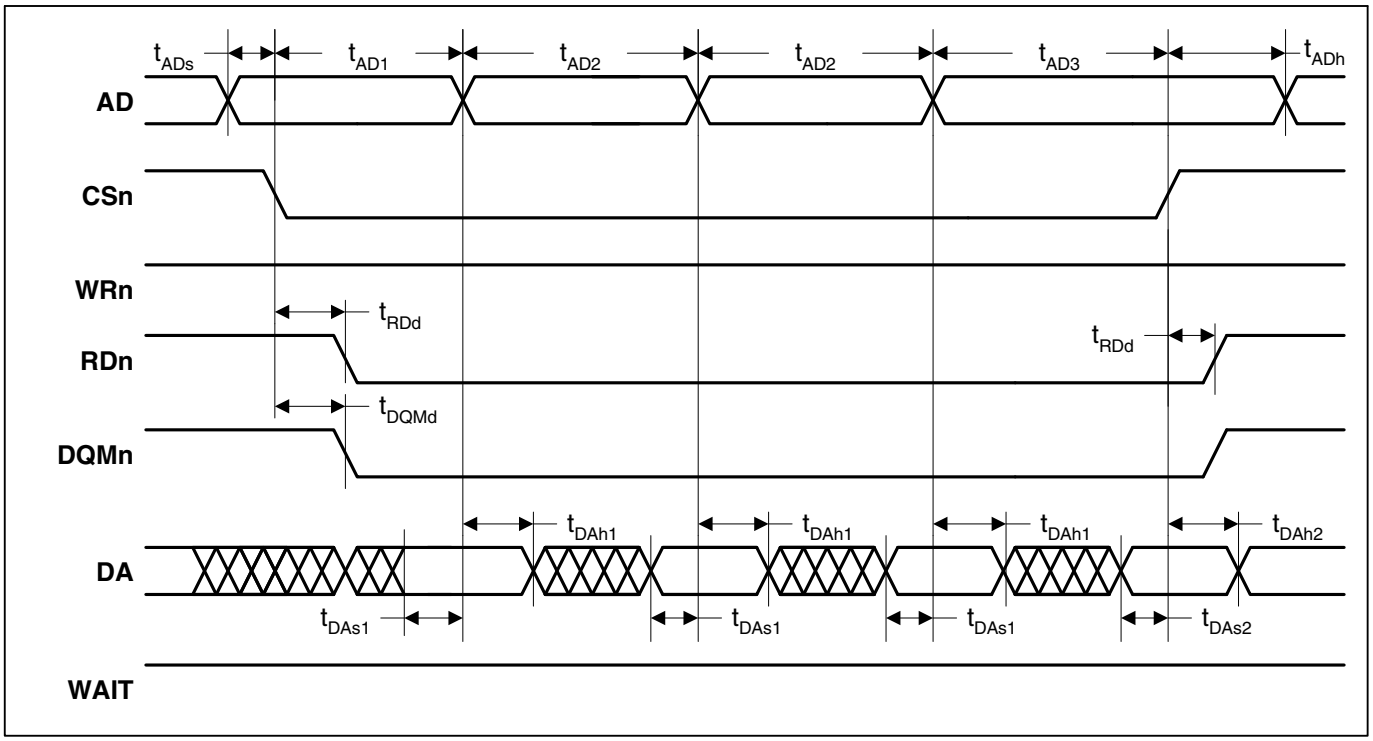


Figure 8. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

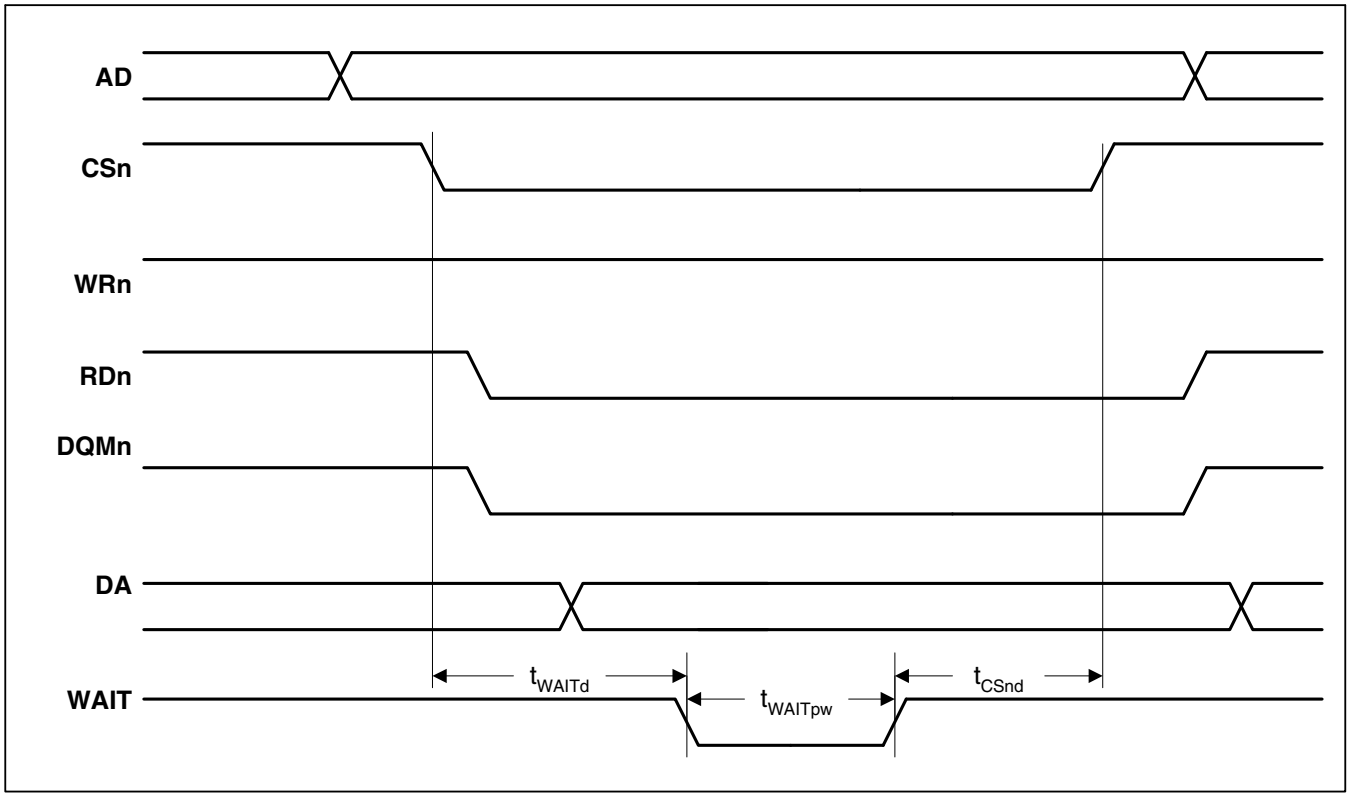


Figure 14. Static Memory Single Read Wait Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

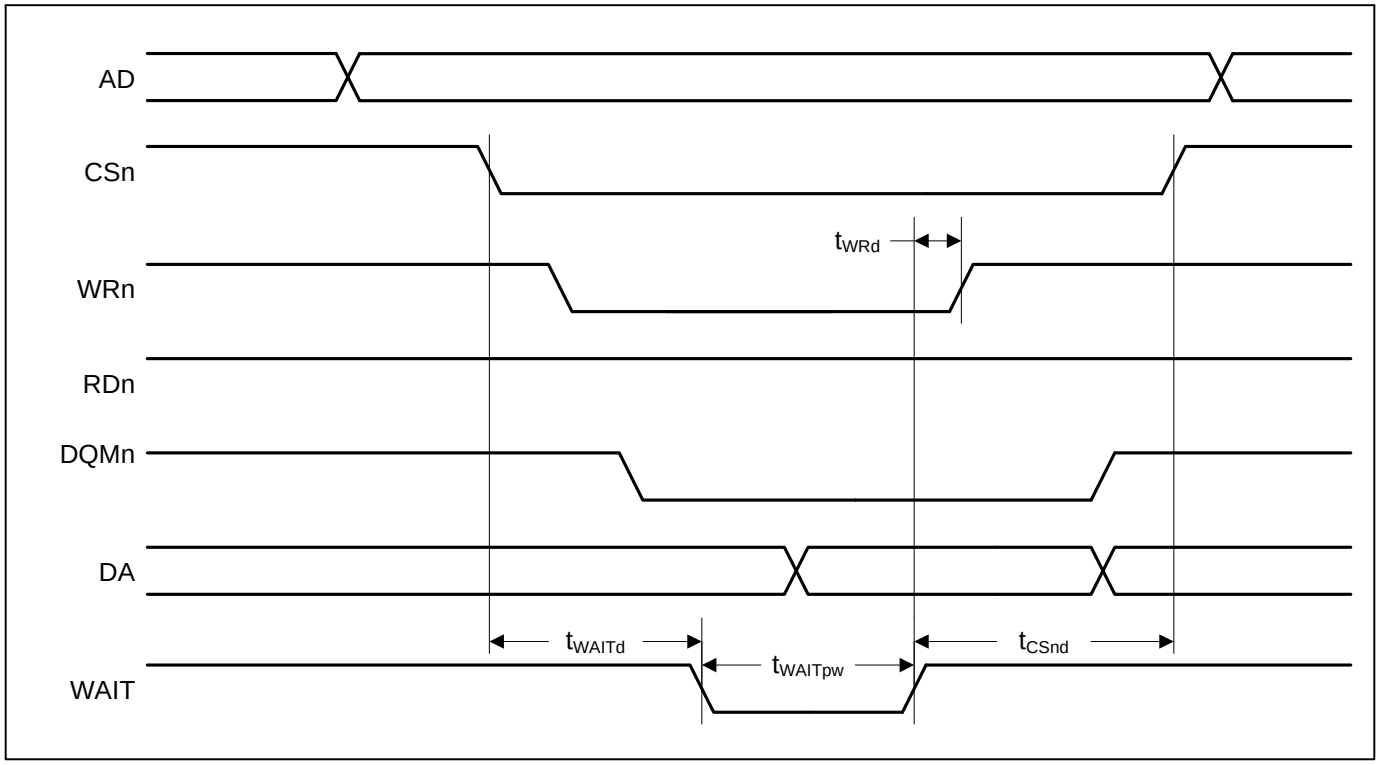


Figure 15. Static Memory Single Write Wait Cycle Timing Measurement

JTAG

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	100	-	ns
TCK clock high time	t_{clk_high}	50	-	ns
TCK clock low time	t_{clk_low}	50	-	ns
TMS / TDI to clock rising setup time	t_{JPs}	20	-	ns
Clock rising to TMS / TDI hold time	t_{JPh}	45	-	ns
JTAG port clock to output	t_{JPco}	-	30	ns
JTAG port high impedance to valid output	t_{JPzx}	-	30	ns
JTAG port valid output to high impedance	t_{JPxz}	-	30	ns

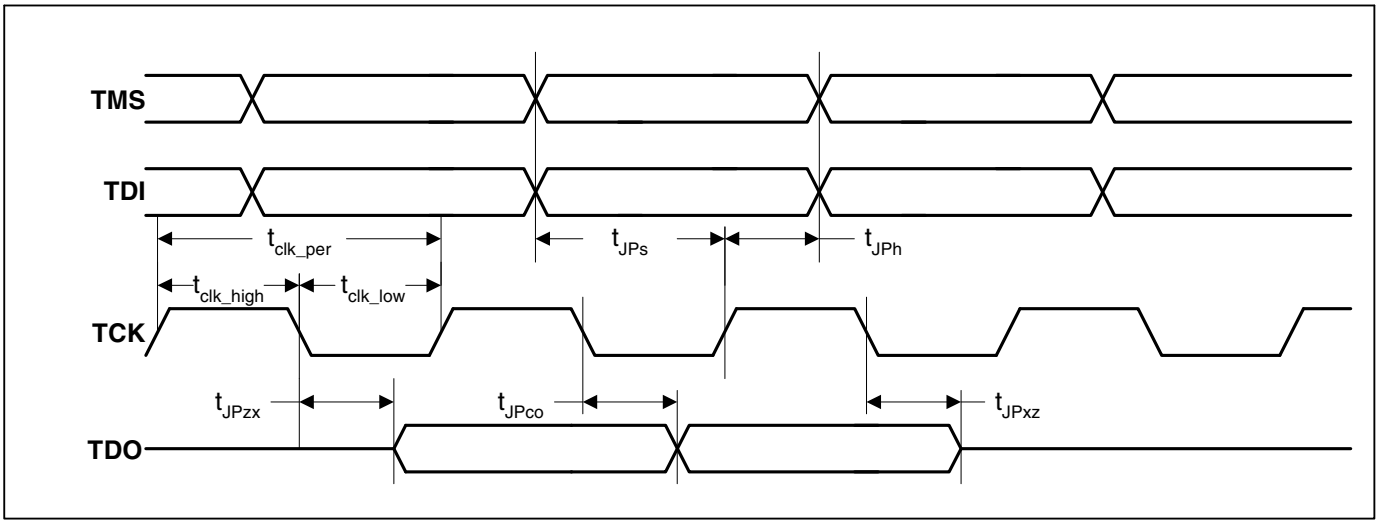
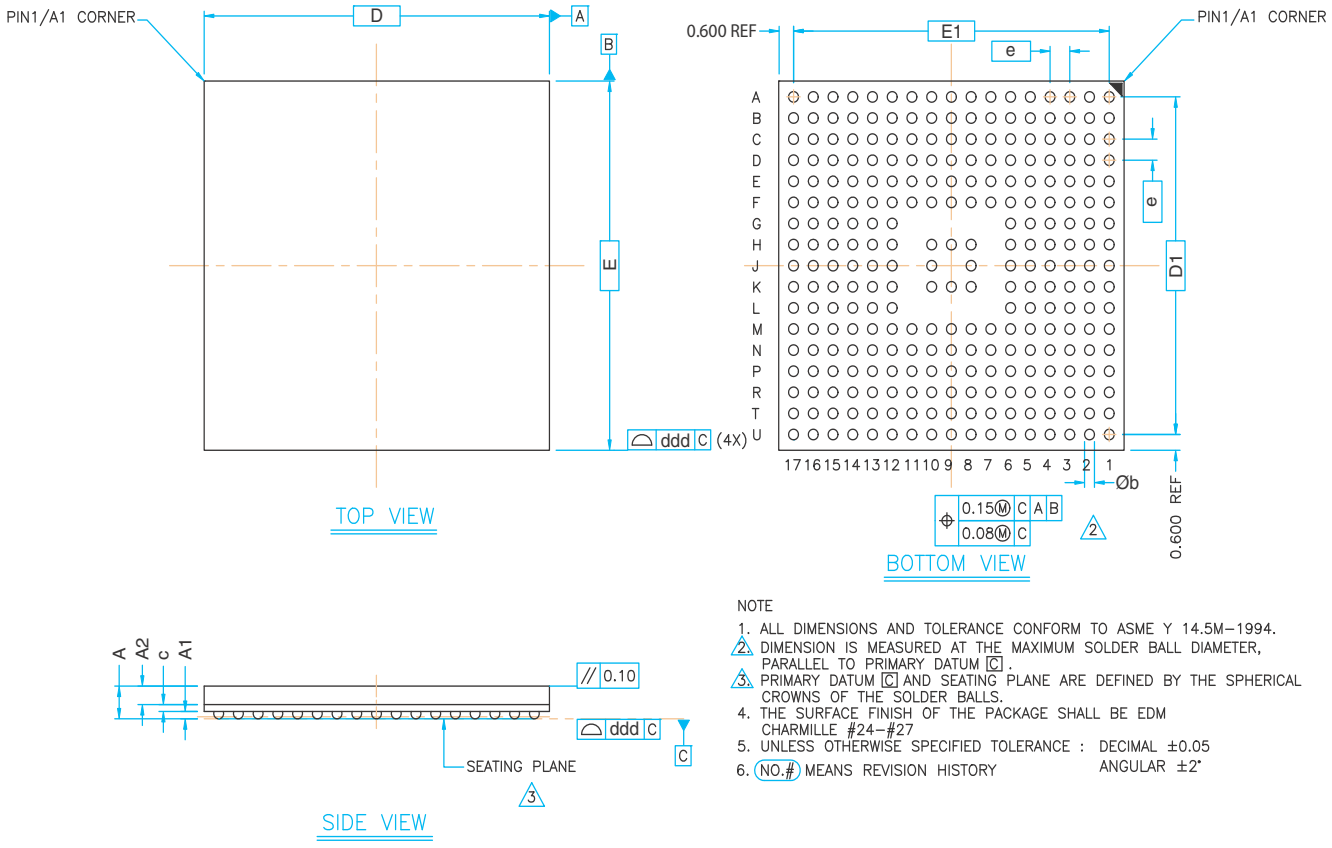


Figure 25. JTAG Timing Measurement

272 Pin TFBGA Package Outline

272 TFBGA Diagram

Figure 26. 272 Pin TFBGA Diagram



NOTE
1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M–1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C .
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARMILLE #24–#27
5. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05 ANGULAR ±2˚
6. NO.# MEANS REVISION HISTORY

Table R. 272 Pin Diagram Dimensions

Symbol	dimension in mm			dimension in inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.40	1.45	0.053	0.055	0.057
A1	0.23	0.28	0.33	0.009	0.011	0.013
A2	0.65	0.70	0.75	0.026	0.028	0.030
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.21	0.26	0.31	0.0083	0.0102	0.0122
D	13.95	14.00	14.05	0.549	0.551	0.553
D3	12.75	12.80	12.85	0.502	0.504	0.506
E	13.95	14.00	14.05	0.549	0.551	0.553
E3	12.75	12.80	12.85	0.502	0.504	0.506
e	0.75	0.80	0.85	0.030	0.031	0.033
ddd			0.10			0.004

Note: 1. Controlling Dimension: Millimeter.
2. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to Primary Datum C.
4. There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
5. Reference Document: JEDEC MO-151, BAL-2

272 Pin TFBGA Pinout (Bottom View)

The following table shows the 272 pin TFBGA pinout. (For better understanding, compare the coordinates on the x and y axis on Figure 27, "272 Pin TFBGA Pinout", on page 42 with Figure 26, "272 Pin TFBGA Diagram", on page 40.

- VDD_core is vddc.
- VDD_ring is vddr.
- GND_core is gndc.
- GND_ring is gndr.

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
C9	MDIO	G14	EGPIO[10]	M9	vddc	T9	DSRn
C10	MIIRXD[2]	G15	EGPIO[11]	M10	gndr	T10	TMS
C11	TXCLK	G16	RTCXTALO	M11	gndr	T11	gndr
C12	MIITXD[0]	G17	RTCXTALI	M12	ROW[6]	T12	SFRM[1]
C13	CLD	H1	DA[18]	M13	ROW[4]	T13	INT[2]
C14	EGPIO[13]	H2	DA[20]	M14	ROW[1]	T14	INT[0]
C15	TRSTn	H3	DA[19]	M15	ROW[0]	T15	USBp[1]
C16	Xp	H4	DA[16]	M16	ROW[3]	T16	NC
C17	Xm	H5	vddr	M17	ROW[2]	T17	NC
D1	SDCSn[3]	H6	vddc	N1	P[14]	U1	NC
D2	DA[23]	H8	gndc	N2	P[16]	U2	NC
D3	SDCLK	H9	gndc	N3	P[15]	U3	P[8]
D4	DA[24]	H10	gndc	N4	P[13]	U4	P[4]
D5	HGPIO[7]	H12	gndr	N5	P[12]	U5	P[1]
D6	HGPIO[6]	H13	vddr	N6	DA[5]	U6	DA[6]
D7	DA[28]	H14	EGPIO[8]	N7	vddr	U7	DA[3]
D8	HGPIO[4]	H15	PRSTn	N8	vddr	U8	AD[10]
D9	AD[16]	H16	COL[7]	N9	vddr	U9	DA[0]
D10	MDC	H17	RSTOn	N10	vddr	U10	TDO
D11	RXERR	J1	AD[6]	N11	EECLK	U11	NC
D12	MIITXD[3]	J2	DA[14]	N12	ASDO	U12	SCLK[1]
D13	EGPIO[12]	J3	AD[7]	N13	CTSn	U13	SSPRX[1]
D14	EGPIO[1]	J4	DA[13]	N14	RXD[0]	U14	INT[1]
D15	EGPIO[0]	J5	vddr	N15	TXD[0]	U15	RTSn
D16	Ym	J6	vddc	N16	TXD[1]	U16	USBm[1]
D17	Yp	J8	gndc	N17	TXD[2]	U17	NC

The following section focuses on the EP9307 pin signals from two viewpoints - the pin usage and pad characteristics, and the pin multiplexing usage. The first table (Table S) is a summary of all the EP9307 pin signals. The second table (Table T) illustrates the pin signal multiplexing and configuration options.

Table S is a summary of the EP9307 pin signals, which illustrates the pad type and pad pull type (if any). The symbols used in the table are defined as follows. (Note: A blank box means Not Applicable (NA) or, for Pull Type, No Pull (NP).)

Under the Pad Type column:

- A - Analog pad
- P - Power pad
- G - Ground pad
- I - Pin is an input only
- I/O - Pin is input/output
- 4mA - Pin is a 4mA output driver
- 8mA - Pin is an 8mA output driver
- 12mA - Pin is an 12mA output driver

See the text description for additional information about bi-directional pins.

Under the Pull Type Column:

- PU - Resistor is a pull up to the RVDD supply
- PD - Resistor is a pull down to the RGND supply

Table T illustrates the pin signal multiplexing and configuration options.

Table T. Pin Multiplex Usage Information

Physical Pin Name	Description	Multiplex signal name
COL[7:0]	GPIO	GPIO Port D[7:0]
ROW[7:0]	GPIO	GPIO Port C[7:0]
EGPIO[0]	Ring Indicator Input	RI
EGPIO[1]	1Hz clock monitor	CLK1HZ
EGPIO[2]	DMA request	DMARQ
EGPIO[3]	HDLC Clock	HDLCCLK1
EGPIO[4]	I2S Transmit Data 1	SDO1
EGPIO[5]	I2S Receive Data 1	SDI1
EGPIO[6]	I2S Transmit Data 2	SDO2
EGPIO[7]	DMA Request 0	DREQ0
EGPIO[8]	DMA Acknowledge 0	DACK0
EGPIO[9]	DMA EOT 0	DEOT0
EGPIO[10]	DMA Request 1	DREQ1
EGPIO[11]	DMA Acknowledge 1	DACK1
EGPIO[12]	DMA EOT 1	DEOT1
EGPIO[13]	I2S Receive Data 2	SDI2
EGPIO[15]	Device active / present	DASP
ABITCLK	I2S Serial clock	SCLK
ASYNC	I2S Frame Clock	LRCK
ASDO	I2S Transmit Data 0	SDO0
ASDI	I2S Receive Data 0	SDI0
ARSTn	I2S Master clock	MCLK
SCLK1	I2S Serial clock	SCLK
SFRM1	I2S Frame Clock	LRCK
SSPTX1	I2S Transmit Data 0	SDO0
SSPRX1	I2S Receive Data 0	SDI0