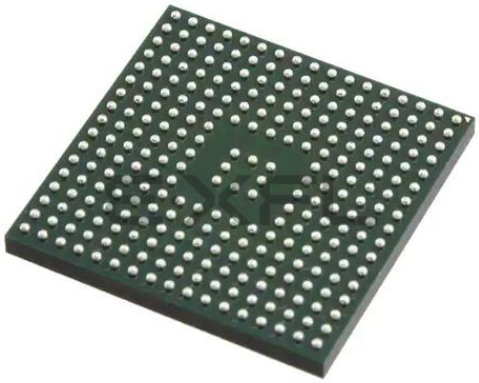

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	272-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9307-irz

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List of Tables

Processor Core - ARM920T

The ARM920T is a Harvard architecture processor with separate 16 kbyte instruction and data caches with an 8-word line length but a unified memory. The processor utilizes a five-stage pipeline consisting of fetch, decode, execute, memory and write stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16 kbyte Instruction Cache with lockdown
- 16 kbyte Data Cache (programmable write-through or write-back) with lockdown
- MMU for Linux®, Microsoft® Windows® CE and other operating systems
- Translation Look Aside Buffers with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 1 Mbyte, 64 kbyte, 4 kbyte, and 1 kbyte
- Independent lockdown of TLB Entries

MaverickCrunch™ Math Engine

The MaverickCrunch Engine is a mixed-mode coprocessor designed primarily to accelerate the math processing required to rapidly encode digital audio formats. It accelerates single- and double-precision integer and floating point operations plus an integer multiply-accumulate (MAC) instruction that is considerably faster than the ARM920T's native MAC instruction. The ARM920T coprocessor interface is utilized thereby sharing its memory interface and instruction stream. Hardware forwarding and interlock allows the ARM to handle looping and addressing while MaverickCrunch handles computation. Features include:

- IEEE-754 single and double precision floating point
- 32/64-bit integer
- Add/multiply/compare
- Integer MAC 32-bit input with 72-bit accumulate
- Integer Shifts
- Floating point to/from integer conversion
- Sixteen 64-bit register files
- Four 72-bit accumulators

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID are programmed into the EP9307 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP9307 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

General Purpose Memory Interface (SDRAM, SRAM, ROM, FLASH)

The EP9307 features a unified memory address model where all memory devices are accessed over a common address/data bus. A separate internal port is dedicated to the read-only Raster/LCD refresh engine, while the rest of the memory accesses are performed via the Processor bus. The SRAM memory controller supports 8, 16 and 32-bit devices and accommodates an internal boot ROM concurrently with 32-bit SDRAM memory.

- 1 to 4 banks of 32-bit, 100 MHz SDRAM
- One internal port dedicated to the Raster/LCD Refresh Engine (Read Only)
- Address and data bus shared between SDRAM, SRAM, ROM, and FLASH memory
- NOR FLASH memory supported

Table B. General Purpose Memory Interface Pin Assignments

Pin Mnemonic	Pin Description
SDCLK	SDRAM Clock
SDCLKEN	SDRAM Clock Enable
SDCSn[3:0]	SDRAM Chip Selects 3-0
RASn	SDRAM RAS
CASn	SDRAM CAS
SDWEn	SDRAM Write Enable
CSn[7:6] and CSn[3:0]	Chip Selects 7, 6, 3, 2, 1, 0
AD[25:0]	Address Bus 25-0
DA[31:0]	Data Bus 31-0
DQMn[3:0]	SDRAM Output Enables / Data Masks
WRn	SRAM Write Strobe
RDn	SRAM Read/OE Strobe
WAITn	SRAM Wait Input

Ethernet Media Access Controller (MAC)

The MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported. Features include:

- Supports 1/10/100 Mbps transfer rates for home/small-business/large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

Table C. Ethernet Media Access Controller Pin Assignments

Pin Mnemonic	Pin Description
MDC	Management Data Clock
MDIO	Management Data I/O
RXCLK	Receive Clock
MIIRXD[3:0]	Receive Data
RXDVAL	Receive Data Valid
RXERR	Receive Data Error
TXCLK	Transmit Clock
MIITXD[3:0]	Transmit Data
TXEN	Transmit Enable
TXERR	Transmit Error
CRS	Carrier Sense
CLD	Collision Detect

Serial Interfaces (SPI, I^{2}S and AC ’97)

The SPI port can be configured as a master or a slave, supporting the National Semiconductor®, Motorola®, and Texas Instruments® signaling protocols.

The AC'97 port supports multiple codecs for multichannel audio output with a single stereo input. The I^{2}S port can be configured to support two channel, 24 bit audio.

These ports are multiplexed so that I^{2}S port 0 will take over either the AC'97 pins or the SPI pins. The second and third I2S ports' serial input and serial output pins are multiplexed with EGPIO[4,5,6,13]. The clocks supplied in the first I2S port are also used for the second and third I2S ports.

- Normal Mode: One SPI Port and one AC’97 Port
- I^{2}S on SSP Mode: One AC’97 Port and up to three I^{2}S Ports
- I^{2}S on AC’97 Mode: One SPI Port and up to three I^{2}S Ports

Note: I^{2}S may not be output on AC’97 and SSP ports at the same time.

Table D. Audio Interfaces Pin Assignment

Pin Name	Normal Mode	I2S on SSP Mode	I2S on AC'97 Mode
	Pin Description	Pin Description	Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

Raster/LCD Interface

The Raster/LCD interface provides data and interface signals for a variety of display types. It features fully programmable video interface timing for non-interlaced flat panel or dual scan displays. Resolutions up to 1024 x 768 are supported from a unified SDRAM based frame buffer. A 16-bit PWM provides control for LCD panel contrast. LCD specific features include:

- Timing and interface signals for digital LCD and TFT displays
- Full programmability for either non-interlaced or dual-scan color and grayscale flat panel displays
- Dedicated data path to SDRAM controller for improved system performance
- Pixel depths of 4, 8, 16, or 24 bits per pixel or 256 levels of grayscale
- Hardware Cursor up to 64 x 64 pixels
- 256 x 18 Color Lookup Table
- Hardware Blinking
- 8-bit interface to low-end panel

Universal Asynchronous Receiver/Transmitters (UARTs)

Three 16550-compatible UARTs are supplied. Two provide asynchronous HDLC (High-level Data Link Control) protocol support for full duplex transmit and receive. The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency, and optionally passes the CRC to the host at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency. The host must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams. A third IrDA® compatible UART is also supplied.

- UART1 supports modem bit rates up to 115.2 kbps, supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.
- UART3 supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx and Tx.

Table H. Universal Asynchronous Receiver / Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTSn	UART1 Clear To Send / Transmit Enable
DSRn/DCDn	UART1 Data Set Ready / Data Carrier Detect
DTRn	UART1 Data Terminal Ready
RTSn	UART1 Ready To Send
EGPIO[0]/RI	UART1 Ring Indicator
TXD1/SIROUT	UART2 Transmit / IrDA Output
RXD1/SIRIN	UART2 Receive / IrDA Input
TXD2	UART3 Transmit
RXD2	UART3 Receive
TENn	HDLC3 Transmit Enable

Internal Boot ROM

The Internal 16-kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP9307 User's Guide for operational details.

Triple-port USB Host

The USB Open Host Controller Interface (Open HCI) provides full-speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB "tiered-star" topology.

This includes the following features:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB device connections
- Root HUB integrated with 3 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table I. Triple Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2:0]	USB Positive signals
USBm[2:0]	USB Negative Signals

Two-wire Interface Support

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table J. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Table O. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15] EGPIO[13:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[7] FGPIO[5] FGPIO[0]	Expanded General Purpose Input / Output Pins with Interrupts

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 200 MHz (184 MHz for industrial conditions).

Table P. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table Q. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-Channel DMA Controller

The DMA module contains 12 separate DMA channels. These may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated due to AC and/or DC output loading.
2. The power supply pins are at maximum values listed in "Recommended Operating Conditions", below.

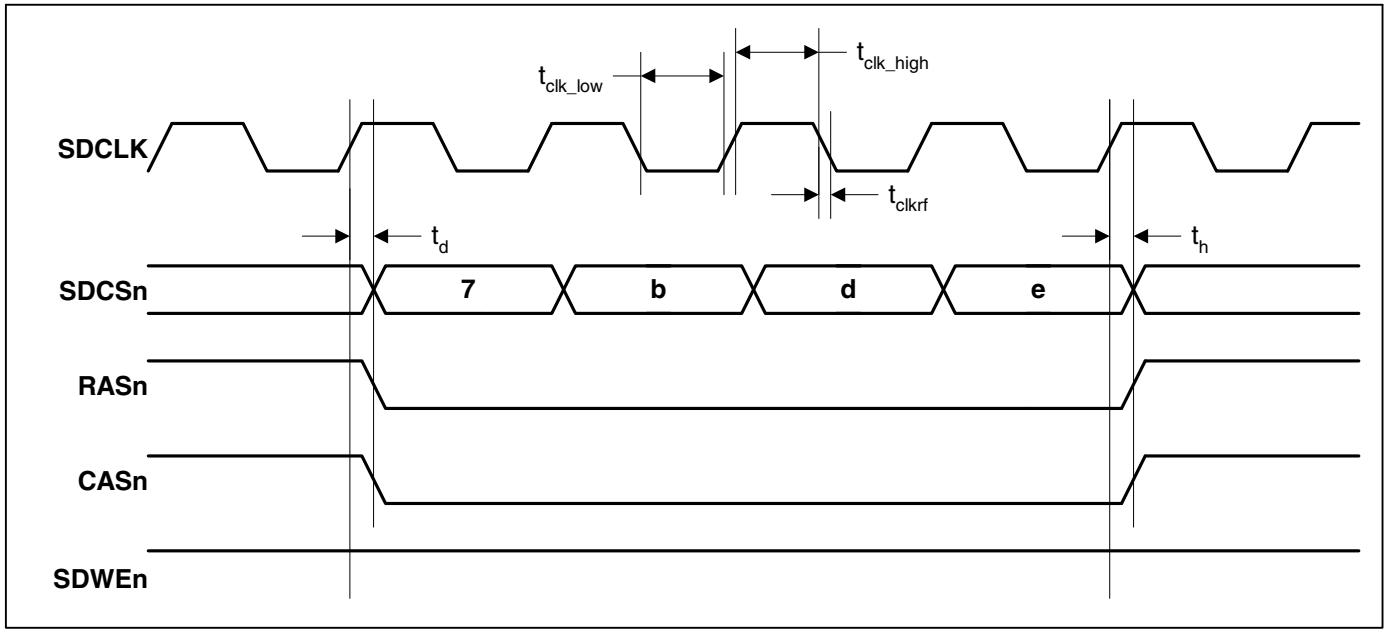
WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	3.0 1.71 1.71 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	200	MHz
Processor Clock Speed - Industrial	FCLK	-	-	184	MHz
System Clock Speed - Commercial	HCLK	-	-	100	MHz
System Clock Speed - Industrial	HCLK	-	-	92	MHz

SDRAM Auto Refresh Cycle



Note: Chip select shown as bus to illustrate multiple devices being put into auto refresh in one access

Figure 5. SDRAM Auto Refresh Cycle Timing Measurement

Static Memory Burst Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to Address 1 transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{ADd2}	-	$t_{HCLK} \times (WST2 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to CSn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

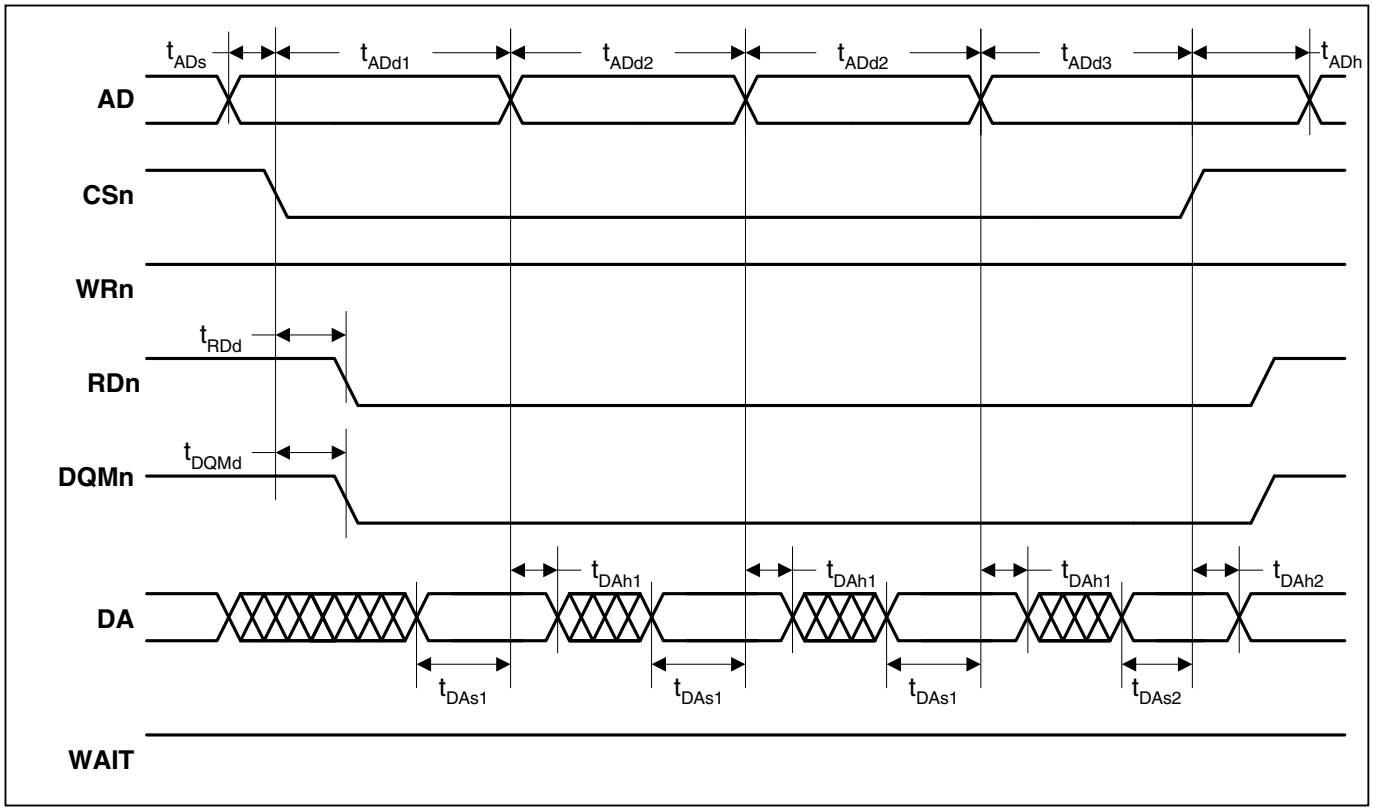


Figure 12. Static Memory Burst Read Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

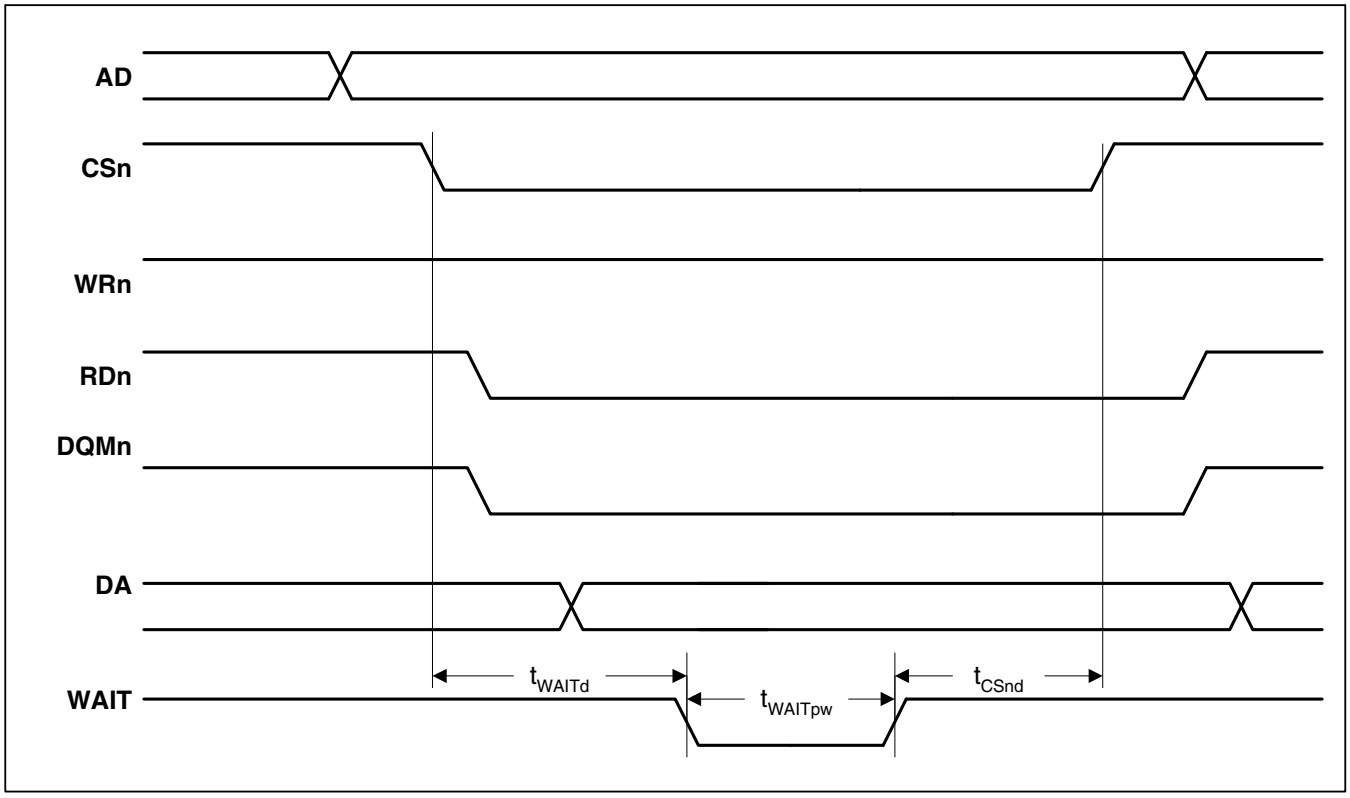


Figure 14. Static Memory Single Read Wait Cycle Timing Measurement

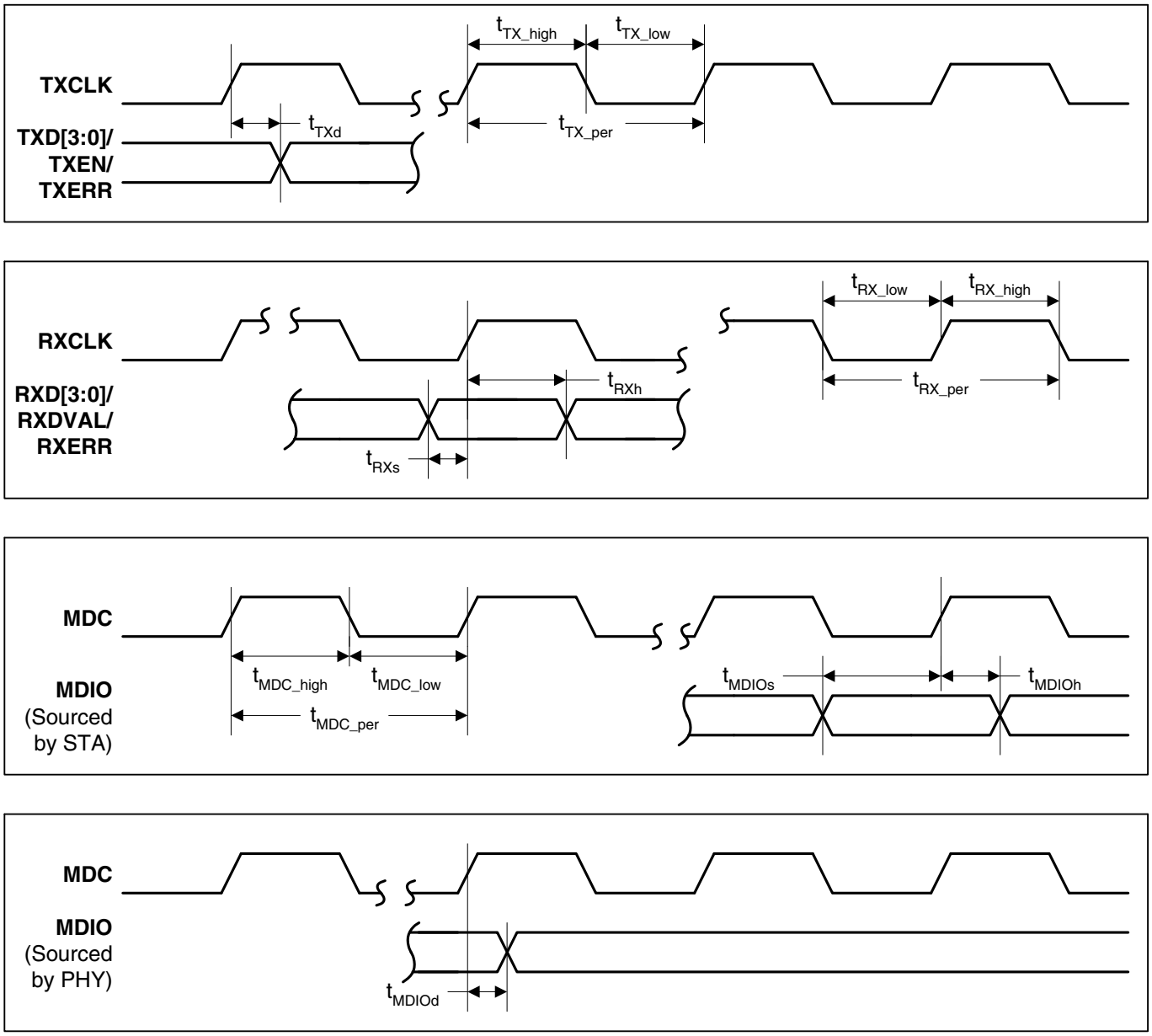


Figure 17. Ethernet MAC Timing Measurement

Inter-IC Sound - I²S

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	t_{i2s_clk}	-	ns
SCLK high time	t_{clk_high}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK low time	t_{clk_low}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK rise/fall time	t_{clkrf}	1	4	8	ns
SCLK to LRCLK assert delay time	t_{LRd}	-	-	3	ns
Hold between SCLK assert then LRCLK deassert *or* Hold between LRCLK deassert then SCLK assert	t_{LRh}	0	-	-	ns
SDI to SCLK deassert setup time	t_{SDIs}	12	-	-	ns
SDI from SCLK deassert hold time	t_{SDIh}	0	-	-	ns
SCLK assert to SDO delay time	t_{SDOd}	-	-	9	ns
SDO from SCLK assert hold time	t_{SDOh}	1	-	-	ns

Note: t_{i2s_clk} is programmable by the user.

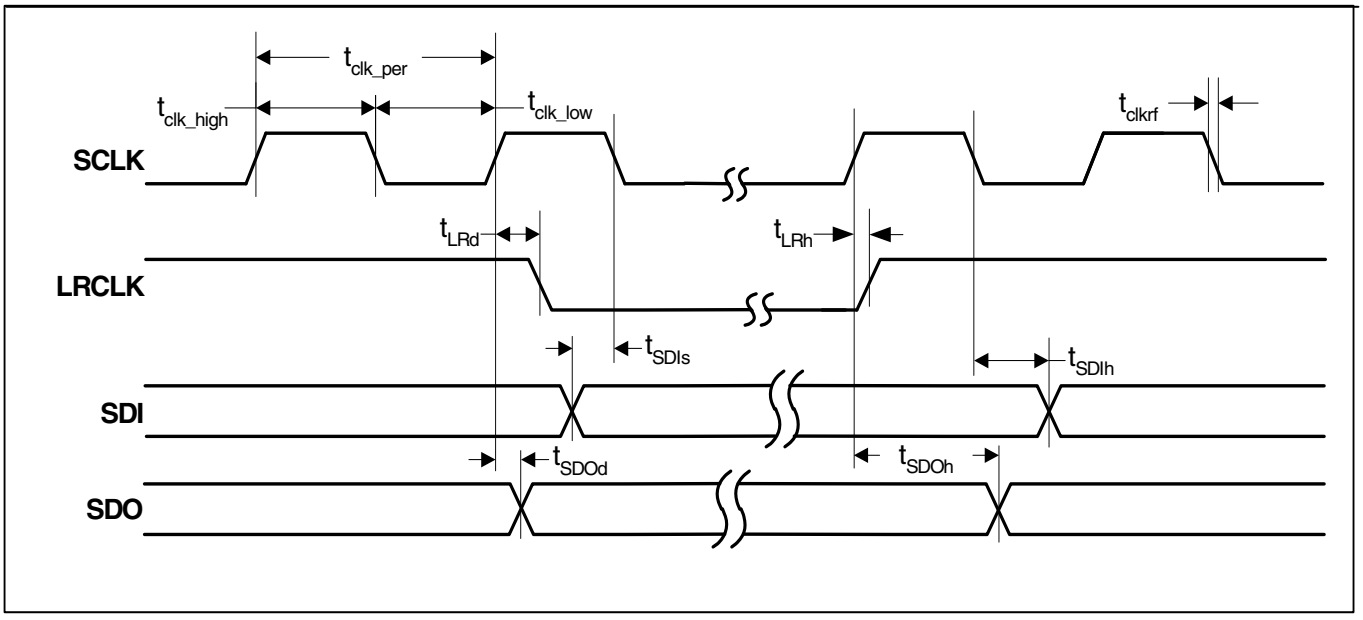


Figure 21. Inter-IC Sound (I^2S) Timing Measurement

AC'97

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK input cycle time	t_{clk_per}	-	81.4	-	ns
ABITCLK input high time	t_{clk_high}	36	-	45	ns
ABITCLK input low time	t_{clk_low}	36	-	45	ns
ABITCLK input rise/fall time	t_{clkrf}	2	-	6	ns
ASDI setup to ABITCLK falling	t_s	10	-	-	ns
ASDI hold after ABITCLK falling	t_h	10	-	-	ns
ASDI input rise/fall time	t_{rfin}	2	-	6	ns
ABITCLK rising to ASDO / ASYNC valid, C_L = 55 pF	t_{co}	2	-	15	ns
ASYNC / ASDO rise/fall time, C_L = 55 pF	t_{rfout}	2	-	6	ns

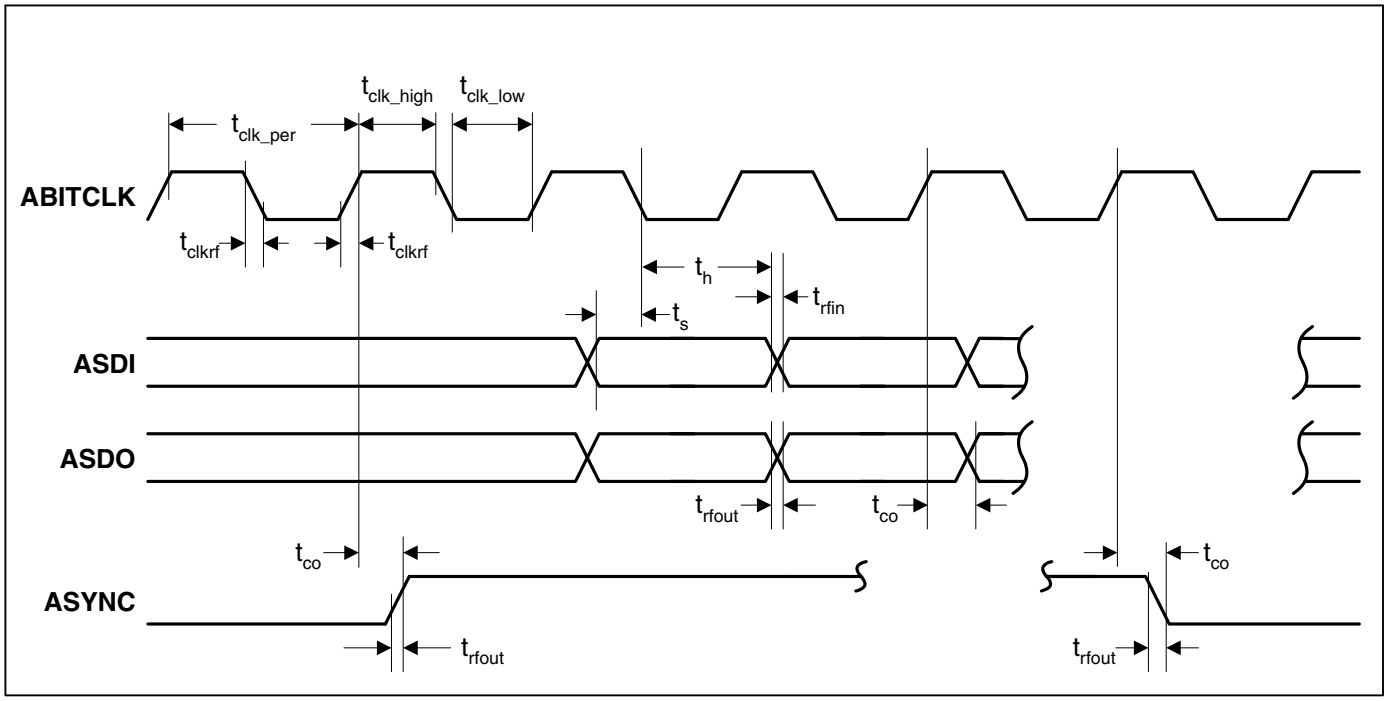
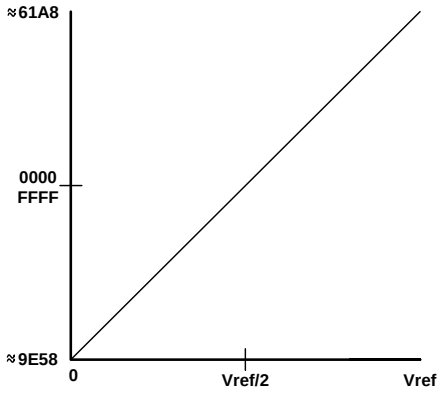


Figure 22. AC '97 Configuration Timing Measurement

ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 24. ADC Transfer Function

Using the ADC:

This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

Figure 27. 272 Pin TFBGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
U	NC	NC	P[8]	P[4]	P[1]	DA[6]	DA[3]	AD[10]	DA[0]	TDO	NC	SCLK[1]	SSPRX[1]	INT[1]	RTSn	USBm[1]	NC	U
T	NC	NC	V_CSYNC	P[7]	P[2]	DA[7]	AD[11]	AD[9]	DSRn	TMS	gndr	SFRM[1]	INT[2]	INT[0]	USBp[1]	NC	NC	T
R	P[9]	HSYNC	P[6]	P[5]	P[0]	AD[14]	DA[4]	DA[1]	DTRn	TDI	BOOT[0]	ASYNC	SSPTX[1]	PWMOUT	USBm[0]	ABITCLK	USBp[0]	R
P	SPCLK	P[10]	P[11]	P[3]	AD[15]	AD[13]	AD[12]	DA[2]	AD[8]	TCK	BOOT[1]	EEDAT	GRLED	RDLED	GGPIO[2]	RXD[1]	RXD[2]	P
N	P[14]	P[16]	P[15]	P[13]	P[12]	DA[5]	vddr	vddr	vddr	vddr	EECLK	ASDO	CTSn	RXD[0]	TXD[0]	TXD[1]	TXD[2]	N
M	BRIGHT	AD[0]	DQMn[1]	DQMn[2]	P[17]	gndr	gndr	vddc	vddc	gndr	gndr	ROW[6]	ROW[4]	ROW[1]	ROW[0]	ROW[3]	ROW[2]	M
L	DA[9]	AD[2]	AD[1]	DA[8]	BLANK	gndr						gndr	ROW[7]	ROW[5]	PLL_GND	XTALI	XTALO	L
K	AD[4]	DA[12]	DA[10]	DA[11]	vddr	gndr		gndc	gndc	gndc		vddc	COL[4]	PLL_VDD	COL[2]	COL[1]	COL[0]	K
J	AD[6]	DA[14]	AD[7]	DA[13]	vddr	vddc		gndc		gndc		vddc	vddr	COL[5]	COL[6]	CSn[0]	COL[3]	J
H	DA[18]	DA[20]	DA[19]	DA[16]	vddr	vddc		gndc	gndc	gndc		gndr	vddr	EGPIO[8]	PRSTn	COL[7]	RSTOn	H
G	DQMn[0]	CASn	DA[21]	AD[22]	vddr	gndr						gndr	EGPIO[9]	EGPIO[10]	EGPIO[11]	RTCXTALO	RTCXTALI	G
F	RASn	SDCSn[1]	SDCSn[0]	DQMn[3]	AD[5]	gndr	gndr	gndr	vddc	vddc	gndr	EGPIO[7]	EGPIO[5]	ADC_GND	EGPIO[6]	sYm	sYp	F
E	SDCSn[2]	SDWEN	DA[22]	AD[3]	DA[15]	AD[21]	DA[17]	vddr	vddr	vddr	MIIRXD[0]	TXERR	EGPIO[2]	EGPIO[4]	EGPIO[3]	sXp	sXm	E
D	SDCSn[3]	DA[23]	SDCLK	DA[24]	HGPIO[7]	HGPIO[6]	DA[28]	HGPIO[4]	AD[16]	MDC	RXERR	MIITXD[3]	EGPIO[12]	EGPIO[1]	EGPIO[0]	Ym	Yp	D
C	AD[23]	DA[26]	CSn[3]	DA[25]	AD[24]	AD[19]	HGPIO[5]	WRn	MDIO	MIIRXD[2]	TXCLK	MIITXD[0]	CLD	EGPIO[13]	TRSTn	Xp	Xm	C
B	AD[25]	CSn[2]	CSn[6]	AD[20]	DA[30]	AD[18]	HGPIO[3]	AD[17]	RXCLK	MIIRXD[1]	MIITXD[2]	TXEN	FGPIO[5]	EGPIO[15]	USBp[2]	ARSTn	ADC_VDD	B
A	CSn[1]	CSn[7]	SDCLKEN	DA[31]	DA[29]	DA[27]	HGPIO[2]	RDn	MIIRXD[3]	RXDVAL	MIITXD[1]	CRS	FGPIO[7]	FGPIO[0]	WAITn	USBm[2]	ASDI	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
C9	MDIO	G14	EGPIO[10]	M9	vddc	T9	DSRn
C10	MIIRXD[2]	G15	EGPIO[11]	M10	gndr	T10	TMS
C11	TXCLK	G16	RTCXTALO	M11	gndr	T11	gndr
C12	MIITXD[0]	G17	RTCXTALI	M12	ROW[6]	T12	SFRM[1]
C13	CLD	H1	DA[18]	M13	ROW[4]	T13	INT[2]
C14	EGPIO[13]	H2	DA[20]	M14	ROW[1]	T14	INT[0]
C15	TRSTn	H3	DA[19]	M15	ROW[0]	T15	USBp[1]
C16	Xp	H4	DA[16]	M16	ROW[3]	T16	NC
C17	Xm	H5	vddr	M17	ROW[2]	T17	NC
D1	SDCSn[3]	H6	vddc	N1	P[14]	U1	NC
D2	DA[23]	H8	gndc	N2	P[16]	U2	NC
D3	SDCLK	H9	gndc	N3	P[15]	U3	P[8]
D4	DA[24]	H10	gndc	N4	P[13]	U4	P[4]
D5	HGPIO[7]	H12	gndr	N5	P[12]	U5	P[1]
D6	HGPIO[6]	H13	vddr	N6	DA[5]	U6	DA[6]
D7	DA[28]	H14	EGPIO[8]	N7	vddr	U7	DA[3]
D8	HGPIO[4]	H15	PRSTn	N8	vddr	U8	AD[10]
D9	AD[16]	H16	COL[7]	N9	vddr	U9	DA[0]
D10	MDC	H17	RSTOn	N10	vddr	U10	TDO
D11	RXERR	J1	AD[6]	N11	EECLK	U11	NC
D12	MIITXD[3]	J2	DA[14]	N12	ASDO	U12	SCLK[1]
D13	EGPIO[12]	J3	AD[7]	N13	CTSn	U13	SSPRX[1]
D14	EGPIO[1]	J4	DA[13]	N14	RXD[0]	U14	INT[1]
D15	EGPIO[0]	J5	vddr	N15	TXD[0]	U15	RTSn
D16	Ym	J6	vddc	N16	TXD[1]	U16	USBm[1]
D17	Yp	J8	gndc	N17	TXD[2]	U17	NC

The following section focuses on the EP9307 pin signals from two viewpoints - the pin usage and pad characteristics, and the pin multiplexing usage. The first table (Table S) is a summary of all the EP9307 pin signals. The second table (Table T) illustrates the pin signal multiplexing and configuration options.

Table S is a summary of the EP9307 pin signals, which illustrates the pad type and pad pull type (if any). The symbols used in the table are defined as follows. (Note: A blank box means Not Applicable (NA) or, for Pull Type, No Pull (NP).)

Under the Pad Type column:

- A - Analog pad
- P - Power pad
- G - Ground pad
- I - Pin is an input only
- I/O - Pin is input/output
- 4mA - Pin is a 4mA output driver
- 8mA - Pin is an 8mA output driver
- 12mA - Pin is an 12mA output driver

See the text description for additional information about bi-directional pins.

Under the Pull Type Column:

- PU - Resistor is a pull up to the RVDD supply
- PD - Resistor is a pull down to the RGND supply

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Table S. Pin Descriptions

Pin Name	Block	Pad Type	Pull Type	Description
TCK	JTAG	I	PD	JTAG clock in
TDI	JTAG	I	PD	JTAG data in
TDO	JTAG	4ma	-	JTAG data out
TMS	JTAG	I	PD	JTAG test mode select
TRSTn	JTAG	I	PD	JTAG reset
BOOT[1:0]	System	I	PD	Boot mode select in
XTALI	PLL	A	-	Main oscillator input
XTALO	PLL	A	-	Main oscillator output
VDD_PLL	PLL	P	-	Main oscillator power, 1.8V
GND_PLL	PLL	G	-	Main oscillator ground
RTCXTALI	RTC	A	-	RTC oscillator input
RTCXTALO	RTC	A	-	RTC oscillator output
WRn	EBUS	4ma	-	SRAM Write strobe out
RDn	EBUS	4ma	-	SRAM Read/OE strobe out
WAITn	EBUS	I	PU	SRAM Wait in
AD[25:0]	EBUS	8ma	-	Shared Address bus out
DA[31:0]	EBUS	8ma	PU	Shared Data bus in/out
CSn[3:0]	EBUS	4ma	PU	Chip select out
CSn[7:6]	EBUS	4ma	PU	Chip select out
DQMn[3:0]	EBUS	8ma	-	Shared data mask out
SDCLK	SDRAM	8ma	-	SDRAM clock out
SDCLKEN	SDRAM	8ma	-	SDRAM clock enable out
SDCSn[3:0]	SDRAM	4ma	-	SDRAM chip selects out
RASn	SDRAM	8ma	-	SDRAM RAS out
CASn	SDRAM	8ma	-	SDRAM CAS out
SDWEn	SDRAM	8ma	-	SDRAM write enable out
P[17:0]	Raster	4ma	PU	Pixel data bus out
SPCLK	Raster	12ma	PU	Pixel clock in/out
HSYNC	Raster	8ma	PU	Horizontal synchronization/ line pulse out
V_CSYNC	Raster	8ma	PU	Vertical or composite synchronization/frame pulse out
BLANK	Raster	8ma	PU	Composite blanking signal out
BRIGHT	Raster	4ma	-	PWM brightness control out
PWMOUT	PWM	8ma		Pulse width modulator output
Xp, Xm	ADC	A	-	Touchscreen ADC X axis
Yp, Ym	ADC	A	-	Touchscreen ADC Y axis
sXp, sXm	ADC	A	-	Touchscreen ADC X axis feedback
sYp, sYm	ADC	A	-	Touchscreen ADC Y axis feedback
VDD_ADC	ADC	P	-	Touchscreen ADC power, 3.3V
GND_ADC	ADC	G	-	Touchscreen ADC ground
COL[7:0]	Key	8ma	PU	Key matrix column inputs
ROW[7:0]	Key	8ma	PU	Key matrix row outputs
USBp[2:0]	USB	A	-	USB positive signals
USBm[2:0]	USB	A	-	USB negative signals
TXD0	UART1	4ma	-	Transmit out
RXD0	UART1	I	PU	Receive in
CTSn	UART1	I	PU	Clear to send/transmit enable
DSRn	UART1	I	PU	Data set ready/Data Carrier Detect

Table S. Pin Descriptions *(Continued)*

Pin Name	Block	Pad Type	Pull Type	Description
DTRn	UART1	4ma	-	Data Terminal Ready output
RTSn	UART1	4ma	-	Ready to send
TXD1	UART2	4ma	-	Transmit/IrDA output
RXD1	UART2	I	PU	Receive/IrDA input
TXD2	UART3	4ma	-	Transmit
RXD2	UART3	I	PU	Receive
MDC	EMAC	4ma		Management data clock
MDIO	EMAC	4ma	PU	Management data input/output
RXCLK	EMAC	I	PD	Receive clock in
MIIRXD[3:0]	EMAC	I	PD	Receive data in
RXDVAL	EMAC	I	PD	Receive data valid
RXERR	EMAC	I	PD	Receive data error
TXCLK	EMAC	4ma	PU	Transmit clock in
MIITXD[3:0]	EMAC	I	PD	Transmit data out
TXEN	EMAC	4ma	PD	Transmit enable
TXERR	EMAC	4ma	PD	Transmit error
CRS	EMAC	I	PD	Carrier sense
CLD	EMAC	I	PU	Collision detect
GRLED	LED	12ma	-	Green LED
RDLED	LED	12ma	-	Red LED
EECLK	EEPROM	4ma	PU	EEPROM/Two-wire Interface clock
EEDAT	EEPROM	4ma	PU	EEPROM/Two-wire Interface data
ABITCLK	AC97	8ma	PD	AC97 bit clock
ASYNC	AC97	8ma	PD	AC97 frame sync
ASDI	AC97	I	PD	AC97 Primary input
ASDO	AC97	8ma	PU	AC97 output
ARSTn	AC97	8ma	-	AC97 reset
SCLK1	SPI1	8ma	PD	SPI bit clock
SFRM1	SPI1	8ma	PD	SPI Frame Clock
SSPRX1	SPI1	I	PD	SPI input
SSPTX1	SPI1	8ma	-	SPI output
INT[2:0]	INT	I	PD	External interrupts
PRSTn	Syscon	I	PU	Power on reset
RSTOn	Syscon	4ma	-	User Reset in out - open drain
EGPIO[15]	GPIO	I/O, 4ma	PU	Enhanced GPIO
EGPIO[13:0]	GPIO	I/O, 4ma	PU	Enhanced GPIO
FGPIO[7, 5, 0]	GPIO	I/O, 8ma	PU	GPIO
GGPIO[2]	GPIO	I/O, 8ma	PU	GPIO
HGPIO[7:2]	GPIO	I/O, 8ma	PU	GPIO
vddc	Power	P	-	Digital power, 1.8V
vddr	Power	P	-	Digital power, 3.3V
gndc	Ground	G	-	Digital ground
gndr	Ground	G	-	Digital ground

Table T illustrates the pin signal multiplexing and configuration options.

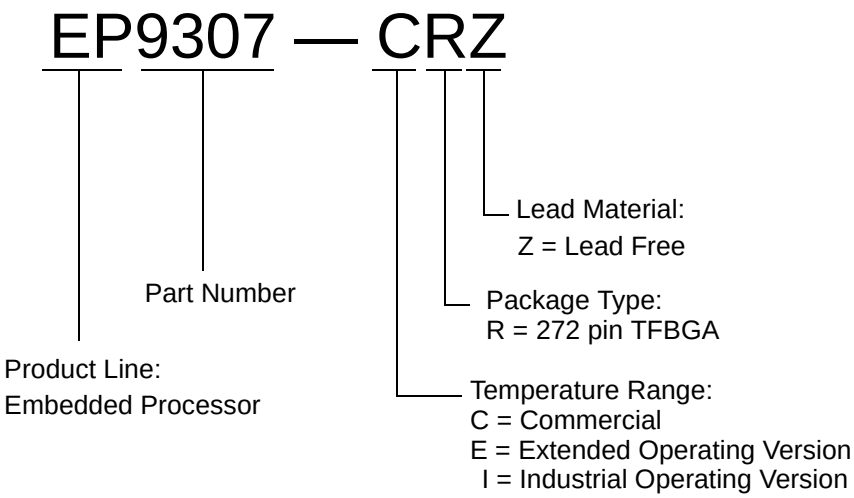
Table T. Pin Multiplex Usage Information

Physical Pin Name	Description	Multiplex signal name
COL[7:0]	GPIO	GPIO Port D[7:0]
ROW[7:0]	GPIO	GPIO Port C[7:0]
EGPIO[0]	Ring Indicator Input	RI
EGPIO[1]	1Hz clock monitor	CLK1HZ
EGPIO[2]	DMA request	DMARQ
EGPIO[3]	HDLC Clock	HDLCCLK1
EGPIO[4]	I2S Transmit Data 1	SDO1
EGPIO[5]	I2S Receive Data 1	SDI1
EGPIO[6]	I2S Transmit Data 2	SDO2
EGPIO[7]	DMA Request 0	DREQ0
EGPIO[8]	DMA Acknowledge 0	DACK0
EGPIO[9]	DMA EOT 0	DEOT0
EGPIO[10]	DMA Request 1	DREQ1
EGPIO[11]	DMA Acknowledge 1	DACK1
EGPIO[12]	DMA EOT 1	DEOT1
EGPIO[13]	I2S Receive Data 2	SDI2
EGPIO[15]	Device active / present	DASP
ABITCLK	I2S Serial clock	SCLK
ASYNC	I2S Frame Clock	LRCK
ASDO	I2S Transmit Data 0	SDO0
ASDI	I2S Receive Data 0	SDI0
ARSTn	I2S Master clock	MCLK
SCLK1	I2S Serial clock	SCLK
SFRM1	I2S Frame Clock	LRCK
SSPTX1	I2S Transmit Data 0	SDO0
SSPRX1	I2S Receive Data 0	SDI0

ORDERING INFORMATION

The order numbers for the device are:

EP9307-CRZ	0°C to +70°C	272 pin TFBGA	Lead Free
EP9307-IRZ	-40°C to +85°C	272 pin TFBGA	Lead Free



Note: Go to the Cirrus Logic Internet site at http://www.cirrus.com to find contact information for your local sales representative.