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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 8x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84763vlh

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except RESETB pin)

- LQFP packages:
  - 64-pin
  - 80-pin
  - 100-pin

Table of Contents

Table 1. 56F844x/5x/7x Family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
PWMB with input capture: Standard channels	1x 12	1x7	1x 12	1x7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12-bit DAC	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	2	2	2	2	2	3	2	3	2	2	2	2	2	2
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total includes FlexNVM and assumes no FlexNVM is used with FlexRAM for EEPROM.

1.2 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, effectively supporting DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers corresponding to the R0, R1, R2, R3, R4, R5, N, N3, and M01 address registers
- Instruction set supporting both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 100 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 144 KW program/data flash memory, including FlexNVM
  - Up to 16 KW dual port data/program RAM

- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block Diagrams

The 56800EX core is based on a modified dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800EX system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

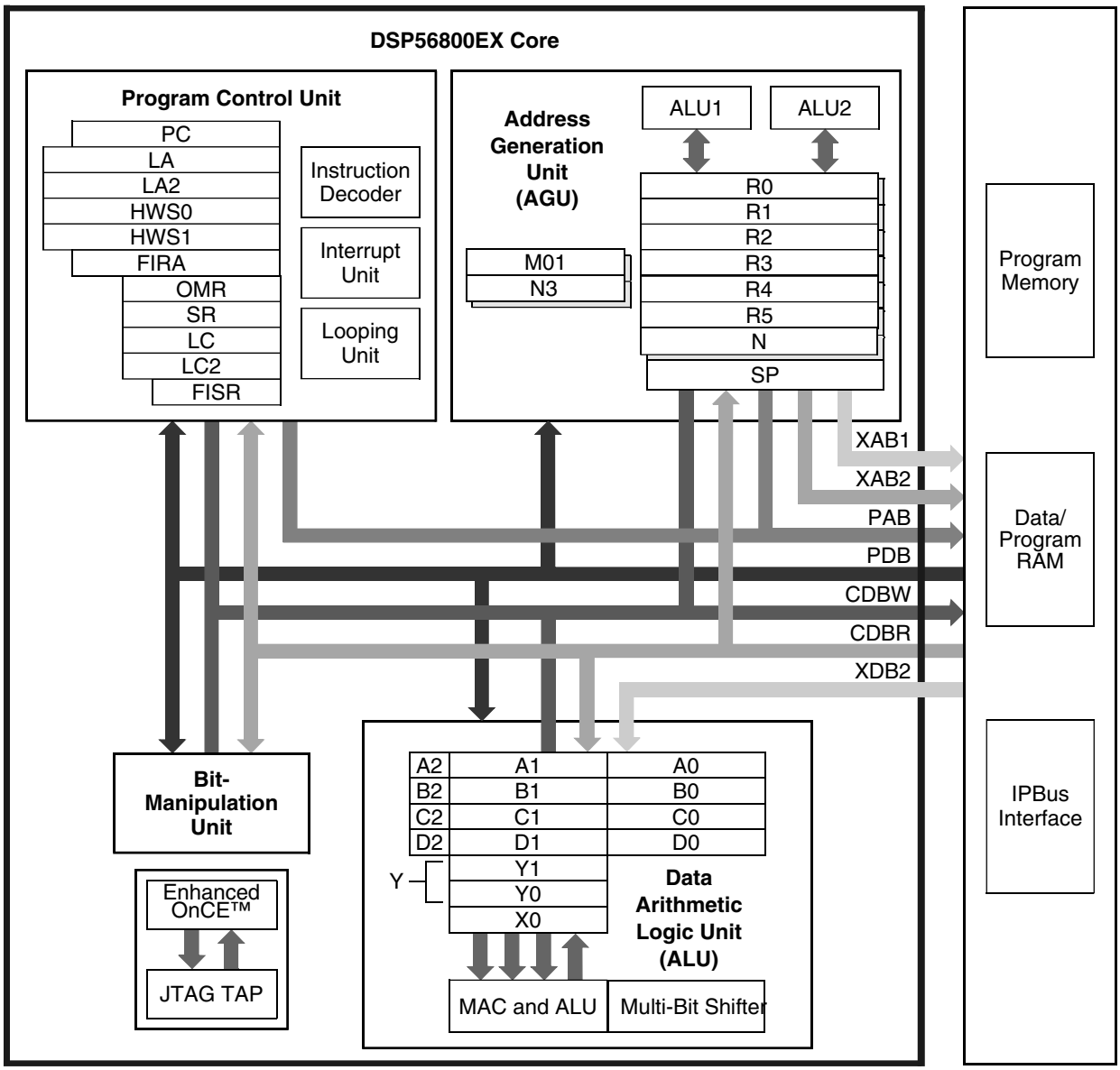


Figure 1. 56800EX Basic Block Diagram

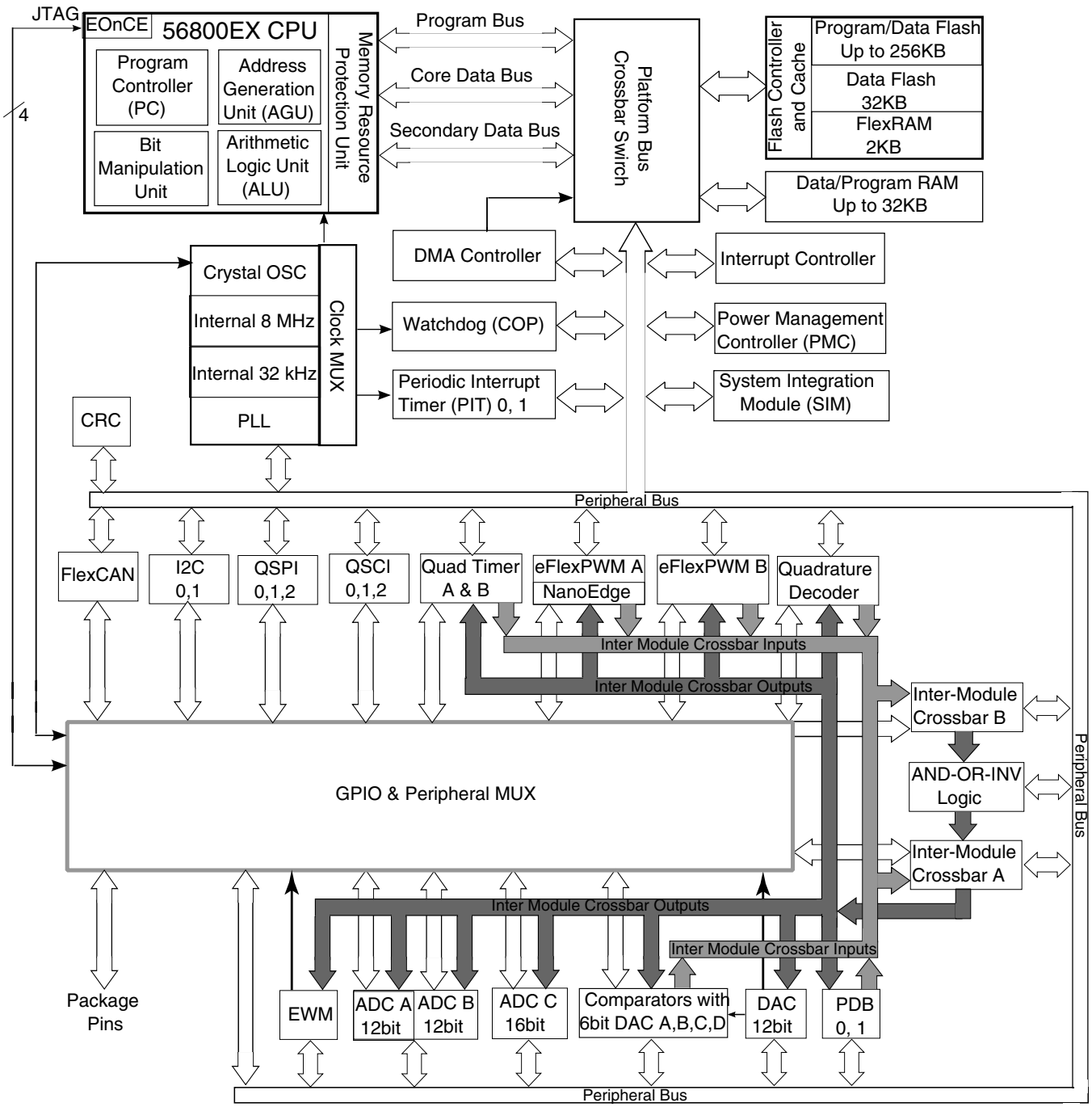
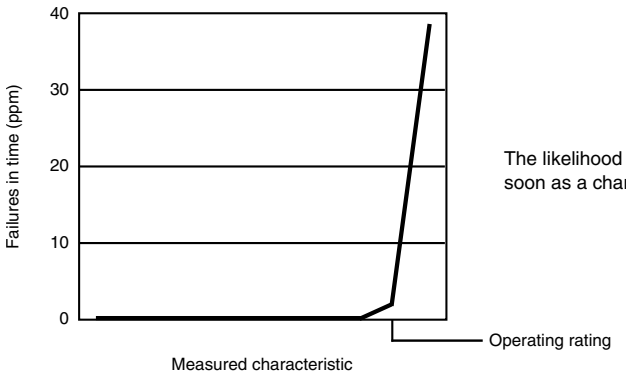


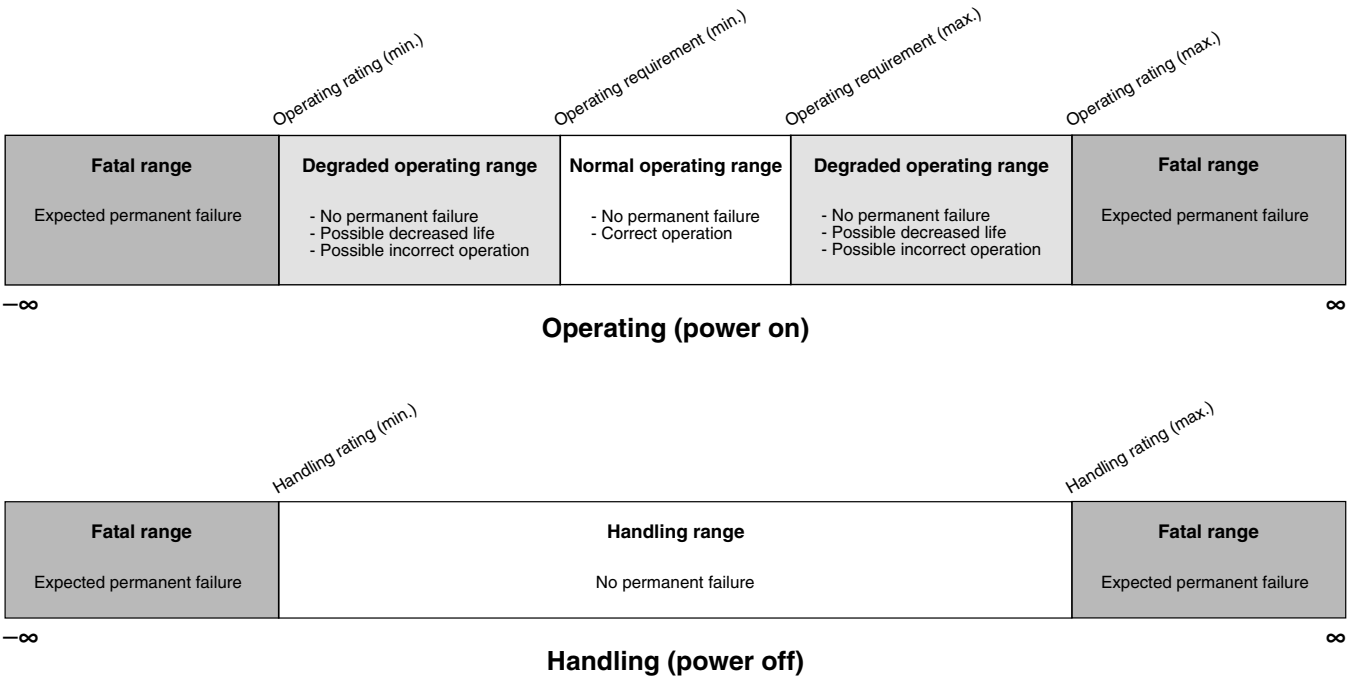
Figure 2. System Diagram

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

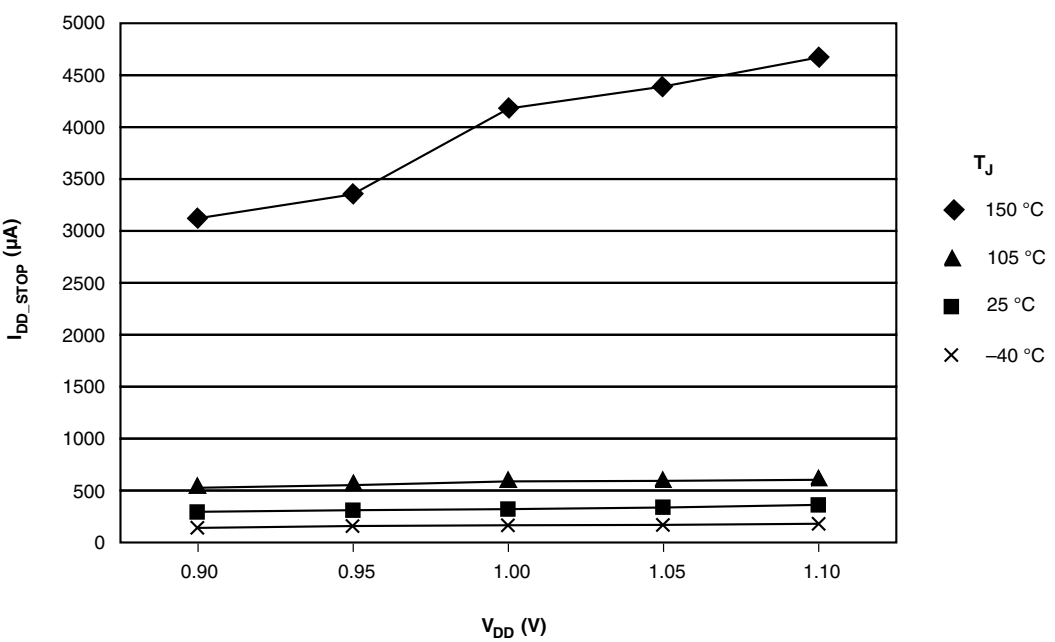
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

6 Ratings

6.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

- Pin Group 3: ADC and Comparator Analog Inputs
- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output

2. ADC (Cyclic) specifications are not guaranteed when V_{DDA} is below 3.0 V.
3. Total chip source or sink current cannot exceed 75 mA.
4. Contiguous pin DC injection current of regional limit—includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 6. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

7.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

Table 7. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High	I_{IH}	Pin Group 1	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
pull-up enabled or disabled		Pin Group 2					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	—	50	kΩ	—
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	—	50	kΩ	—

Table continues on the next page...

Table 7. DC Electrical Characteristics at Recommended Operating Conditions (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ ll C_{LD} = 400 pf
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

7.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 8. Reset, Stop, Wait, and Interrupt Timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.

NOTE

In the Table 8, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 100 MHz, T = 10 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG Timing

Table 14. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/16	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

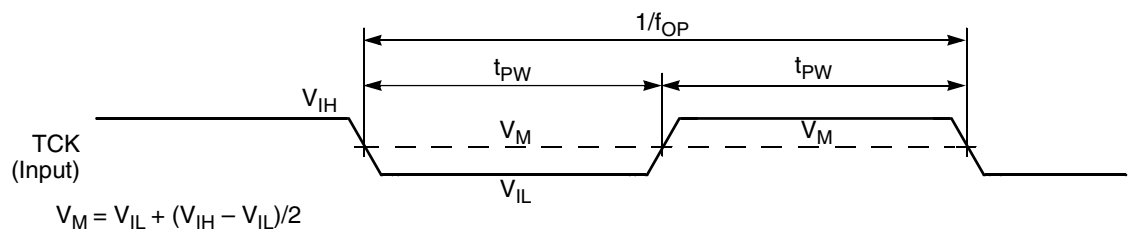


Figure 5. Test Clock Input Timing Diagram

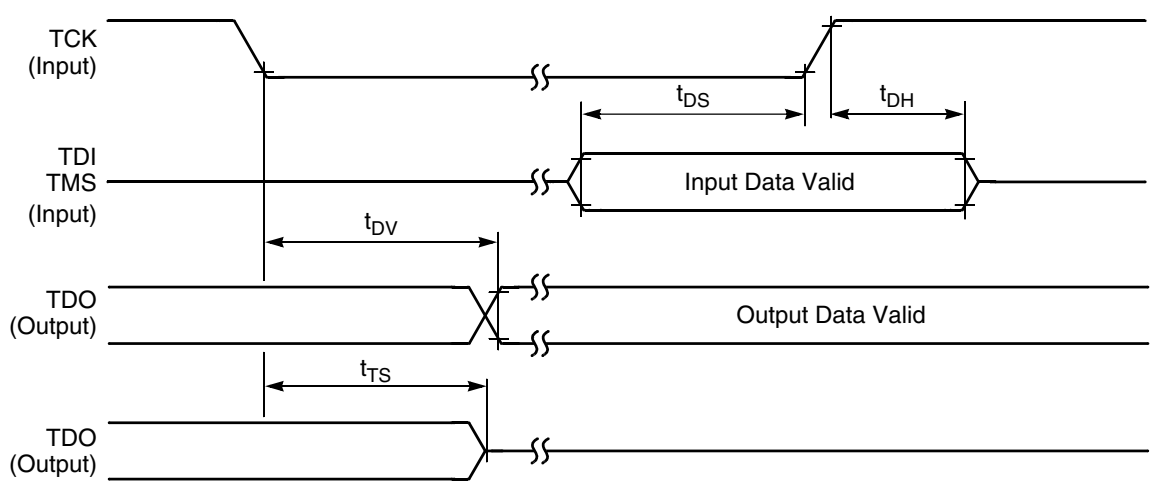


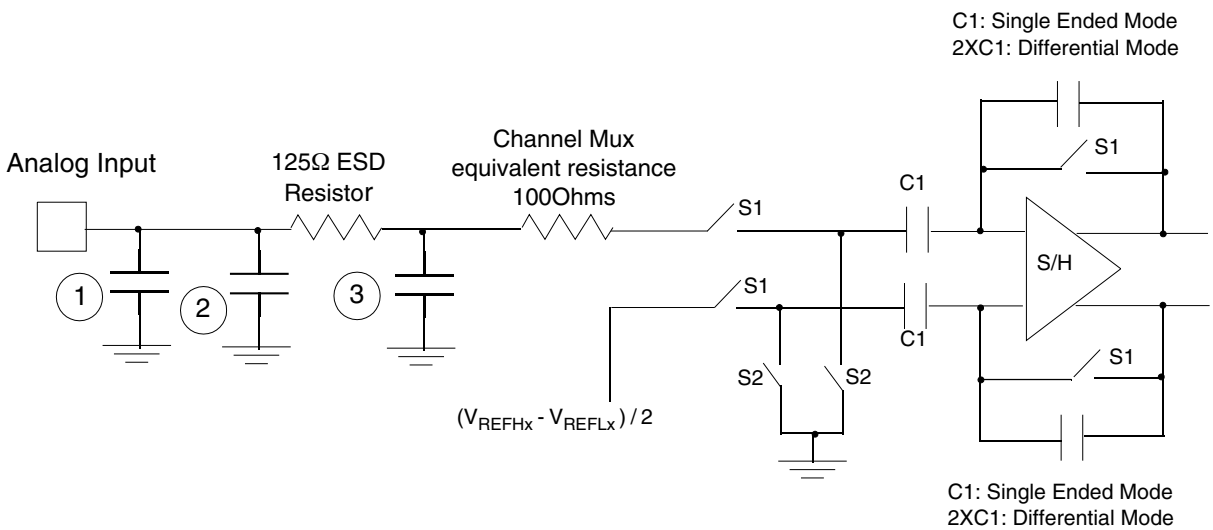
Figure 6. Test Access Port Timing Diagram

4. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$.
5. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting
6. Offset over the conversion range of 0025 to 4080
7. Measured converting a 1 kHz input Full Scale sine wave
8. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC

8.5.1.1 Equivalent Circuit for ADC Inputs

The following figure illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100ohm + 125ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time of 4.8pF
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

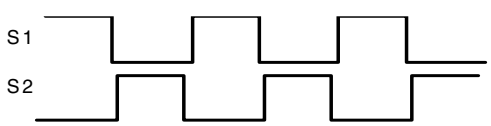


Figure 9. Equivalent Circuit for A/D Loading

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)		250		ns
	Analog comparator initialization delay[3]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
	6-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	V_{DDA}	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[4]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Signal swing is 100 mV
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
4. 1 LSB = $V_{reference}$/64

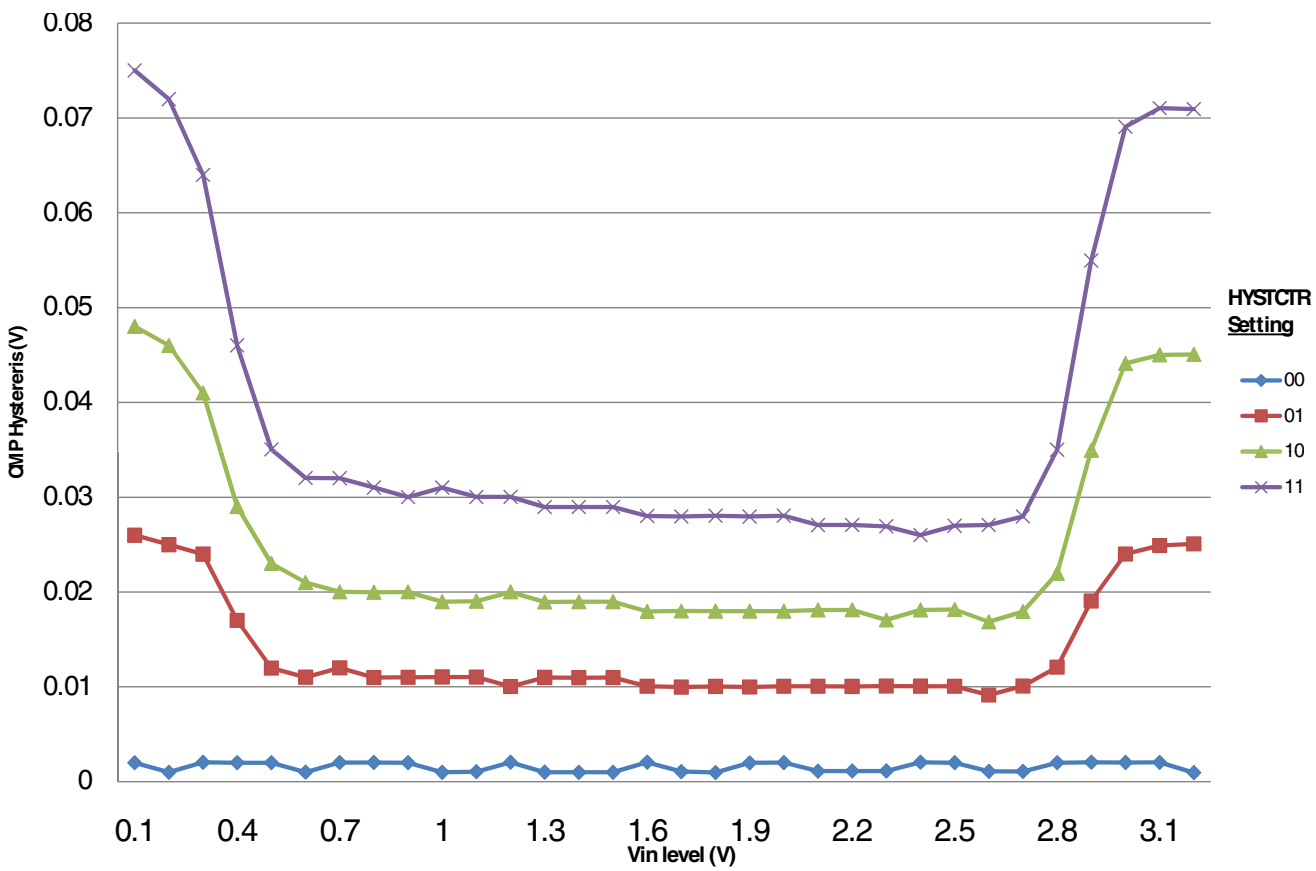


Figure 12. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

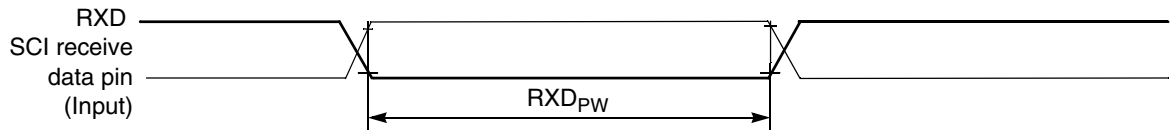


Figure 19. RXD Pulse Width

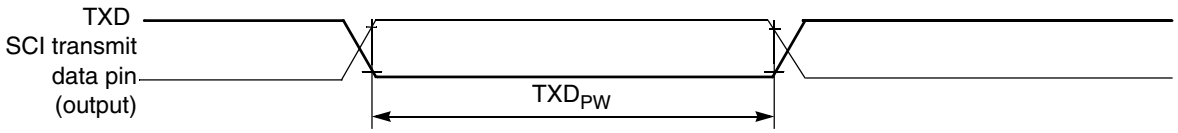


Figure 20. TXD Pulse Width

8.7.3 Freescale's Scalable Controller Area Network (FlexCAN)

Table 34. FlexCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	2	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

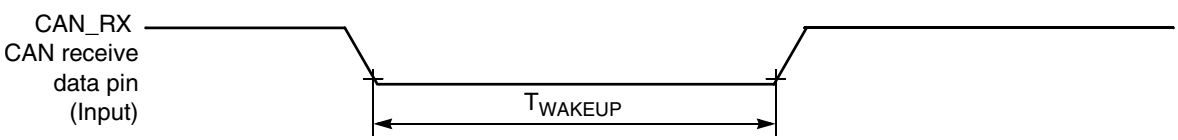


Figure 21. Bus Wake-up Detection

8.7.4 Inter-Integrated Circuit Interface (I^2C) Timing

Table 35. I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns

Table continues on the next page...

11.1 Signal Multiplexing and Pin Assignments

This section shows the signals available on each package pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

The RESETB pin is a 3.3 V pin only.

NOTE

If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.

NOTE

PWMB signals—including PWMB_2A, PWMB_2B, and PWMB_3X—are not available on the 64 LQFP package.

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	TCK	TCK	GPIOD2			
2	2	2	RESETB	RESETB	GPIOD4			
3	3	3	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	4	4	GPIOC1	GPIOC1	XTAL			
5	5	5	GPIOC2	GPIOC2	TXD0	TB0	XB_IN2	CLKO0
6	6	6	GPIOF8	GPIOF8	RXD0	TB1	CMPD_O	
7	—	—	VDD	VDD				
8	—	—	VSS	VSS				
9	7	—	GPIOD6	GPIOD6	TXD2	XB_IN4	XB_OUT8	
10	8	—	GPIOD5	GPIOD5	RXD2	XB_IN5	XB_OUT9	
11	9	7	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
12	10	8	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN8	EWM_OUT_B
13	—	—	GPIOA10	GPIOA10	ANC18&CMPD_IN3			
14	—	—	GPIOA9	GPIOA9	ANC17&CMPD_IN2			
15	11	—	VSS	VSS				
16	12	—	VCAP	VCAP				
17	13	9	GPIOA7	GPIOA7	ANA7&ANC11			
18	—	—	GPIOA8	GPIOA8	ANC16&CMPD_IN1			
19	14	10	GPIOA6	GPIOA6	ANA6&ANC10			
20	15	11	GPIOA5	GPIOA5	ANA5&ANC9			
21	16	12	GPIOA4	GPIOA4	ANA4&ANC8&CMPD_IN0			
22	17	13	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
23	18	14	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
24	19	15	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
64	—	—	GPIOG8	GPIOG8	PWMB_0X	PWMA_0X	TA2	XB_OUT10
65	—	—	GPIOG9	GPIOG9	PWMB_1X	PWMA_1X	TA3	XB_OUT11
66	53	43	VSS	VSS				
67	54	44	VDD	VDD				
68	55	45	GPIOE0	GPIOE0	PWMA_0B			
69	56	46	GPIOE1	GPIOE1	PWMA_0A			
70	57	—	GPIOG2	GPIOG2	PWMB_0B	XB_OUT4		
71	58	—	GPIOG3	GPIOG3	PWMB_0A	XB_OUT5		
72	—	—	GPIOE8	GPIOE8	PWMB_2B	PWMA_FAULT0		
73	—	—	GPIOE9	GPIOE9	PWMB_2A	PWMA_FAULT1		
74	59	47	GPIOE2	GPIOE2	PWMA_1B			
75	60	48	GPIOE3	GPIOE3	PWMA_1A			
76	61	49	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
77	62	50	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
78	63	—	GPIOG0	GPIOG0	PWMB_1B	XB_OUT6		
79	64	—	GPIOG1	GPIOG1	PWMB_1A	XB_OUT7		
80	—	—	GPIOG4	GPIOG4	PWMB_3B	PWMA_FAULT2		
81	—	—	GPIOG5	GPIOG5	PWMB_3A	PWMA_FAULT3		
82	65	51	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		
83	66	52	GPIOE5	GPIOE5	PWMA_2A	XB_IN3		
84	67	53	GPIOE6	GPIOE6	PWMA_3B	XB_IN4	PWMB_2B	
85	68	54	GPIOE7	GPIOE7	PWMA_3A	XB_IN5	PWMB_2A	
86	69	—	GPIOG6	GPIOG6	PWMA_FAULT4	PWMB_FAULT4	TB2	XB_OUT8
87	70	55	GPIOC14	GPIOC14	SDA0	XB_OUT4		
88	71	56	GPIOC15	GPIOC15	SCL0	XB_OUT5		
89	—	—	GPIOF12	GPIOF12	MISO1	PWMB_FAULT2		
90	—	—	GPIOF13	GPIOF13	MOSI1	PWMB_FAULT1		
91	—	—	GPIOF14	GPIOF14	SCLK1	PWMB_FAULT0		
92	72	—	GPIOG7	GPIOG7	PWMA_FAULT5	PWMB_FAULT5	XB_OUT9	
93	73	57	VCAP	VCAP				
94	74	58	GPIOF6	GPIOF6	TB2	PWMA_3X	PWMB_3X	XB_IN2
95	75	59	GPIOF7	GPIOF7	TB3	CMPC_O	SS1_B	XB_IN3
96	76	60	VDD	VDD				
97	77	61	VSS	VSS				
98	78	62	TDO	TDO	GPIOD1			
99	79	63	TMS	TMS	GPIOD3			
100	80	64	TDI	TDI	GPIOD0			

NOTE

The RESETB pin is a 3.3 V pin only.

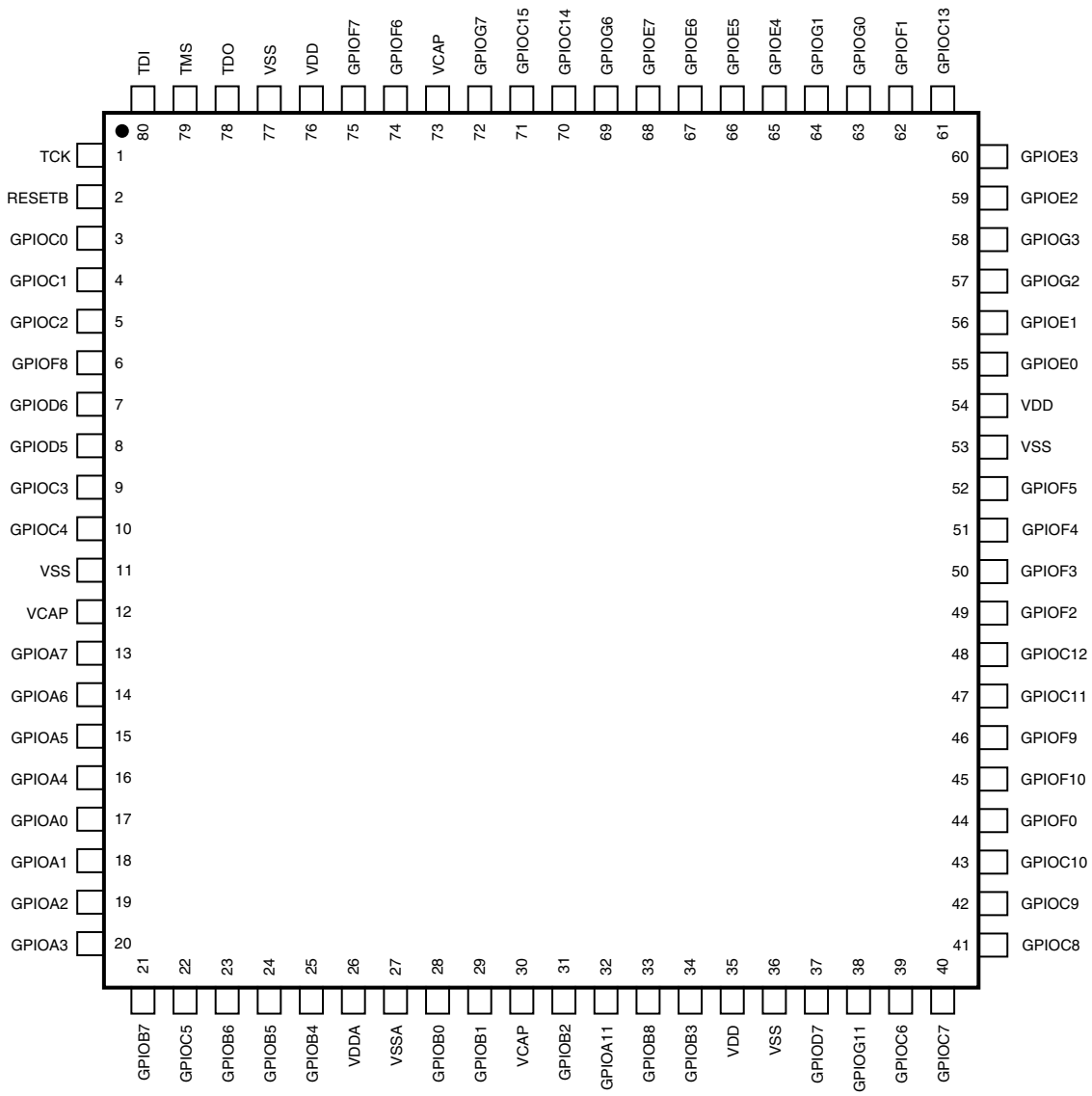


Figure 24. 80-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product Documentation

The documents listed in Table 36 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at http://www.freescale.com.

Table 36. Device Documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F847xx Reference Manual	Detailed functional description and programming model	MC56F847XXRM
Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the DSC family of devices	
MC56F847xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F847XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

13 Revision History

The following table summarizes changes to this document since the release of the previous version.