Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 8x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84763vlhr

- Support for simultaneous and software triggering conversions
- Support for multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, Comparators, Quad Timers, eFlexPWMs, PDBs, EWM, Quadrature Decoder, and select I/O pins
- User-defined input/output pins for all modules connected to crossbar
- DMA request and interrupt generation from crossbar
- Write-once protection for all registers
- AND-OR-INVERT function that provides a universal Boolean function generator using a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high speed mode and low speed mode
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising edge, falling edge, or toggle of comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms including square, triangle, and sawtooth waveforms for applications such as slope compensation
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally off chip

- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block Diagrams

The 56800EX core is based on a modified dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800EX system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: VSS = VSSA = 0 V, VDD = VDDA = 3.0 V to 3.6 V, CL ≤ 50 pF, f_{OP} = 100 MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

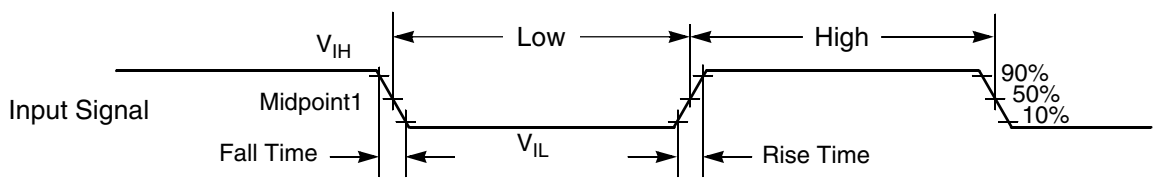


Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

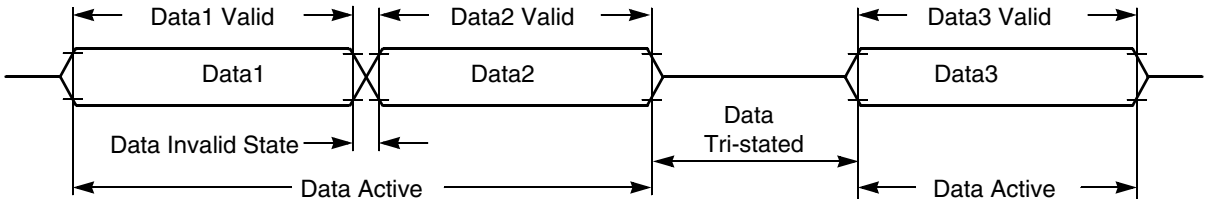


Figure 4. Signal States

7.3 Nonswitching electrical specifications

7.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 5. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		3.0		V_{DDA}	V
ADC (SAR) Reference Voltage High	V_{REFHC}		2.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -2 -9	 mA
Output Source Current Low (at V_{OL} max.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 2 9	 mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	40	49	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	44	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	34	43	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	24	35	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	12	17	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG Timing

Table 14. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/16	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

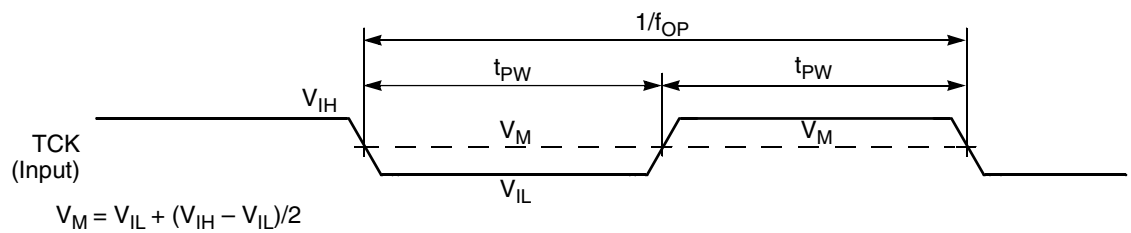


Figure 5. Test Clock Input Timing Diagram

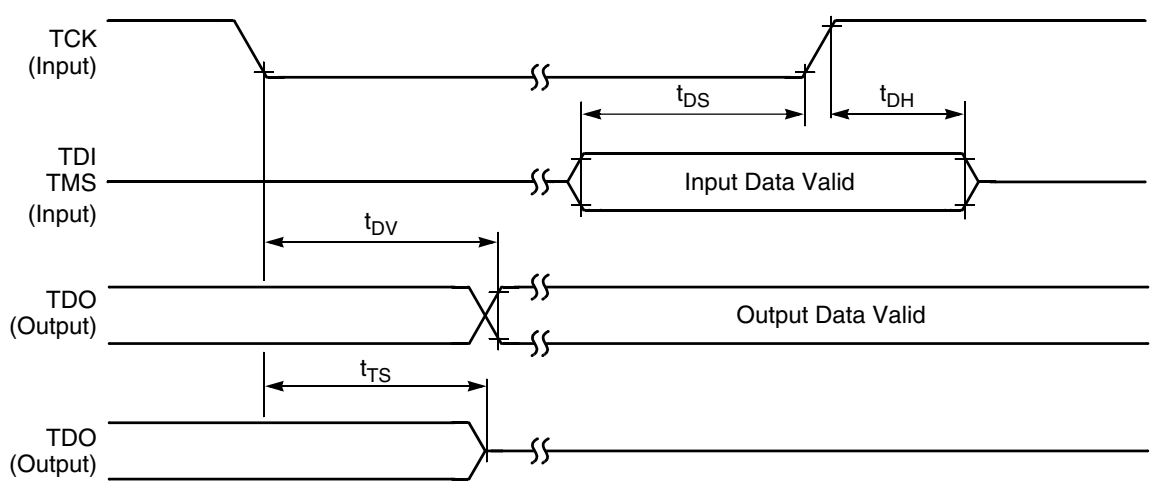


Figure 6. Test Access Port Timing Diagram

8.2 System modules

8.2.1 Voltage Regulator Specifications

The regulator supplies approximately 1.2 V to the MC56F84xxx's core logic. This regulator requires an external 2.2 µF capacitor on each V_{CAP} pin for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 15.

Table 15. Regulator 1.2 V Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600		mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 16. Bandgap Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

8.3 Clock modules

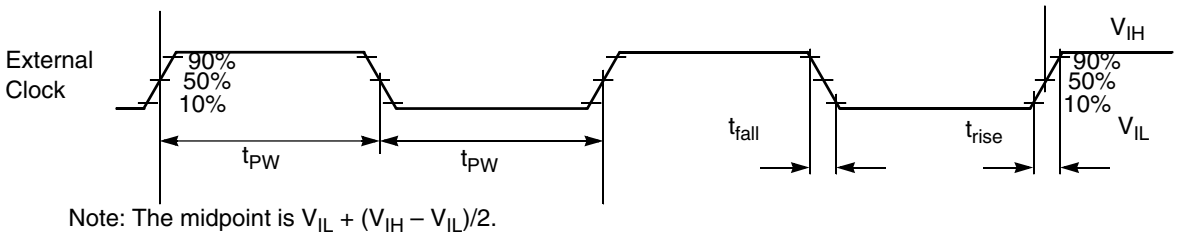
8.3.1 External Clock Operation Timing

Parameters listed are guaranteed by design.

Table 17. External Clock Operation Timing Requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	0.85VDD	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

1. See Figure 7 for detail on using the recommended connection of an external clock driver.
2. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 7. External Clock Timing

8.3.2 Phase Locked Loop Timing

Table 18. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	8	8	16	MHz
PLL output frequency[2]	f_{op}	240	—	400	MHz
PLL lock time[3]	t_{plls}	35.5		73.2	µs
Allowed Duty Cycle of input reference	t_{dc}	40	50	60	%

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
2. The frequency of the core system clock cannot exceed 100 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
3. This is the time required after the PLL is enabled to ensure reliable operation.

8.3.3 External Crystal or Resonator Requirement

Table 19. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

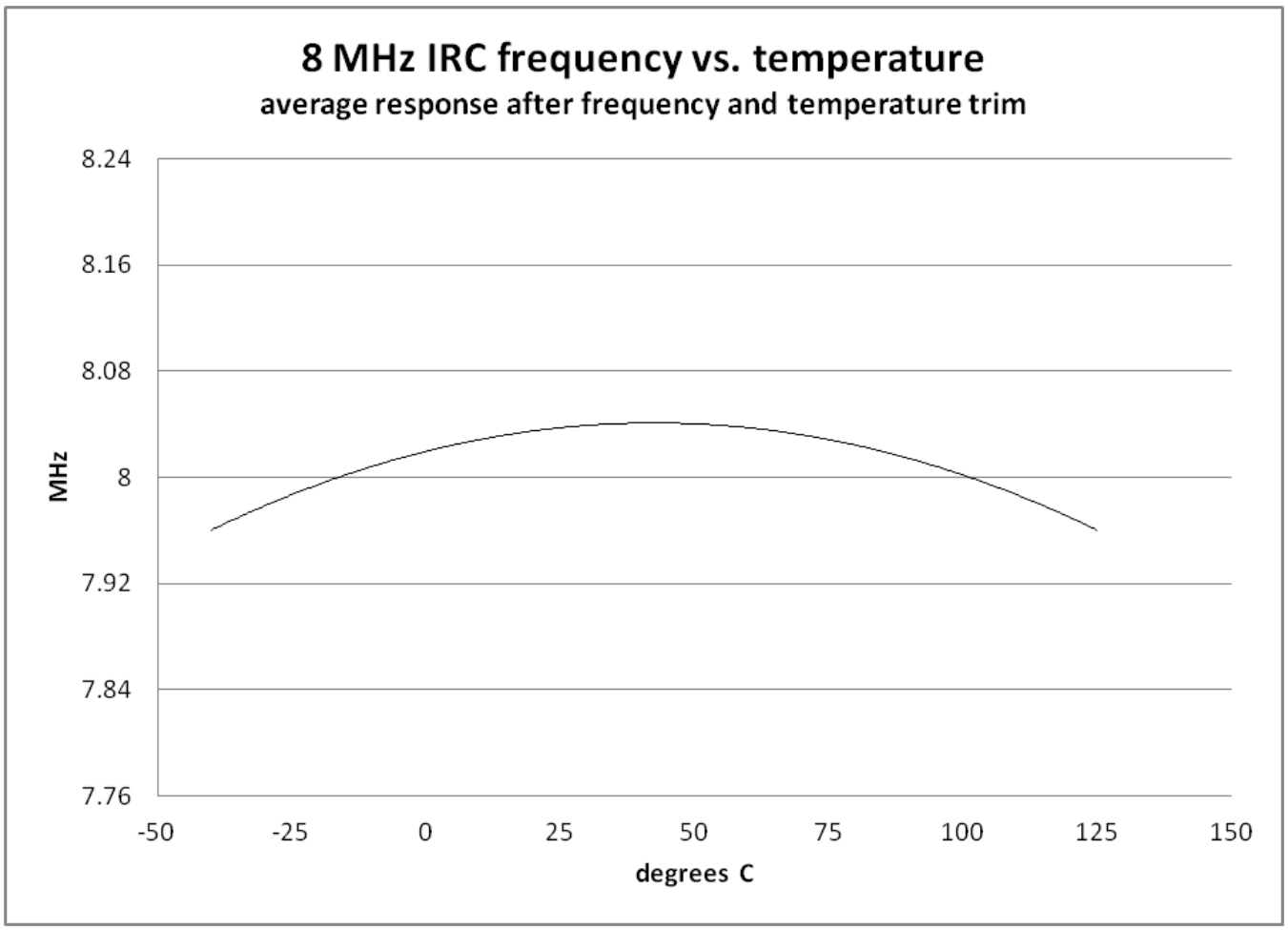


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	

Table continues on the next page...

Table 21. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (data flash sector)	—	—	60	µs	1
$t_{rd1sec2k}$	Read 1s Section execution time (program flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512p}$	• 512 B program flash	—	2.4	—	ms	
$t_{pgmsec512d}$	• 512 B data flash	—	4.7	—	ms	
$t_{pgmsec1kp}$	• 1 KB program flash	—	4.7	—	ms	
$t_{pgmsec1kd}$	• 1 KB data flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	175	1500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	

Table continues on the next page...

8.5.2 16-bit SAR ADC electrical specifications

8.5.2.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} - V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-/10-/12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	7
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1ns.
6. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

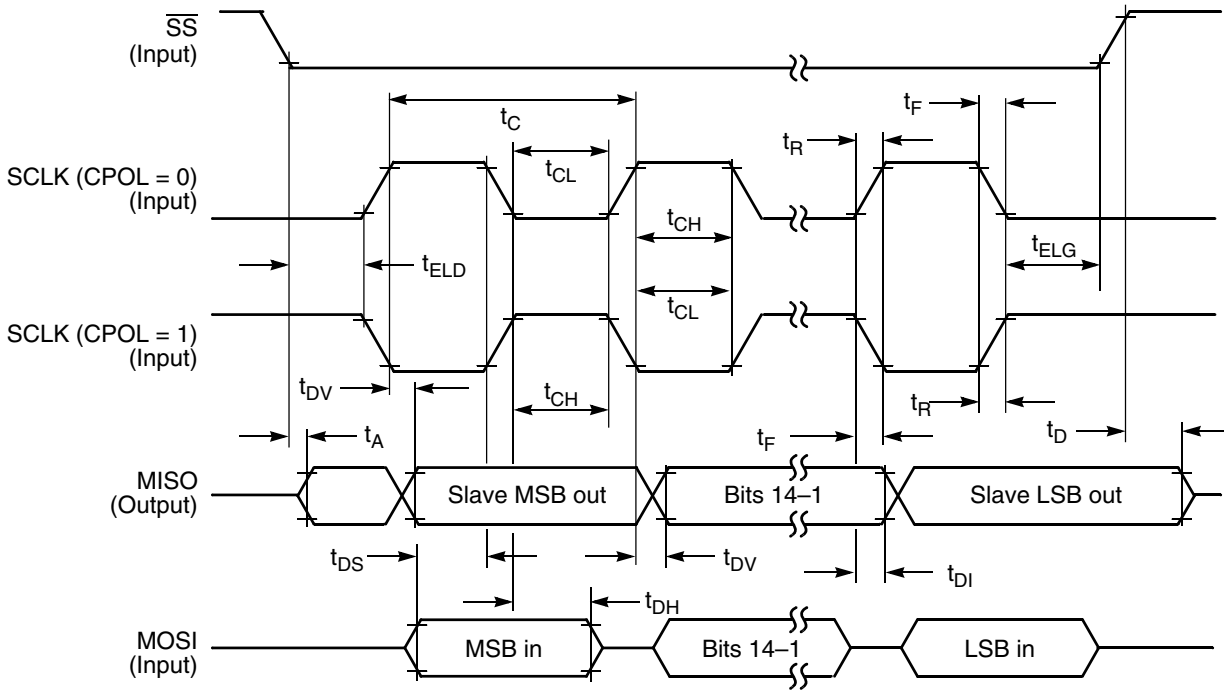


Figure 18. SPI Slave Timing (CPHA = 1)

8.7.2 Queued Serial Communication Interface (SCI) Timing

Parameters listed are guaranteed by design.

Table 33. SCI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbps	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 19
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 20
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max. 200 MHz depending on part number) or 2x bus clock (max. 200 MHz) for the devices.

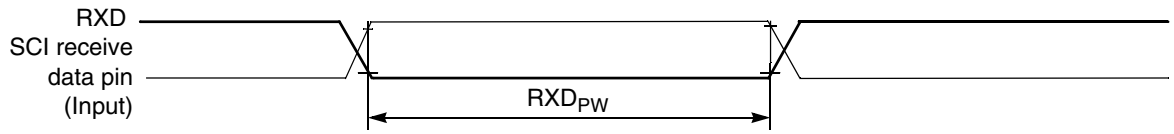


Figure 19. RXD Pulse Width

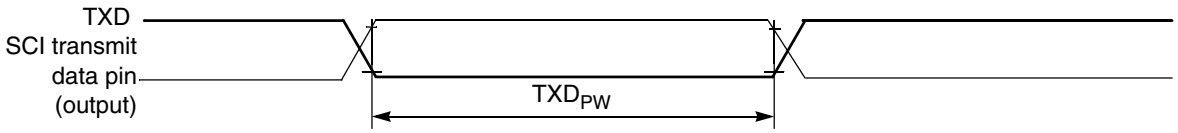


Figure 20. TXD Pulse Width

8.7.3 Freescale's Scalable Controller Area Network (FlexCAN)

Table 34. FlexCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	2	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

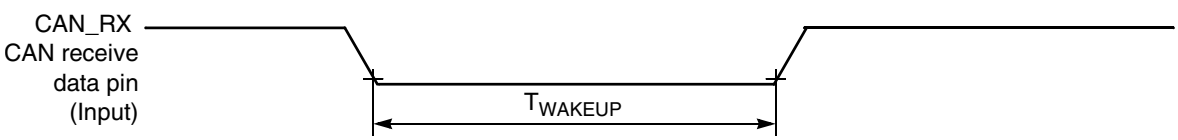


Figure 21. Bus Wake-up Detection

8.7.4 Inter-Integrated Circuit Interface (I^2C) Timing

Table 35. I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns

Table continues on the next page...

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over

- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23174W
100-pin LQFP	98ASS23308W

11 Pinout

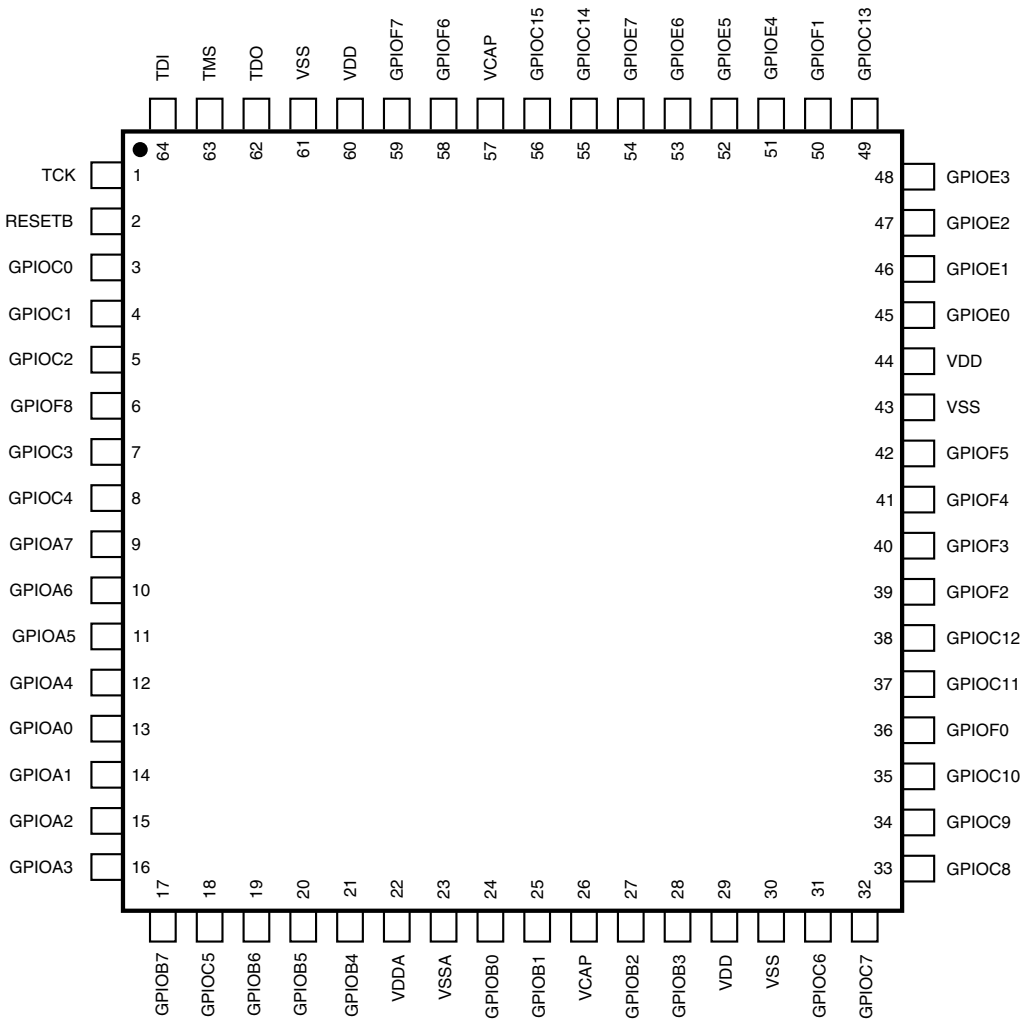


Figure 25. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product Documentation

The documents listed in Table 36 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at http://www.freescale.com.

Table 36. Device Documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F847xx Reference Manual	Detailed functional description and programming model	MC56F847XXRM
Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the DSC family of devices	
MC56F847xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F847XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev.	Date	Substantial Changes
3	08/2012	In various locations: Clarified that the RESETB pin is a 3.3 V pin only
		MC56F844x/5x/7x Product Family: Clarified that DAC table row applies to 12-bit DAC
		Voltage and current operating ratings: Added rows for RESET input voltage range and RESET output voltage range
		Voltage and current operating requirements: Added row for RESET voltage high, and added new final footnote
		Voltage and current operating behaviors: For Digital Input Current High, created separate sub-rows for Pin Groups 1 and 2
		Power mode transition operating behaviors: Updated row for RESET deassertion to First Address Fetch
		Power consumption operating behaviors: Replaced all TBD values, and updated Typical at 3.3 V I_{DDA} value for WAIT mode
		EMC radiated emissions operating behaviors: Removed this section
		Thermal attributes: Updated values for 100 LQFP
		JTAG Timing: Changed divider value of Max for TCK frequency of operation
		Relaxation Oscillator Timing: Replaced all TBDs, and removed Standby Mode specification for 8 MHz Frequency Variation
		Peripheral operating requirements and behaviors: Updated Flash timing specifications and added Flash high voltage current behaviors
		16-bit ADC electrical characteristics: Updated DNL information about Max value for 16-bit modes and 12-bit modes, and updated INL information about Max value for 16-bit modes
		Signal Multiplexing and Pin Assignments: Added note about GPIOC1, added JTAG signals to table and diagrams, and changed "SCK" signal names to "SCLK"

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: MC56F847XX
Rev. 3, 08/2012