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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 10x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84766vlk

- Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
- Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Support for nested interrupt: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- PWM module contains four identical submodules with up to three outputs per submodule
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWMA with NanoEdge high resolution
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - 312 ps PWM frequency and duty-cycle resolution when NanoEdge functionality is enabled
- PWMB with supporting accumulative fractional clock calculation
  - Accumulative fractional clock calculation improves the resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - Equivalent to 312 ps PWM frequency and duty-cycle resolution on average

1.6.6 Quad Timer

- Four 16-bit up/down counters with programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.6.7 Queued Serial Communications Interface (QSCI) Modules

- Operating clock up to two times CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

1.6.8 Queued Serial Peripheral Interface (QSPI) Modules

- Maximum 25 Mbps baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) Modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation

- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter

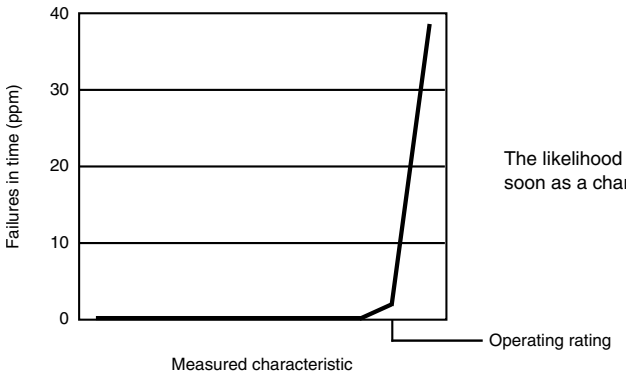
1.6.10 Flex Controller Area Network (FlexCAN) Module

- Clock source from PLL or XOSC/CLKIN
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbps
- Support for remote frames
- Sixteen Message Buffers, each configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Global network time, synchronized by a specific message
- Low power modes, with programmable wakeup on bus activity

1.6.11 Computer Operating Properly (COP) Watchdog

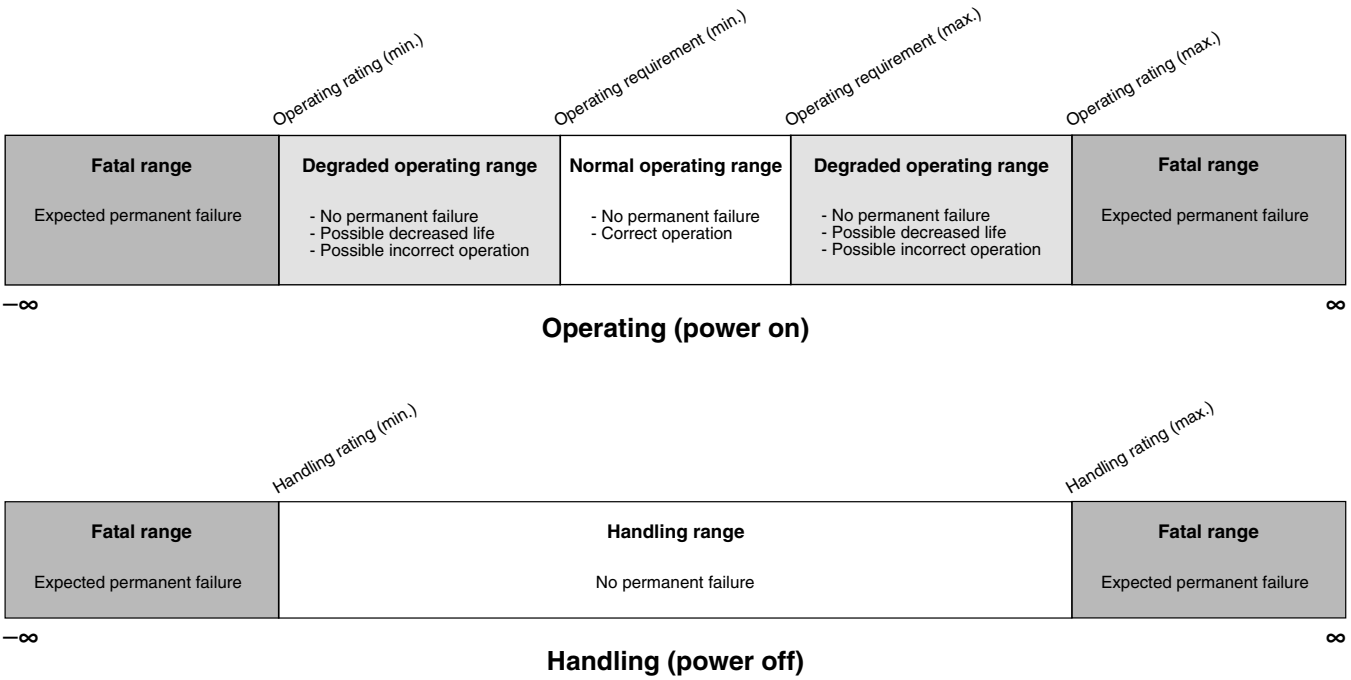
- Programmable timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

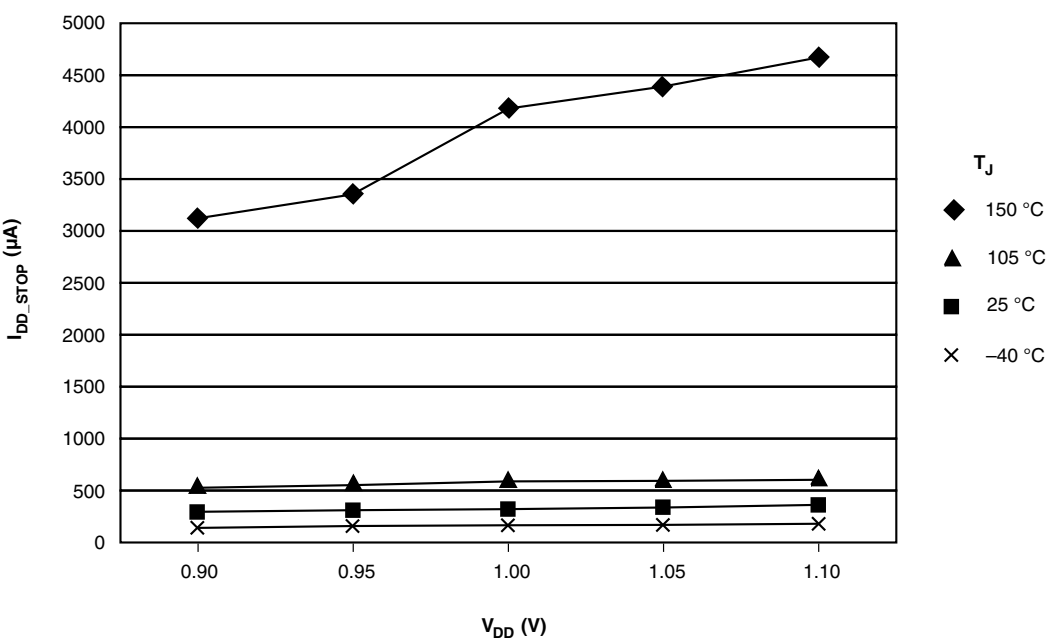
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

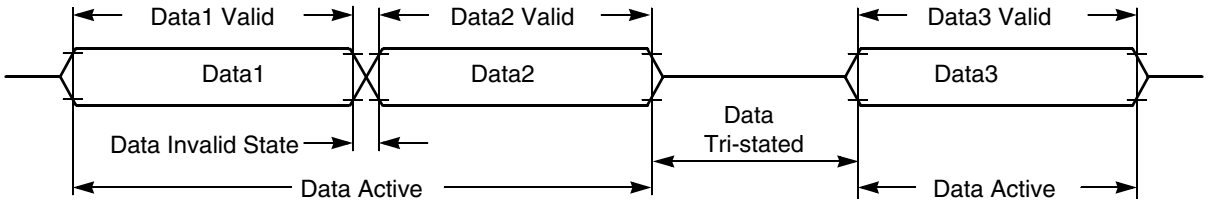


Figure 4. Signal States

7.3 Nonswitching electrical specifications

7.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 5. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		3.0		V_{DDA}	V
ADC (SAR) Reference Voltage High	V_{REFHC}		2.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -2 -9	 mA
Output Source Current Low (at V_{OL} max.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 2 9	 mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$

Table 7. DC Electrical Characteristics at Recommended Operating Conditions (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ ll C_{LD} = 400 pf
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

7.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 8. Reset, Stop, Wait, and Interrupt Timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.

NOTE

In the Table 8, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 100 MHz, T = 10 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG Timing

Table 14. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/16	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

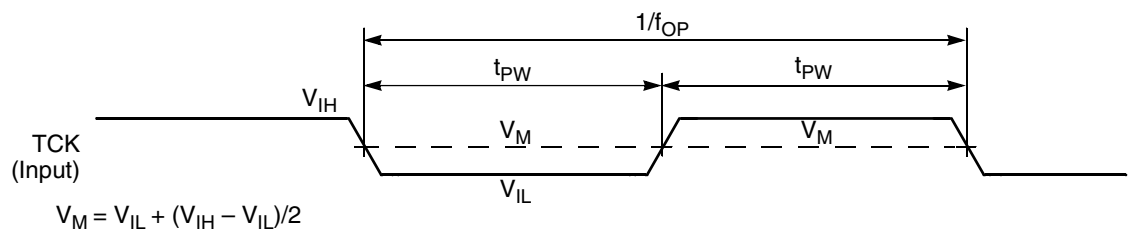


Figure 5. Test Clock Input Timing Diagram

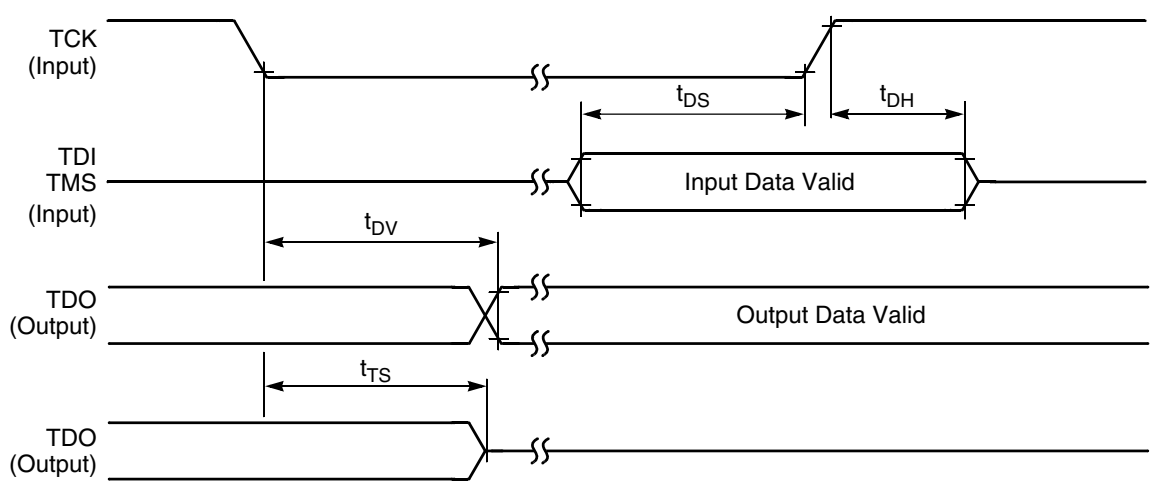


Figure 6. Test Access Port Timing Diagram

Table 21. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (data flash sector)	—	—	60	µs	1
$t_{rd1sec2k}$	Read 1s Section execution time (program flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512p}$	• 512 B program flash	—	2.4	—	ms	
$t_{pgmsec512d}$	• 512 B data flash	—	4.7	—	ms	
$t_{pgmsec1kp}$	• 1 KB program flash	—	4.7	—	ms	
$t_{pgmsec1kd}$	• 1 KB data flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	175	1500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	

Table continues on the next page...

8.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

8.5 Analog

8.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 25. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	V_{DDA}	2.7	3.3	3.6	V
Vrefh Supply Voltage[2]	Vrefhx	3.0		V_{DDA}	V
ADC Conversion Clock[3]	f_{ADCCLK}	0.6		20	MHz
Conversion Range	R_{AD}	V_{REFL}		V_{REFH}	V

Table continues on the next page...

7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.
8. System Clock = 4 MHz, ADC Clock = 2 MHz, AVG = Max, Long Sampling = Max

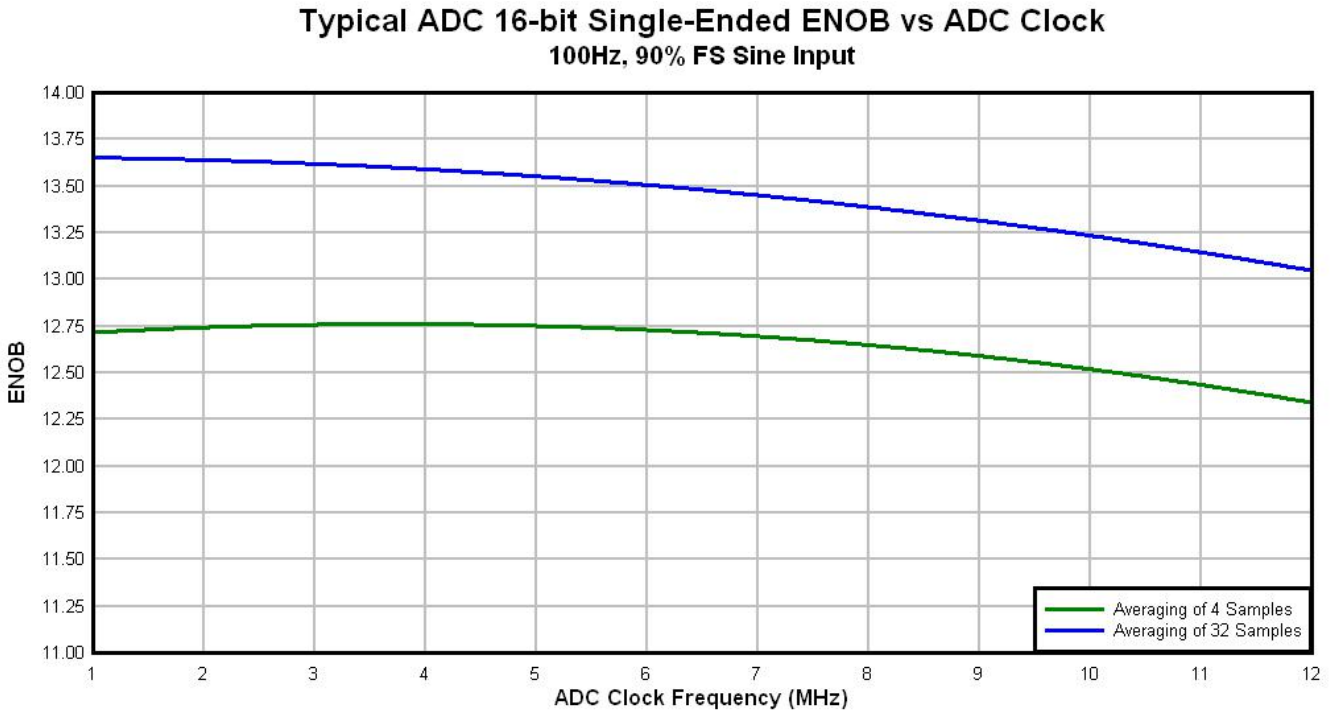


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

8.5.3 12-bit Digital-to-Analog Converter (DAC) Parameters

Table 28. DAC Parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pf		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 4	LSB[3]
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]

Table continues on the next page...

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Enable lead time	t_{ELD}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Enable lag time	t_{ELG}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Clock (SCK) high time	t_{CH}				Figure 15
Master		16.6	—	ns	Figure 16
Slave		16.6	—	ns	Figure 17
					Figure 18
Clock (SCK) low time	t_{CL}				Figure 18
Master		16.6	—	ns	
Slave		16.6	—	ns	
Data set-up time required for inputs	t_{DS}				Figure 15
Master		16.5	—	ns	Figure 16
Slave		1	—	ns	Figure 17
					Figure 18
Data hold time required for inputs	t_{DH}				Figure 15
Master		1	—	ns	Figure 16
Slave		3	—	ns	Figure 17
					Figure 18
Access time (time to data active from high-impedance state)	t_A				Figure 18
Slave		5	—	ns	
Disable time (hold time to high-impedance state)	t_D				Figure 18
Slave		5	—	ns	
Data valid for outputs	t_{DV}				Figure 15
Master		—	5	ns	Figure 16
Slave (after enable edge)		—	15	ns	Figure 17
					Figure 18
Data invalid	t_{DI}				Figure 15
Master		0	—	ns	Figure 16
Slave		0	—	ns	Figure 17
					Figure 18

Table continues on the next page...

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Rise time	t_R				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
					Figure 18
Fall time	t_F				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
					Figure 18

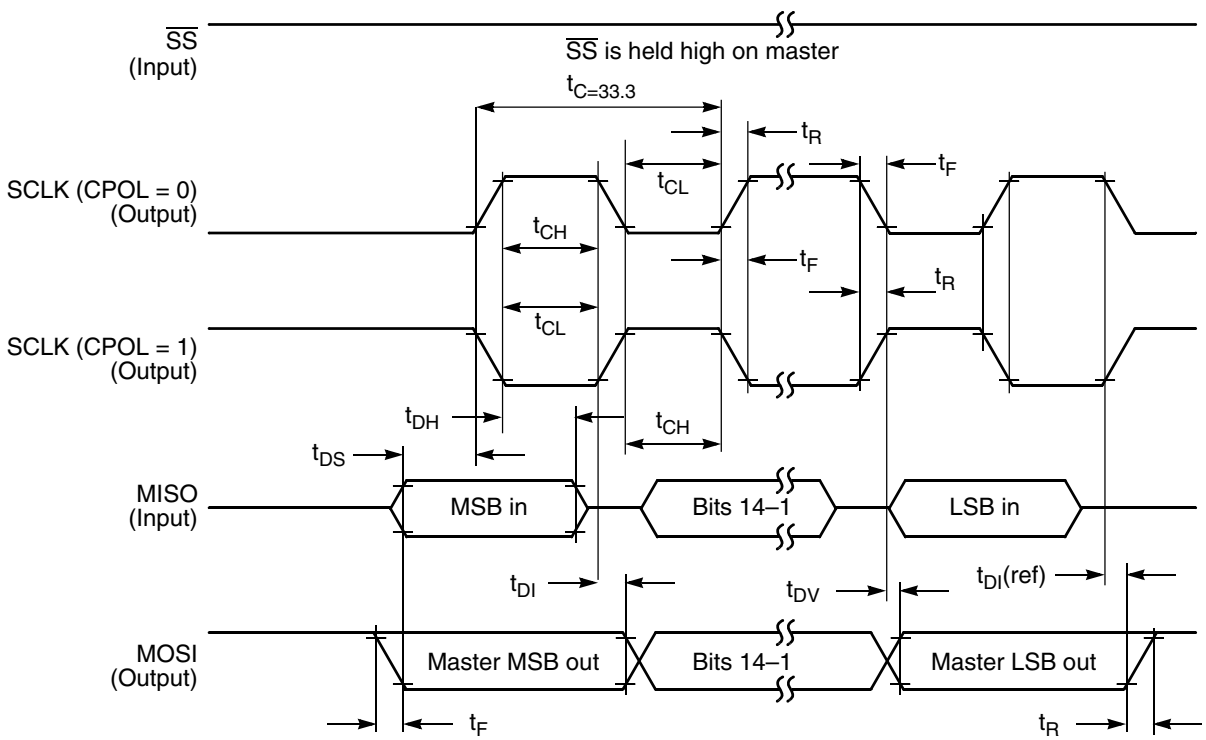


Figure 15. SPI Master Timing (CPHA = 0)

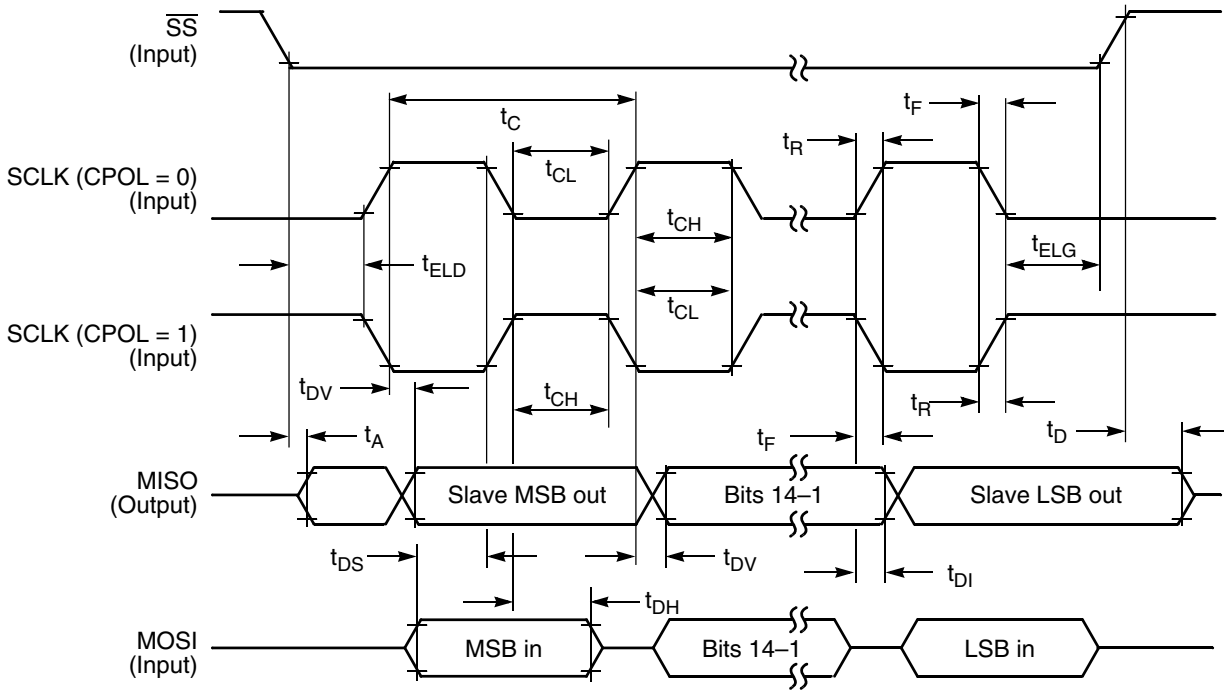


Figure 18. SPI Slave Timing (CPHA = 1)

8.7.2 Queued Serial Communication Interface (SCI) Timing

Parameters listed are guaranteed by design.

Table 33. SCI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbps	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 19
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 20
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max. 200 MHz depending on part number) or 2x bus clock (max. 200 MHz) for the devices.

Table 35. I ^{2}C Timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^{2}C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^{2}C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^{2}C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

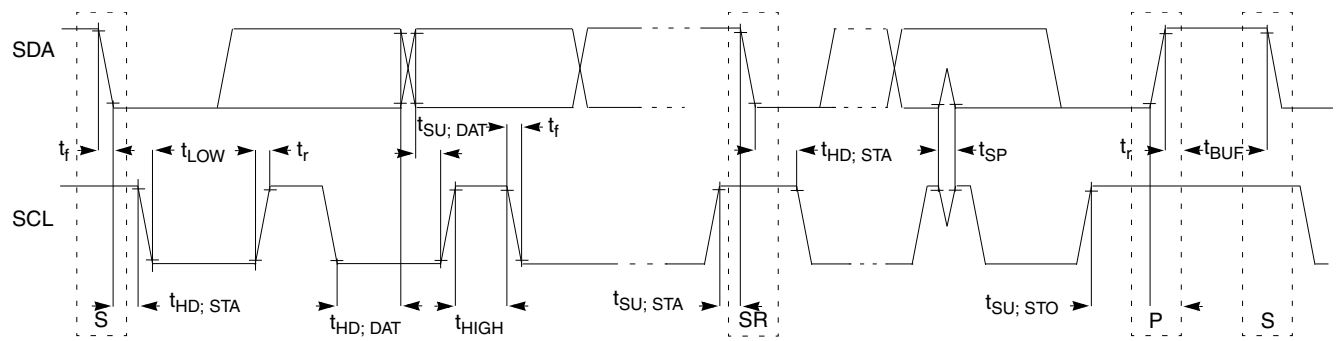


Figure 22. Timing Definition for Fast and Standard Mode Devices on the I^{2}C Bus

9 Design Considerations

9.1 Thermal Design Considerations

An estimation of the chip junction temperature, TJ, can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

11.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

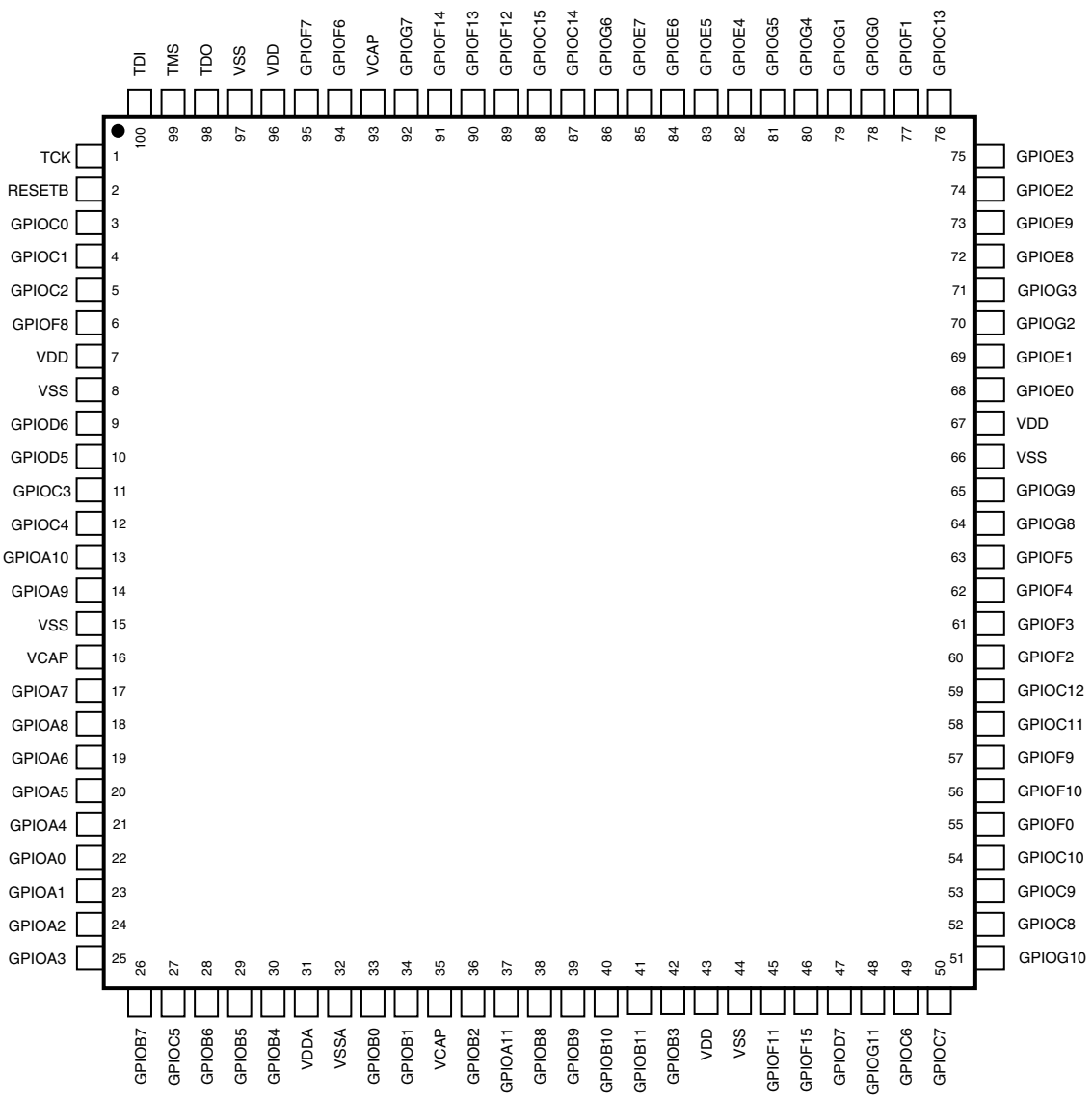


Figure 23. 100-pin LQFP

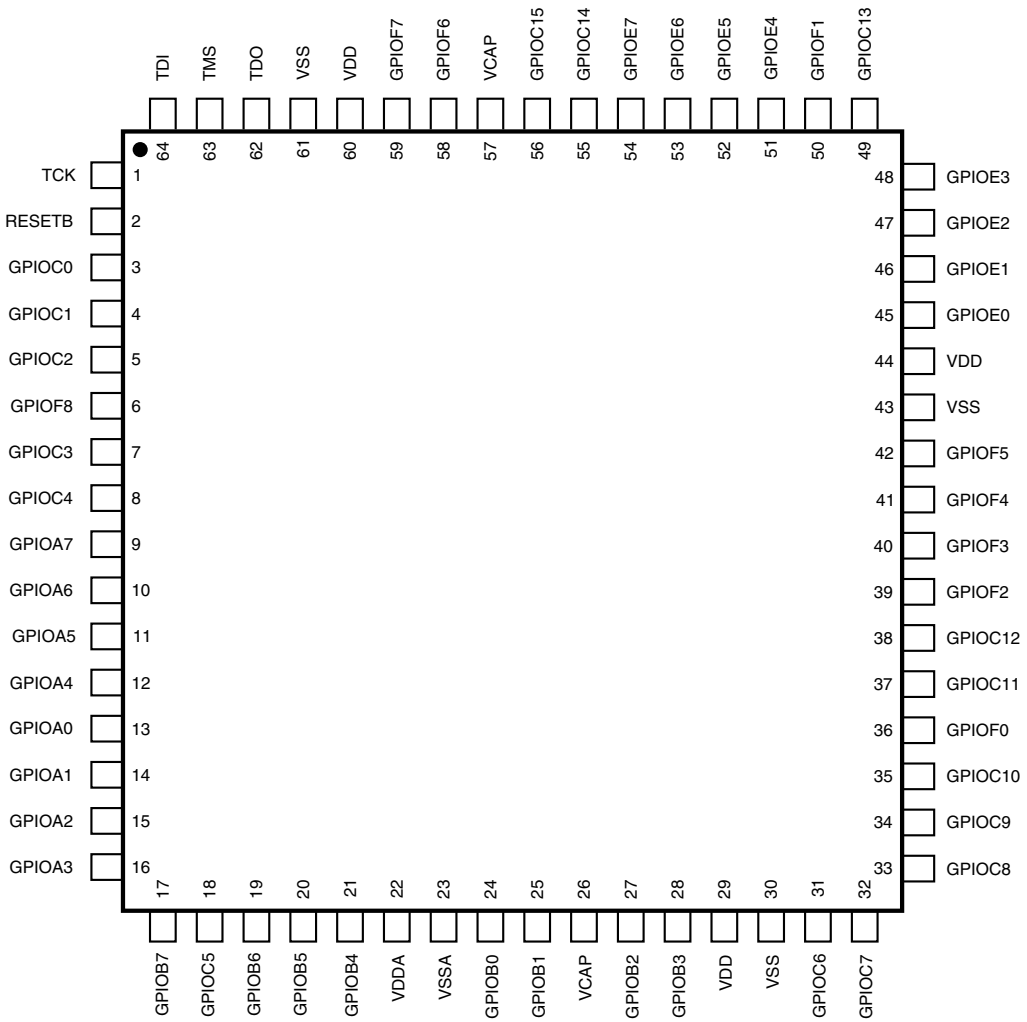


Figure 25. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product Documentation

The documents listed in Table 36 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at http://www.freescale.com.

Table 36. Device Documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F847xx Reference Manual	Detailed functional description and programming model	MC56F847XXRM
Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the DSC family of devices	
MC56F847xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F847XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev.	Date	Substantial Changes
3	08/2012	In various locations: Clarified that the RESETB pin is a 3.3 V pin only
		MC56F844x/5x/7x Product Family: Clarified that DAC table row applies to 12-bit DAC
		Voltage and current operating ratings: Added rows for RESET input voltage range and RESET output voltage range
		Voltage and current operating requirements: Added row for RESET voltage high, and added new final footnote
		Voltage and current operating behaviors: For Digital Input Current High, created separate sub-rows for Pin Groups 1 and 2
		Power mode transition operating behaviors: Updated row for RESET deassertion to First Address Fetch
		Power consumption operating behaviors: Replaced all TBD values, and updated Typical at 3.3 V I_{DDA} value for WAIT mode
		EMC radiated emissions operating behaviors: Removed this section
		Thermal attributes: Updated values for 100 LQFP
		JTAG Timing: Changed divider value of Max for TCK frequency of operation
		Relaxation Oscillator Timing: Replaced all TBDs, and removed Standby Mode specification for 8 MHz Frequency Variation
		Peripheral operating requirements and behaviors: Updated Flash timing specifications and added Flash high voltage current behaviors
		16-bit ADC electrical characteristics: Updated DNL information about Max value for 16-bit modes and 12-bit modes, and updated INL information about Max value for 16-bit modes
		Signal Multiplexing and Pin Assignments: Added note about GPIOC1, added JTAG signals to table and diagrams, and changed "SCK" signal names to "SCLK"