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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 16x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84769vll

Table of Contents

Table 1. 56F844x/5x/7x Family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
PWMB with input capture: Standard channels	1x 12	1x7	1x 12	1x7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12-bit DAC	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	2	2	2	2	2	3	2	3	2	2	2	2	2	2
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total includes FlexNVM and assumes no FlexNVM is used with FlexRAM for EEPROM.

1.2 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input
  - Channels not used for PWM generation can be used for buffered output compare functions
  - Channels not used for PWM generation can be used for input capture functions
  - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware
- Support for double switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8-channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency is up to 20 MHz with as low as 50 ns period
  - Single conversion time of 8.5 ADC clock cycles
  - Additional conversion time of 6 ADC clock cycles
- Support of analog inputs for single-ended and differential conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by any module connected to internal crossbar module, such as PWM and timer modules and GPIO and comparators

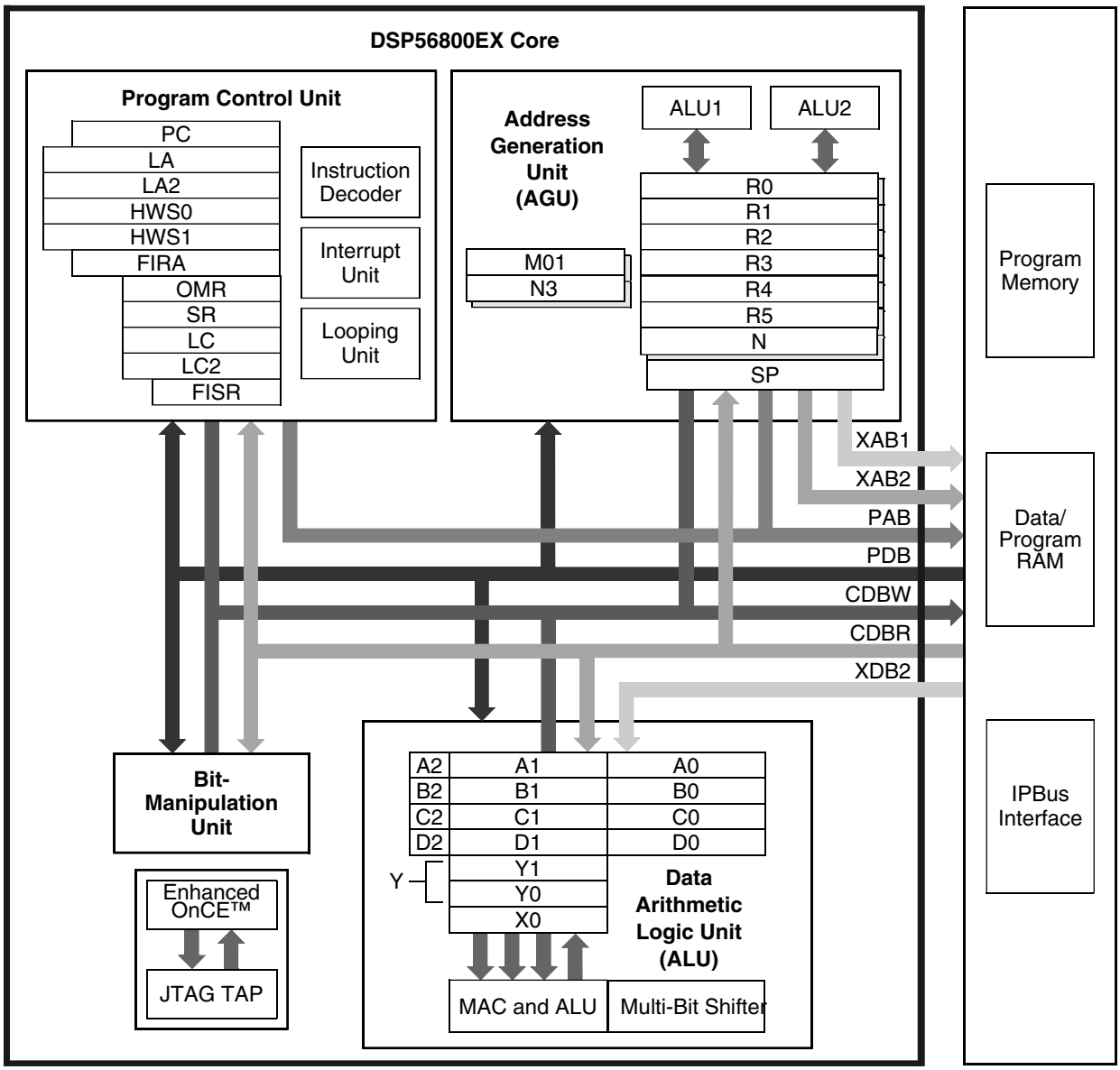


Figure 1. 56800EX Basic Block Diagram

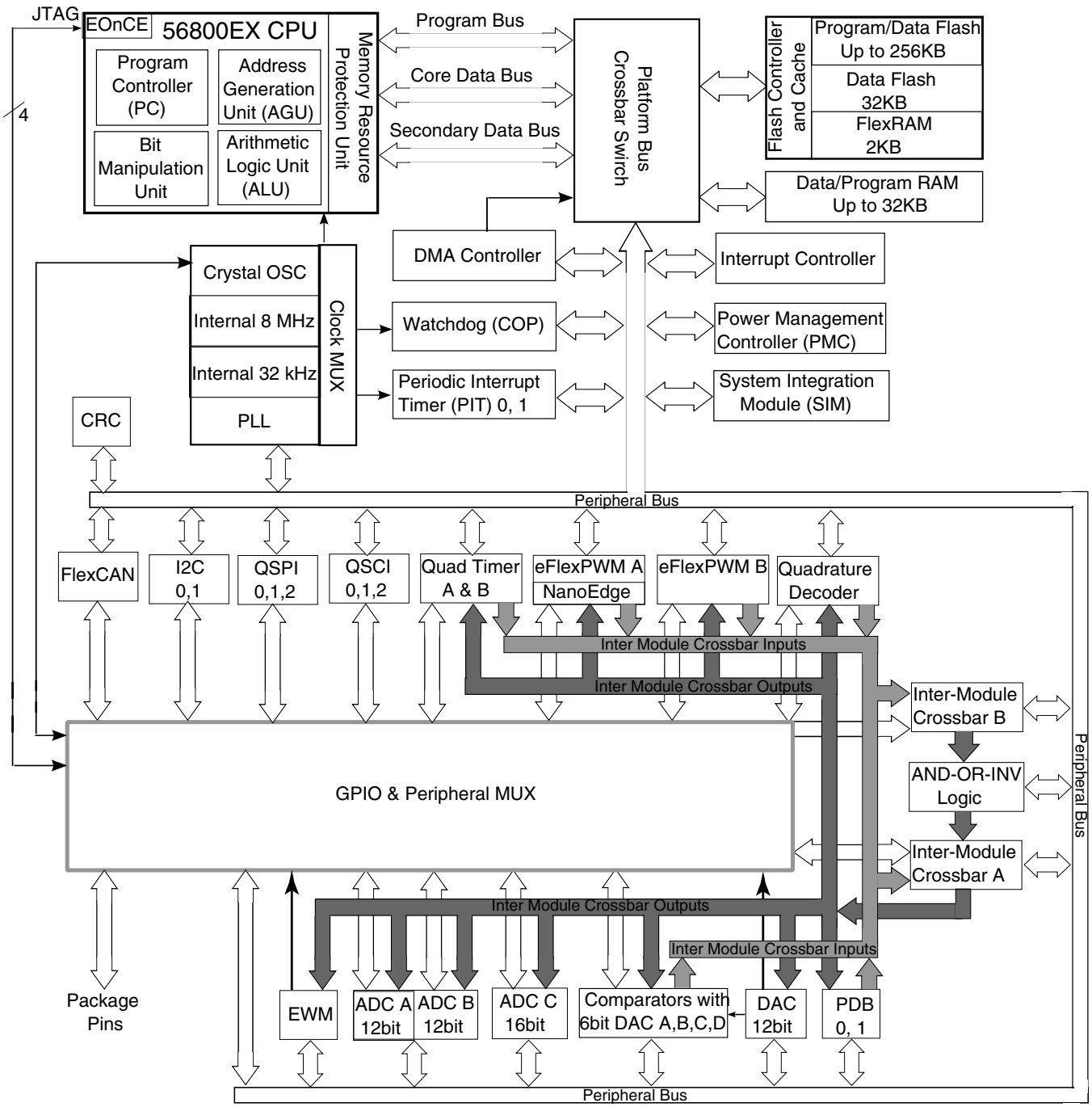


Figure 2. System Diagram

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

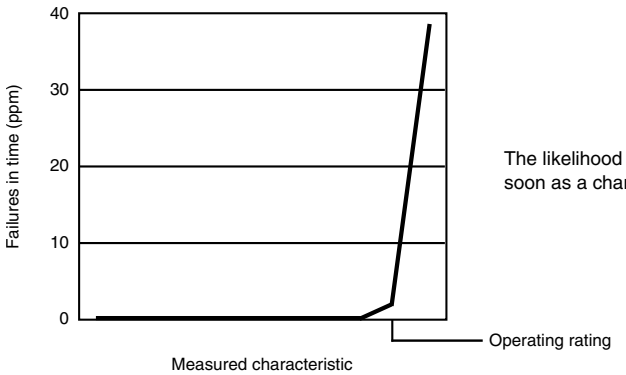
Part numbers for this device have the following format: Q 56F8 4 C F P T PP N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

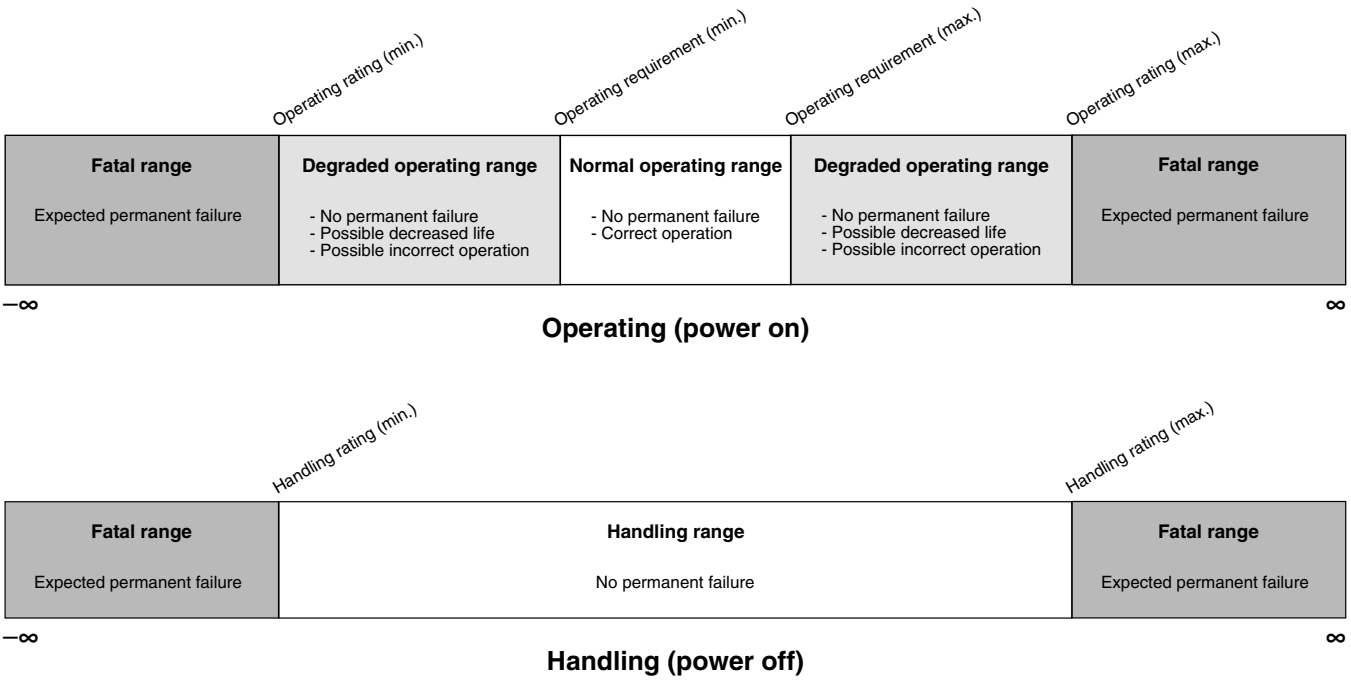
Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
4	DSC subfamily	• 4
C	Maximum CPU frequency (MHz)	• 4 = 60 MHz • 5 = 80 MHz • 7 = 100 MHz
F	Primary program flash memory size	• 4 = 64 KB • 5 = 96 KB • 6 = 128 KB • 8 = 256 KB
P	Pin count	• 0 and 1 = 48 • 2 and 3 = 64 • 4, 5, and 6 = 80 • 7, 8, and 9 = 100
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LF = 48LQFP • LH = 64LQFP • LK = 80LQFP • LL = 100LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

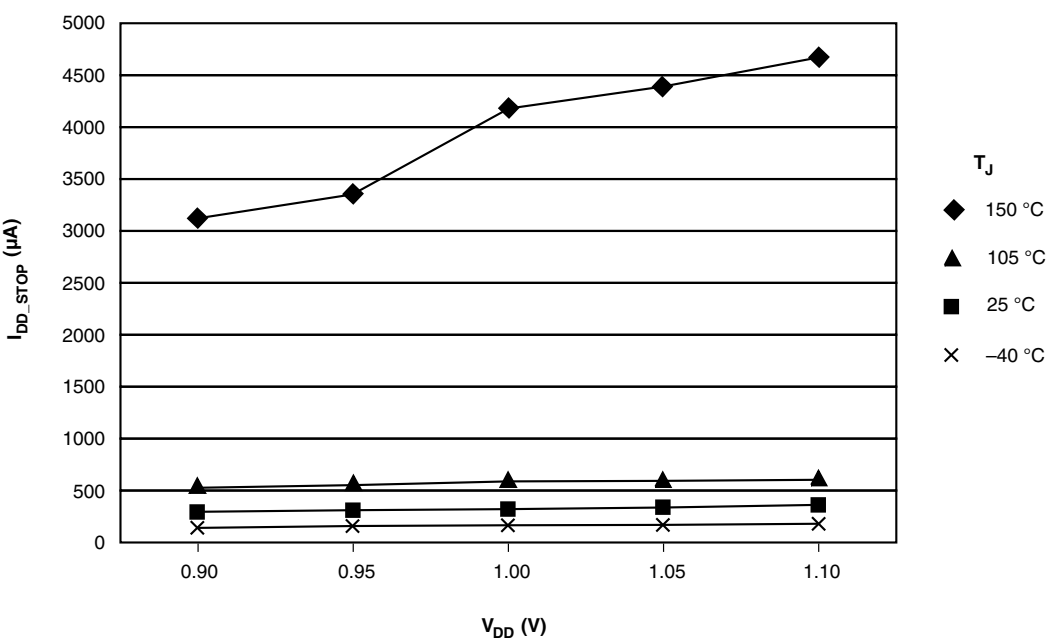
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: VSS = VSSA = 0 V, VDD = VDDA = 3.0 V to 3.6 V, CL ≤ 50 pF, f_{OP} = 100 MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

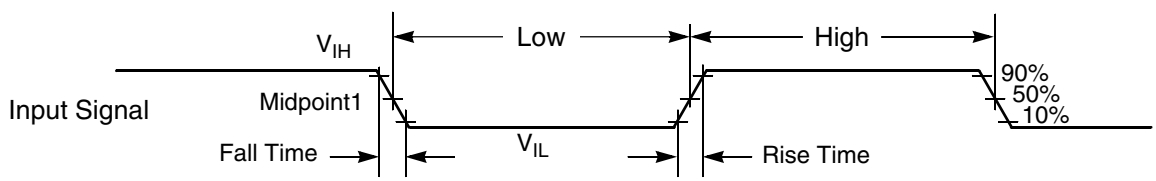


Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

7.3.5 Power consumption operating behaviors

Table 9. Current Consumption

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	100 MHz	• 100 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 1X clock • ADC/DAC powered on and clocked at 5 MHz[2] • Comparator powered on	63.7 mA	16.7 mA	101 mA	32 mA
WAIT	100 MHz	• 100 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 2X clock • ADC/DAC/Comparator powered off	43.5 mA	1.4 µA	80 mA	6.8 µA
STOP	4 MHz	• 4 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/DAC/Comparator powered off	10.1 mA	—	37 mA	—
LPRUN (LsRUN)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • Repeat NOP instructions • All peripheral modules enabled, except NanoEdge and cyclic ADCs[3] • Simple loop with running from platform instruction buffer	2.30 mA	2.73 mA	30 mA	5.9 mA
LPWAIT (LsWAIT)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • All peripheral modules enabled, except NanoEdge and cyclic ADCs[3] • Processor core in wait mode	2.29 mA	2.73 mA	30 mA	5.9 mA

Table continues on the next page...

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	40	49	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	44	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	34	43	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	24	35	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	12	17	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG Timing

Table 14. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/16	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

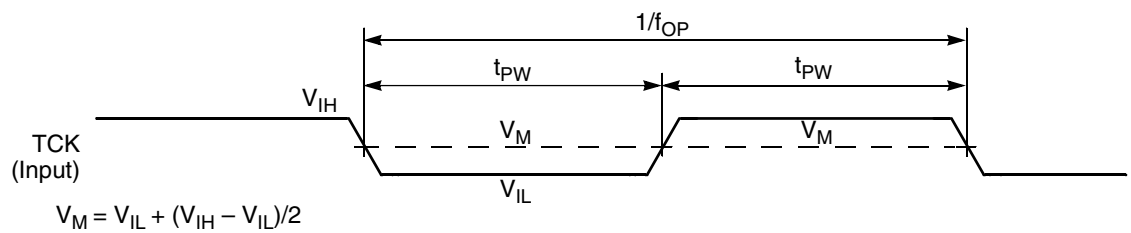


Figure 5. Test Clock Input Timing Diagram

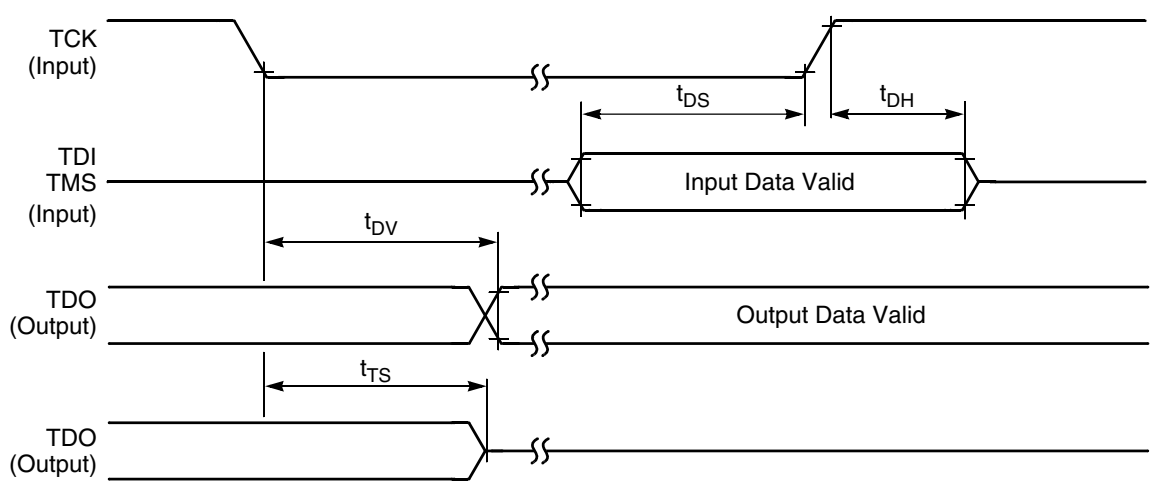


Figure 6. Test Access Port Timing Diagram

8.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

8.5 Analog

8.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 25. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	V_{DDA}	2.7	3.3	3.6	V
Vrefh Supply Voltage[2]	Vrefhx	3.0		V_{DDA}	V
ADC Conversion Clock[3]	f_{ADCCLK}	0.6		20	MHz
Conversion Range	R_{AD}	V_{REFL}		V_{REFH}	V

Table continues on the next page...

8.5.2 16-bit SAR ADC electrical specifications

8.5.2.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} - V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-/10-/12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	7
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1ns.
6. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)		250		ns
	Analog comparator initialization delay[3]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
	6-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	V_{DDA}	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[4]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Signal swing is 100 mV
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
4. 1 LSB = $V_{reference}$/64

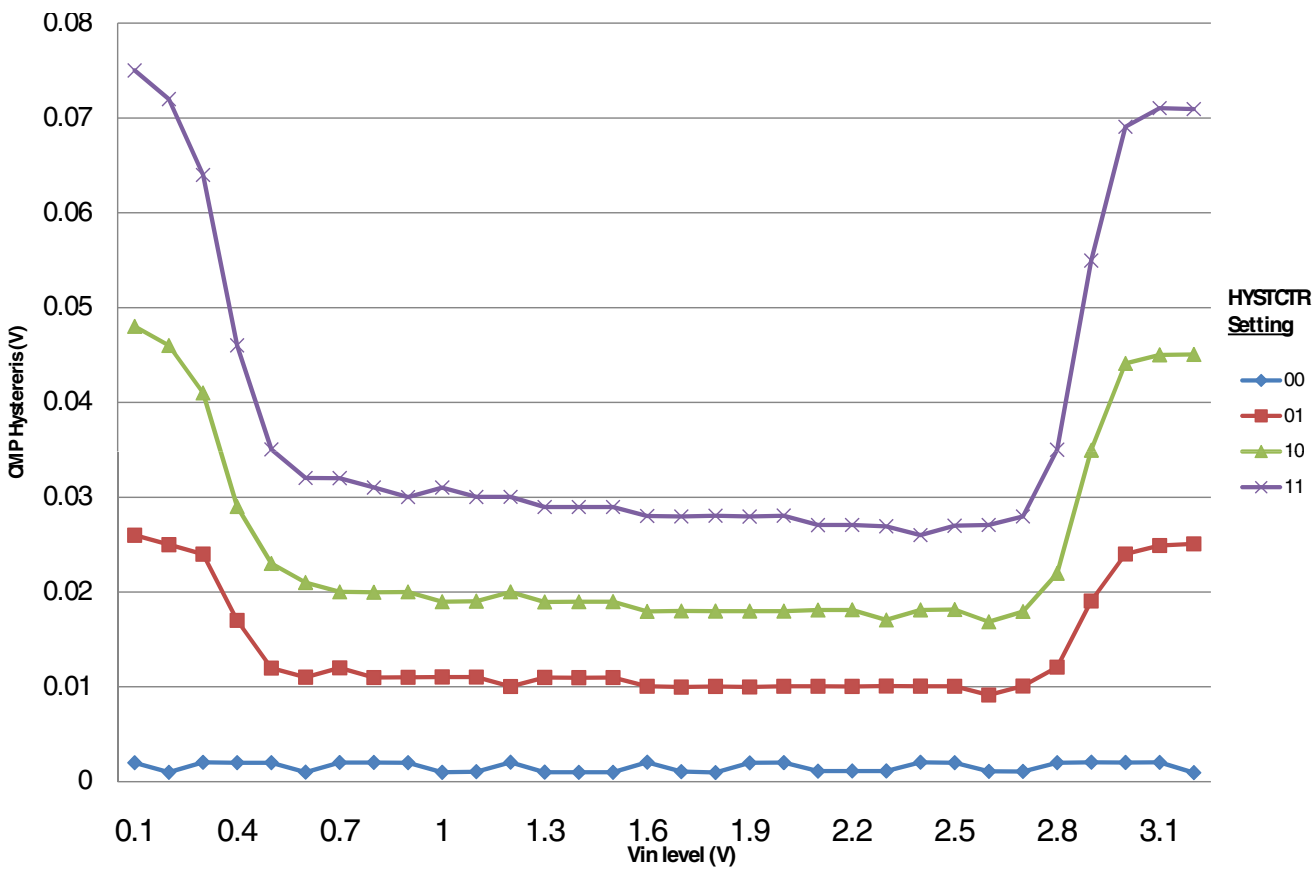


Figure 12. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Enable lead time	t_{ELD}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Enable lag time	t_{ELG}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Clock (SCK) high time	t_{CH}				Figure 15
Master		16.6	—	ns	Figure 16
Slave		16.6	—	ns	Figure 17
					Figure 18
Clock (SCK) low time	t_{CL}				Figure 18
Master		16.6	—	ns	
Slave		16.6	—	ns	
Data set-up time required for inputs	t_{DS}				Figure 15
Master		16.5	—	ns	Figure 16
Slave		1	—	ns	Figure 17
					Figure 18
Data hold time required for inputs	t_{DH}				Figure 15
Master		1	—	ns	Figure 16
Slave		3	—	ns	Figure 17
					Figure 18
Access time (time to data active from high-impedance state)	t_A				Figure 18
Slave		5	—	ns	
Disable time (hold time to high-impedance state)	t_D				Figure 18
Slave		5	—	ns	
Data valid for outputs	t_{DV}				Figure 15
Master		—	5	ns	Figure 16
Slave (after enable edge)		—	15	ns	Figure 17
					Figure 18
Data invalid	t_{DI}				Figure 15
Master		0	—	ns	Figure 16
Slave		0	—	ns	Figure 17
					Figure 18

Table continues on the next page...

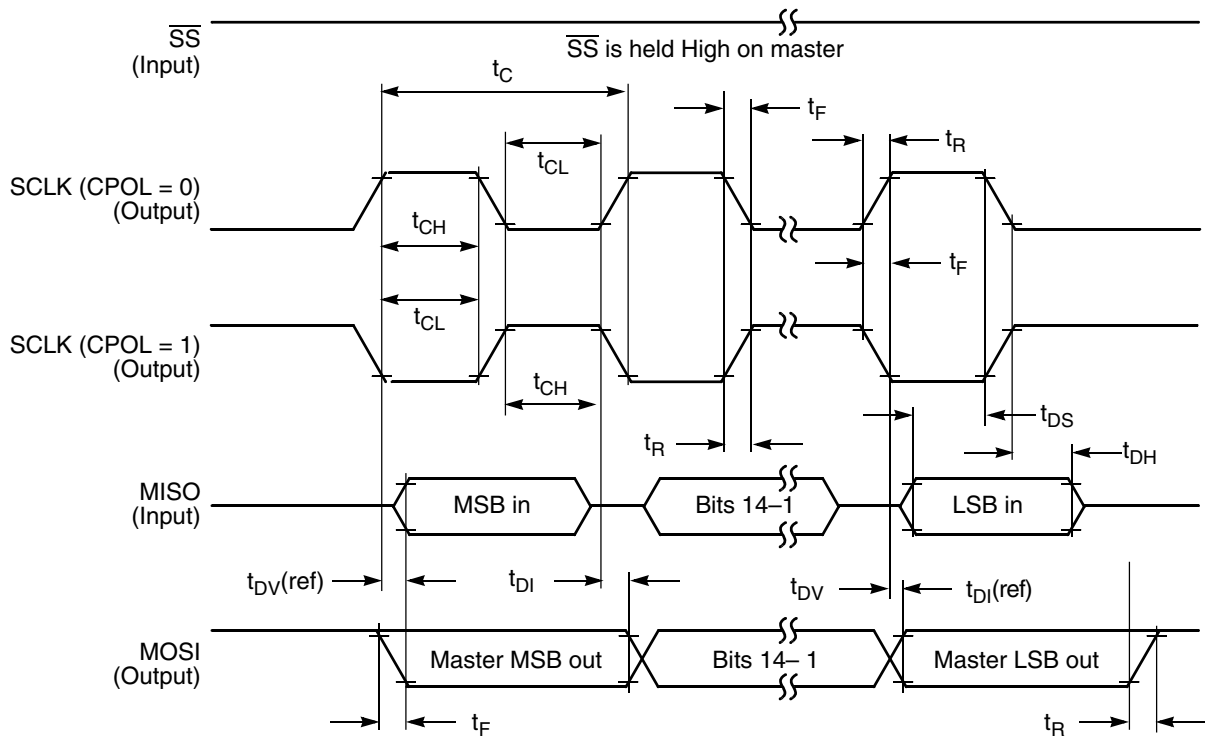


Figure 16. SPI Master Timing (CPHA = 1)

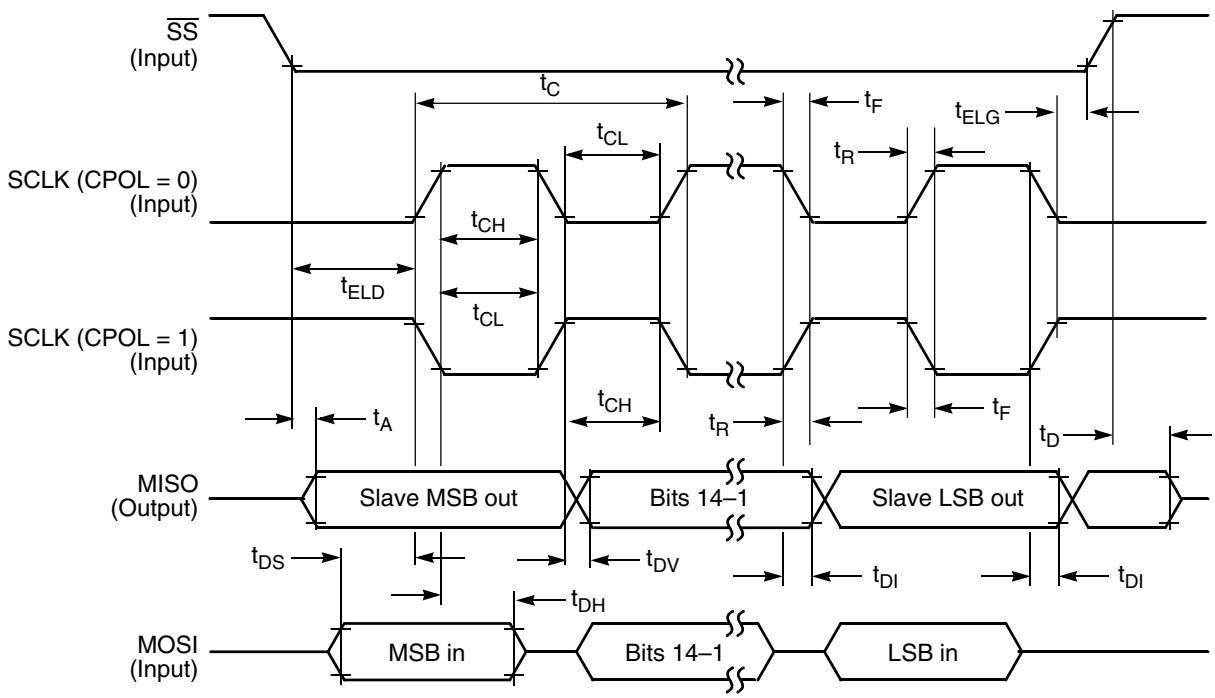


Figure 17. SPI Slave Timing (CPHA = 0)

Table 35. I ^{2}C Timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^{2}C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^{2}C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^{2}C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

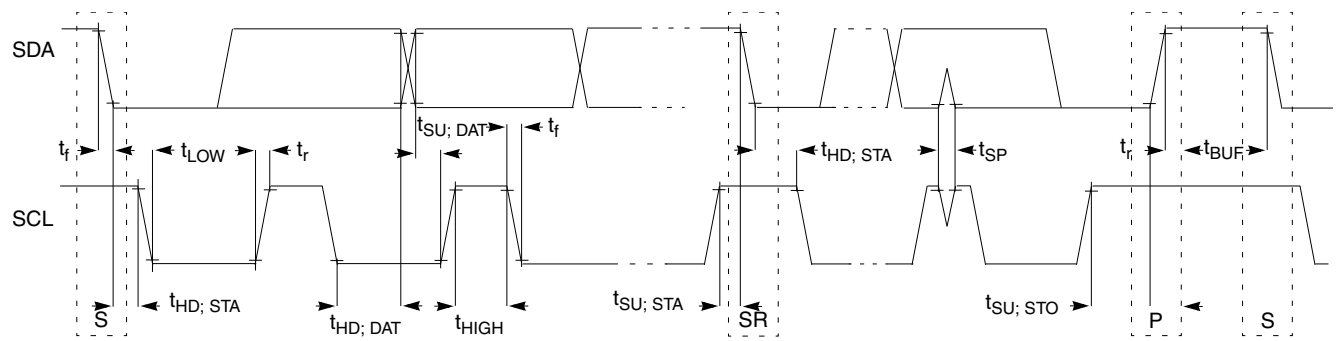


Figure 22. Timing Definition for Fast and Standard Mode Devices on the I^{2}C Bus

9 Design Considerations

9.1 Thermal Design Considerations

An estimation of the chip junction temperature, TJ, can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

9.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
64	—	—	GPIOG8	GPIOG8	PWMB_0X	PWMA_0X	TA2	XB_OUT10
65	—	—	GPIOG9	GPIOG9	PWMB_1X	PWMA_1X	TA3	XB_OUT11
66	53	43	VSS	VSS				
67	54	44	VDD	VDD				
68	55	45	GPIOE0	GPIOE0	PWMA_0B			
69	56	46	GPIOE1	GPIOE1	PWMA_0A			
70	57	—	GPIOG2	GPIOG2	PWMB_0B	XB_OUT4		
71	58	—	GPIOG3	GPIOG3	PWMB_0A	XB_OUT5		
72	—	—	GPIOE8	GPIOE8	PWMB_2B	PWMA_FAULT0		
73	—	—	GPIOE9	GPIOE9	PWMB_2A	PWMA_FAULT1		
74	59	47	GPIOE2	GPIOE2	PWMA_1B			
75	60	48	GPIOE3	GPIOE3	PWMA_1A			
76	61	49	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
77	62	50	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
78	63	—	GPIOG0	GPIOG0	PWMB_1B	XB_OUT6		
79	64	—	GPIOG1	GPIOG1	PWMB_1A	XB_OUT7		
80	—	—	GPIOG4	GPIOG4	PWMB_3B	PWMA_FAULT2		
81	—	—	GPIOG5	GPIOG5	PWMB_3A	PWMA_FAULT3		
82	65	51	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		
83	66	52	GPIOE5	GPIOE5	PWMA_2A	XB_IN3		
84	67	53	GPIOE6	GPIOE6	PWMA_3B	XB_IN4	PWMB_2B	
85	68	54	GPIOE7	GPIOE7	PWMA_3A	XB_IN5	PWMB_2A	
86	69	—	GPIOG6	GPIOG6	PWMA_FAULT4	PWMB_FAULT4	TB2	XB_OUT8
87	70	55	GPIOC14	GPIOC14	SDA0	XB_OUT4		
88	71	56	GPIOC15	GPIOC15	SCL0	XB_OUT5		
89	—	—	GPIOF12	GPIOF12	MISO1	PWMB_FAULT2		
90	—	—	GPIOF13	GPIOF13	MOSI1	PWMB_FAULT1		
91	—	—	GPIOF14	GPIOF14	SCLK1	PWMB_FAULT0		
92	72	—	GPIOG7	GPIOG7	PWMA_FAULT5	PWMB_FAULT5	XB_OUT9	
93	73	57	VCAP	VCAP				
94	74	58	GPIOF6	GPIOF6	TB2	PWMA_3X	PWMB_3X	XB_IN2
95	75	59	GPIOF7	GPIOF7	TB3	CMPC_O	SS1_B	XB_IN3
96	76	60	VDD	VDD				
97	77	61	VSS	VSS				
98	78	62	TDO	TDO	GPIOD1			
99	79	63	TMS	TMS	GPIOD3			
100	80	64	TDI	TDI	GPIOD0			