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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 16x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84789vll

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1 Overview

1.1 MC56F844x/5x/7x Product Family

The following table highlights major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. 56F844x/5x/7x Family

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
Core freq. (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory (KB) ¹	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12-bit Cyclic ADC channels	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x5 (600 ns)	2x8 (600 ns)	2x5 (600 ns)
16-bit SAR ADC (with Temp Sensor) channels	1x 16	1x 10	1x 16	1x 10	1x8	1x8	0	1x8	0	1x 16	1x 10	1x 16	1x 10	0	1x8	0	1x8	0
PWMA with input capture:																		
High-resolution channels	1x8	1x8	1x8	1x8	1x8	1x8	1x6	1x8	1x6	0	0	0	0	0	0	0	0	0
Standard channels	4	1	4	1	1	1	0	1	0	2x 12	1x 12, 1x9	2x 12	1x 12, 1x9	1x9	1x9	1x6	1x9	1x6

Table continues on the next page...

- Support for simultaneous and software triggering conversions
- Support for multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, Comparators, Quad Timers, eFlexPWMs, PDBs, EWM, Quadrature Decoder, and select I/O pins
- User-defined input/output pins for all modules connected to crossbar
- DMA request and interrupt generation from crossbar
- Write-once protection for all registers
- AND-OR-INVERT function that provides a universal Boolean function generator using a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high speed mode and low speed mode
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising edge, falling edge, or toggle of comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms including square, triangle, and sawtooth waveforms for applications such as slope compensation
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally off chip

- Option to transpose input data or output data (CRC result) bitwise or bytewise,¹ which is required for certain CRC standards
- Option for inversion of final CRC result

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block Diagrams

The 56800EX core is based on a modified dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The device's basic architecture appears in [Figure 1](#) and [Figure 2](#). [Figure 1](#) illustrates how the 56800EX system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800EX core. [Figure 2](#) shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

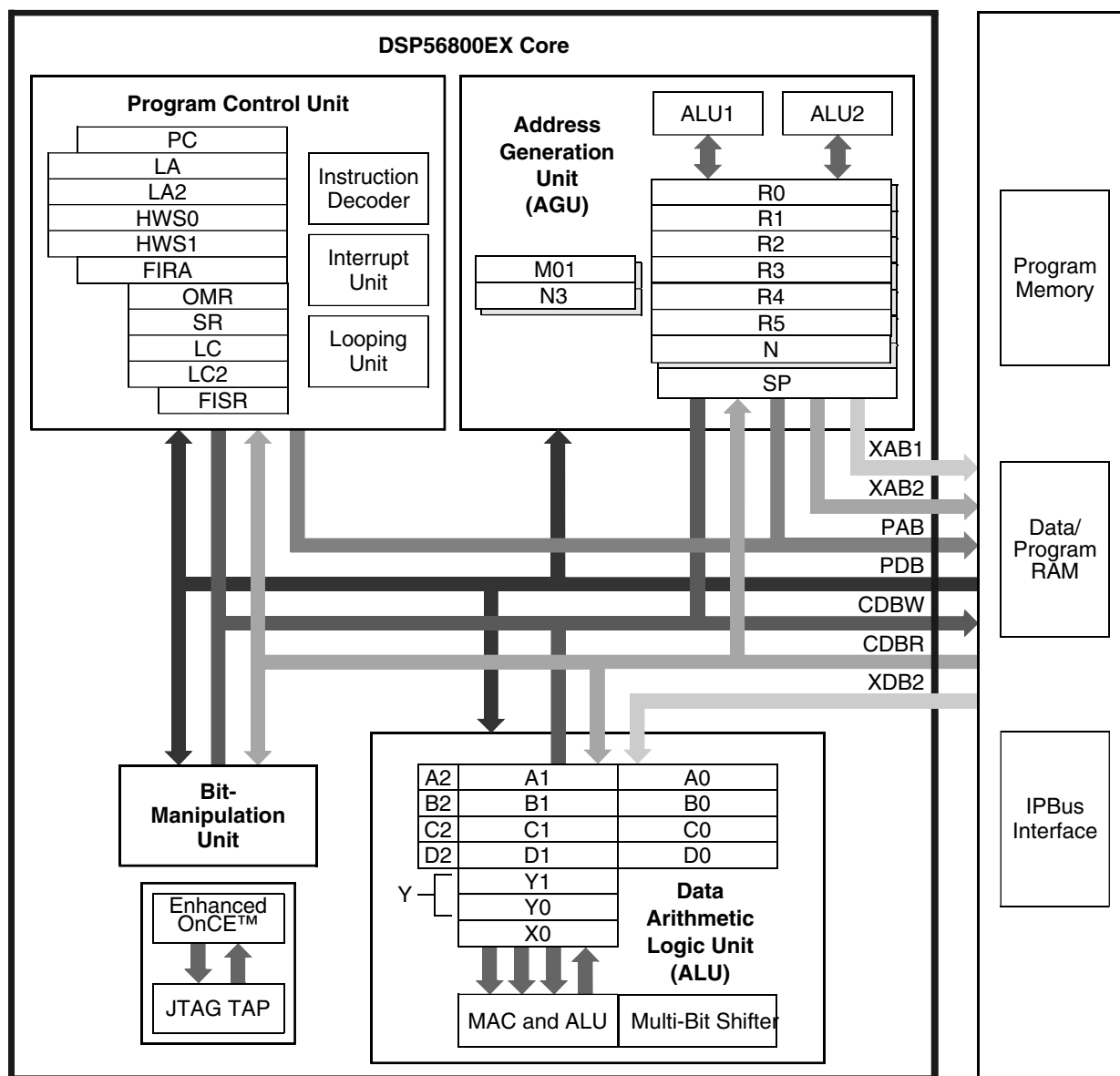


Figure 1. 56800EX Basic Block Diagram

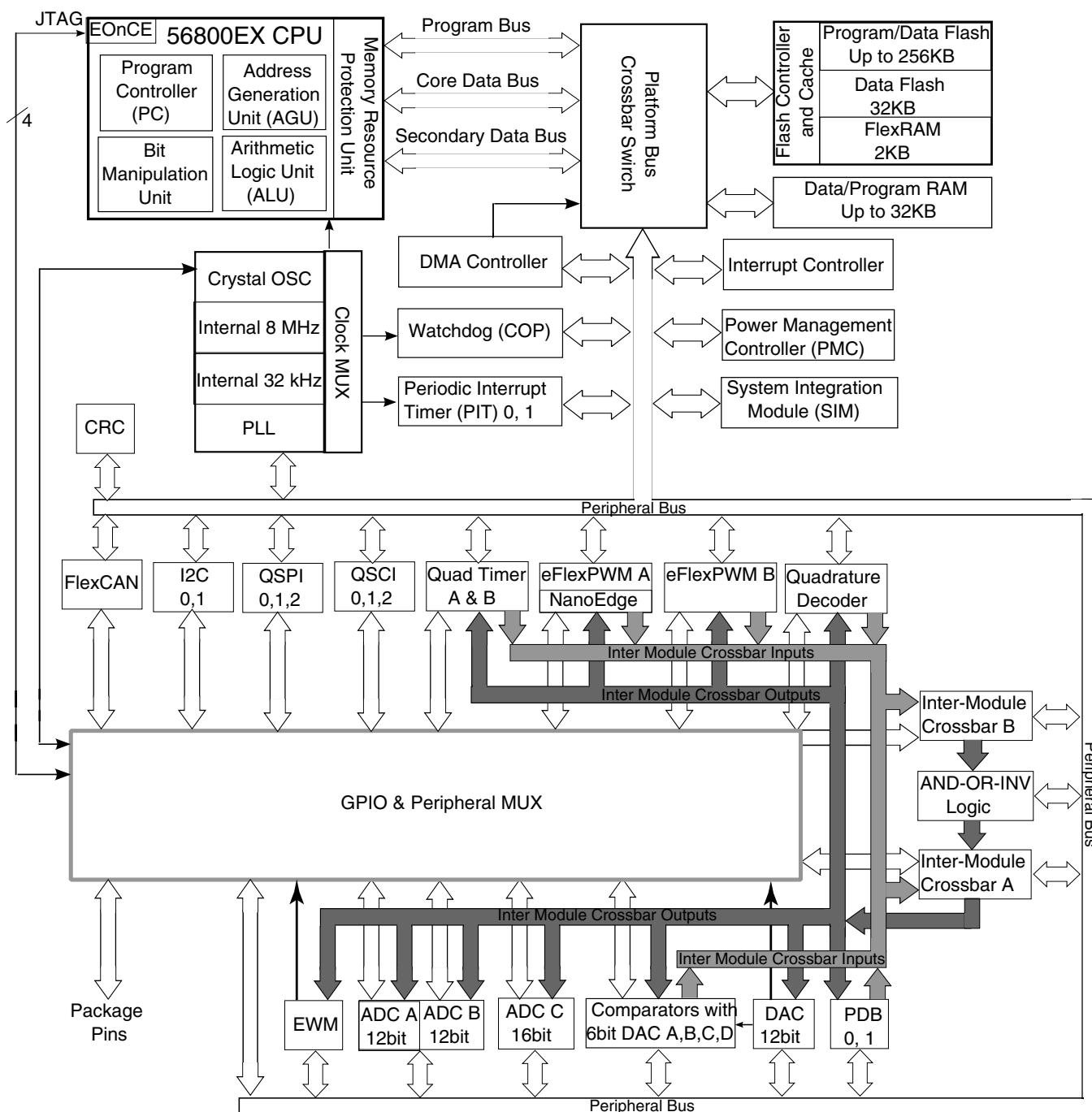


Figure 2. System Diagram

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

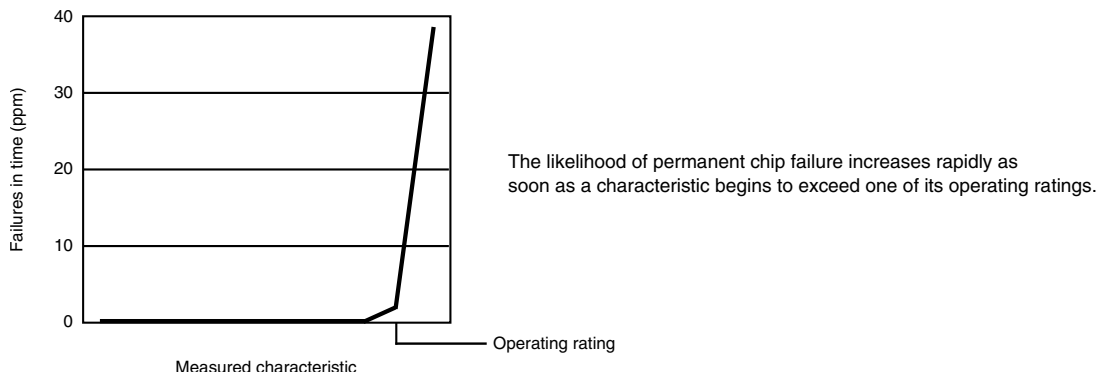
Part numbers for this device have the following format: Q 56F8 4 C F P T PP N

4.3 Fields

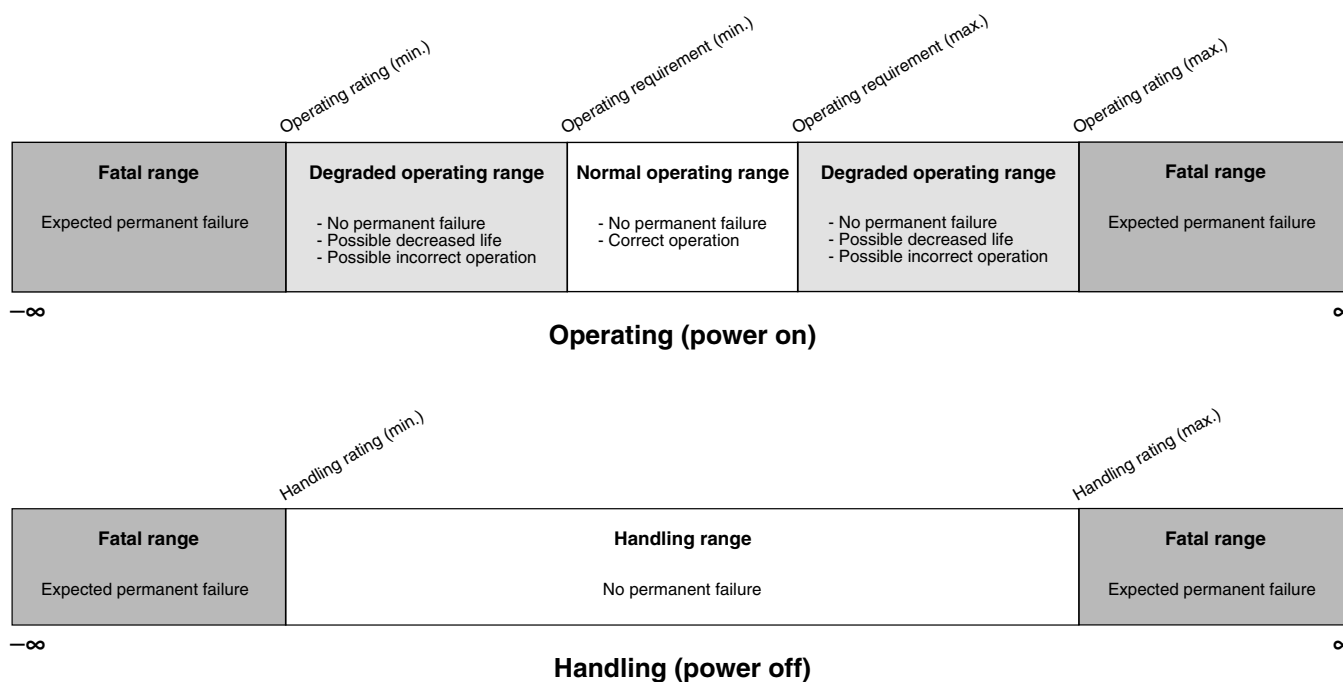
This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> MC = Fully qualified, general market flow PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	<ul style="list-style-type: none"> 56F8
4	DSC subfamily	<ul style="list-style-type: none"> 4
C	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> 4 = 60 MHz 5 = 80 MHz 7 = 100 MHz
F	Primary program flash memory size	<ul style="list-style-type: none"> 4 = 64 KB 5 = 96 KB 6 = 128 KB 8 = 256 KB
P	Pin count	<ul style="list-style-type: none"> 0 and 1 = 48 2 and 3 = 64 4, 5, and 6 = 80 7, 8, and 9 = 100
T	Temperature range (°C)	<ul style="list-style-type: none"> V = -40 to 105
PP	Package identifier	<ul style="list-style-type: none"> LF = 48LQFP LH = 64LQFP LK = 80LQFP LL = 100LQFP
N	Packaging type	<ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays

5.5 Result of exceeding a rating



5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

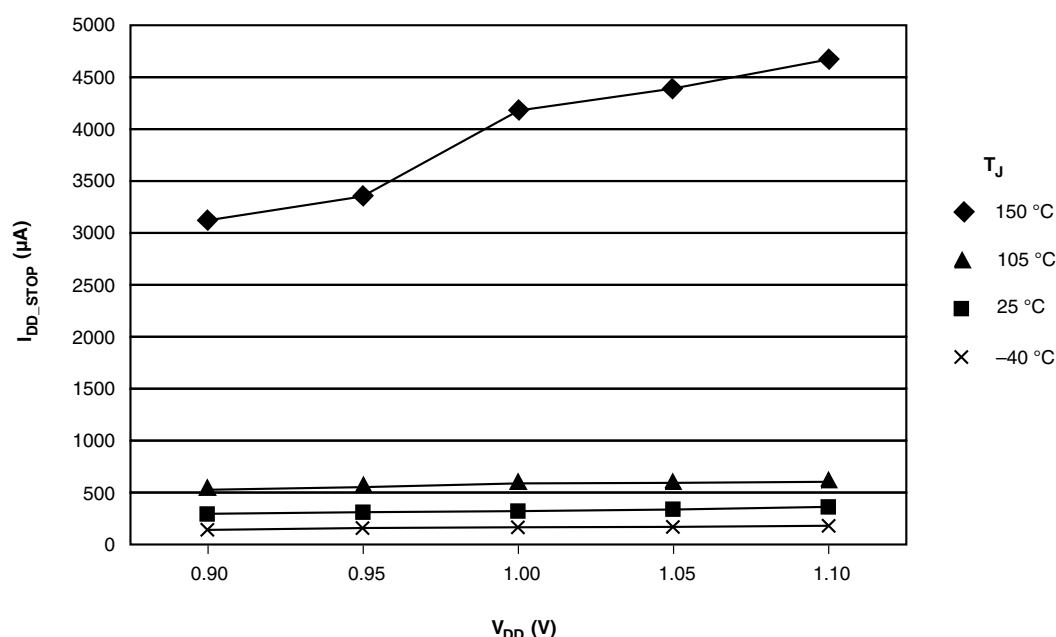
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic ¹	Min	Max	Unit
ESD for Human Body Model (HBM)	-2000	+2000	V
ESD for Machine Model (MM)	-200	+200	V
ESD for Charge Device Model (CDM)	-500	+500	V
Latch-up current at TA= 85°C (I _{LAT})	-100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 4](#) may affect device reliability or cause permanent damage to the device.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes ¹	Min	Max	Unit
Supply Voltage Range	V _{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V _{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V _{REFHx}		-0.3	4.0	V
Voltage difference V _{DD} to V _{DDA}	ΔV _{DD}		-0.3	0.3	V
Voltage difference V _{SS} to V _{SSA}	ΔV _{SS}		-0.3	0.3	V

Table continues on the next page...

Table 4. Absolute Maximum Ratings ($V_{SS} = 0\text{ V}$, $V_{SSA} = 0\text{ V}$) (continued)

Characteristic	Symbol	Notes ¹	Min	Max	Unit
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
RESET Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin ($V_{IN} < V_{SS} - 0.3\text{ V}$) ^{2, 3}	V_{IC}		—	-5.0	mA
Output clamp current, per pin ⁴	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
RESET Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature Industrial	T_A		-40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. Default Mode

- Pin Group 1: GPIO, TDI, TDO, TMS, TCK
 - Pin Group 2: RESET
 - Pin Group 3: ADC and Comparator Analog Inputs
 - Pin Group 4: XTAL, EXTAL
 - Pin Group 5: DAC analog output
2. Continuous clamp current
 3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through a ESD protection diode. There is no diode connection to VDD. If V_{IN} greater than $VDIO_MIN (=VSS-0.3V)$ is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required.
 4. I/O is configured as push-pull mode.

7 General

7.1 General Characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except for the \overline{RESET} pin which is 3.3 V only. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum

voltage of $3.3\text{ V} \pm 10\%$ during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in [Table 4](#) are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges:

$V_{SS} = V_{SSA} = 0\text{ V}$, $V_{DD} = V_{DDA} = 3.0\text{ V}$ to 3.6 V , $CL \leq 50\text{ pF}$, $f_{OP} = 100\text{ MHz}$.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in [Table 7](#). Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in [Figure 3](#).

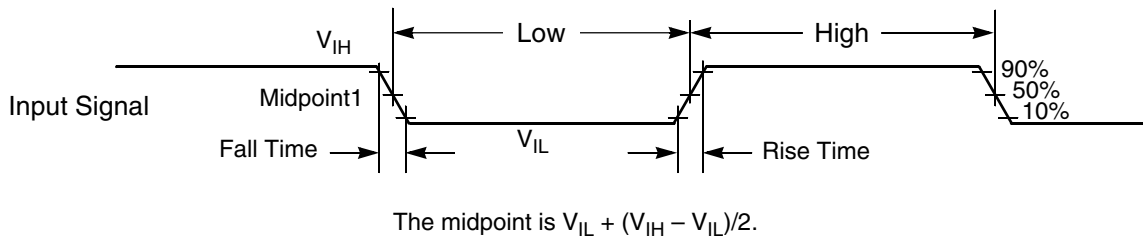


Figure 3. Input Signal Measurement References

[Figure 4](#) shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

Table 12. Switching Timing (continued)

Symbol	Description	Min	Max	Unit	Notes
	Port rise and fall time (low drive strength). Slew disabled . 2.7 $\leq V_{DD} \leq 3.6V$	8.2	17.8	ns	4
	Port rise and fall time (low drive strength). Slew enabled . 2.7 $\leq V_{DD} \leq 3.6V$	3.2	9.2	ns	4

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIO_n_IPOLR and GPIO_n_IENR.
2. The greater synchronous and asynchronous timing must be met.
3. 75 pF load
4. 15 pF load

7.5 Thermal specifications

7.5.1 Thermal operating requirements

Table 13. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature (extended industrial)	-40	105	°C

7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See [Thermal Design Considerations](#) for more detail on thermal design considerations.

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	64	55	62	°C/W	1, 2

Table continues on the next page...

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	40	49	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	44	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	34	43	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	24	35	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	12	17	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

8.3.4 Relaxation Oscillator Timing

Table 20. Relaxation Oscillator Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency ¹					
RUN Mode					
• 0°C to 105°C		7.84	8	8.16	MHz
• -40°C to 105°C		7.76	8	8.24	
Standby Mode (IRC trimmed @ 8 MHz)					
• -40°C to 105°C		266.8	402	554.3	kHz
8 MHz Frequency Variation					
RUN Mode					
Due to temperature					
• 0°C to 105°C			+/- 1.5	+/-2	%
• -40°C to 105°C			+/- 1.5	+/-3	
32 kHz Output Frequency ²					
RUN Mode					
• -40°C to 105°C		30.1	32	33.9	kHz
32 kHz Output Frequency Variation					
RUN Mode					
Due to temperature					
• -40°C to 105°C			+/-2.5	+/-4	%
Stabilization Time	tstab				
• 8 MHz output ³			0.12	0.4	μs
• 32 kHz output ⁴			14.4	16.2	
Output Duty Cycle		48	50	52	%

1. Frequency after application of 8 MHz trim
2. Frequency after application of 32 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

8.6.2 Quad Timer Timing

Parameters listed are guaranteed by design.

Table 31. Timer Timing

Characteristic	Symbol	Min ¹	Max	Unit	See Figure
Timer input period	P_{IN}	$2T + 6$	—	ns	Figure 14
Timer input high/low period	P_{INHL}	$1T + 3$	—	ns	Figure 14
Timer output period	P_{OUT}	20	—	ns	Figure 14
Timer output high/low period	P_{OUTHL}	10	—	ns	Figure 14

1. T = clock cycle. For 100 MHz operation, $T = 10$ ns.

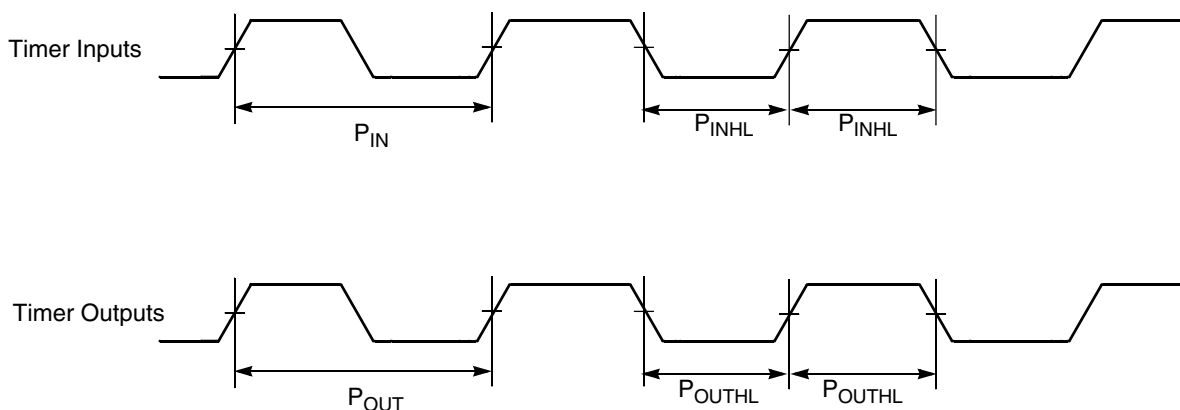


Figure 14. Timer Timing

8.7 Communication interfaces

8.7.1 Queued Serial Peripheral Interface (SPI) Timing

Parameters listed are guaranteed by design.

Table 32. SPI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time	t_C				Figure 15
Master		35	—	ns	Figure 16
Slave		35	—	ns	Figure 17
					Figure 18

Table continues on the next page...

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Rise time	t_R				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
Fall time	t_F				Figure 18
Master		—	1	ns	Figure 15
Slave		—	1	ns	Figure 16
					Figure 17
					Figure 18

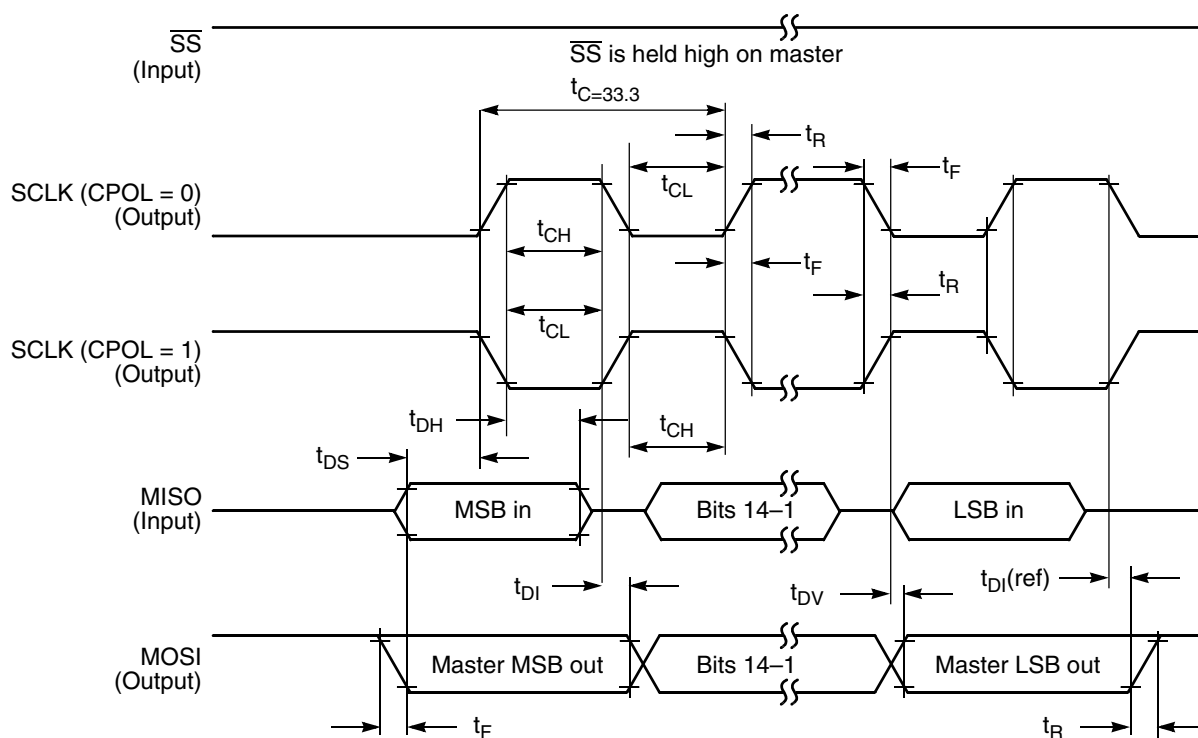
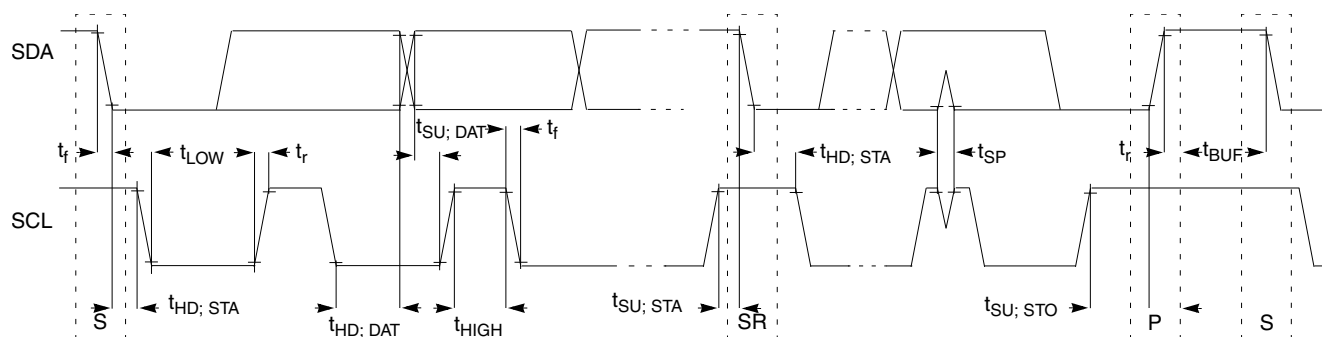
**Figure 15. SPI Master Timing (CPHA = 0)**

Table 35. I²C Timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Fall time of SDA and SCL signals	t_f	—	300	$20 + 0.1C_b^5$	300	ns
Set-up time for STOP condition	$t_{SU; STO}$	4	—	0.6	—	μs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD; DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{SU; DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

Figure 22. Timing Definition for Fast and Standard Mode Devices on the I²C Bus

9 Design Considerations

9.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

11.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

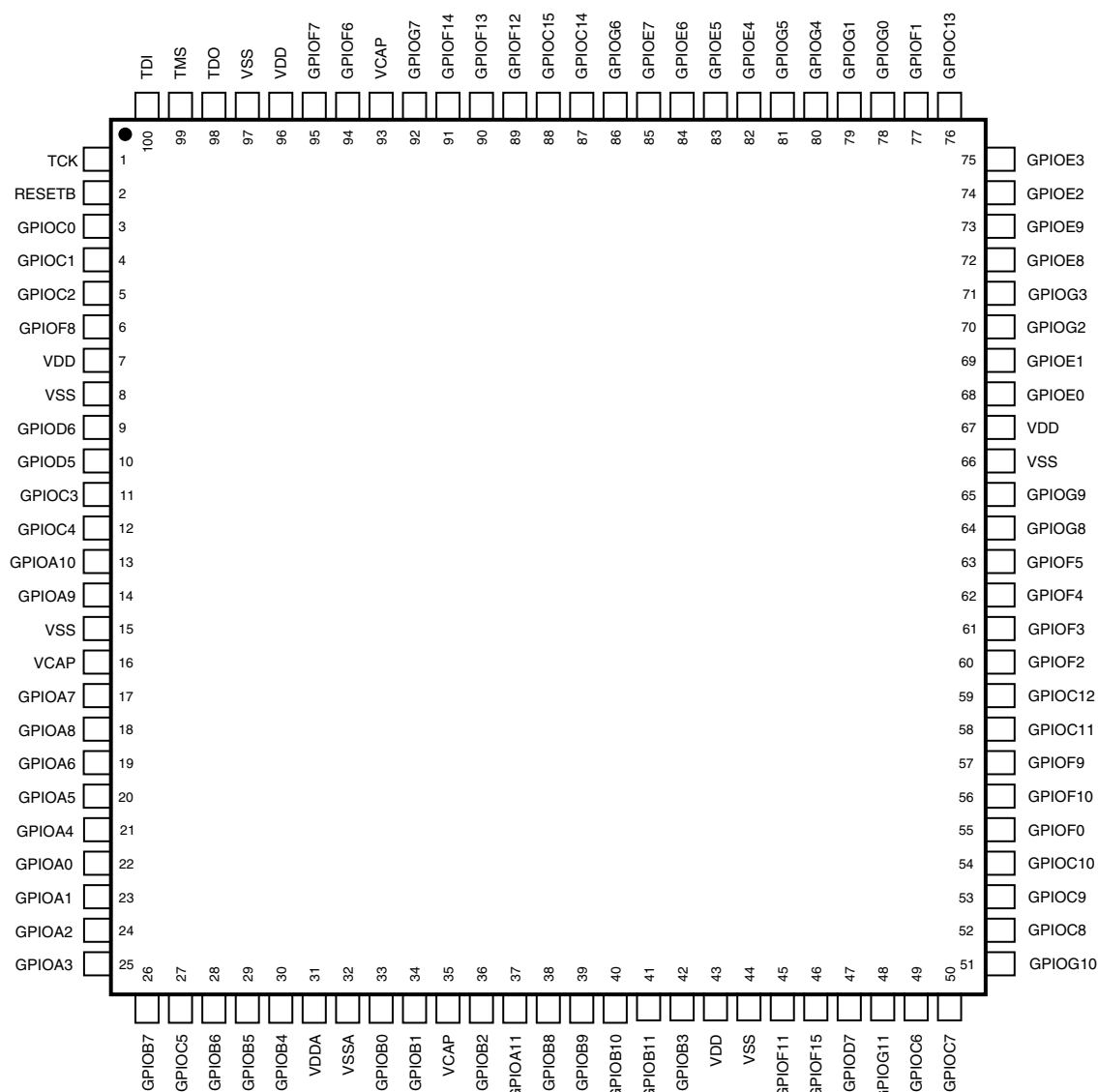


Figure 23. 100-pin LQFP

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