Analog Devices Inc./Maxim Integrated - MAX32620ICQ+ Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	1-Wire, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	49
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-30°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP Exposed Pad
Supplier Device Package	100-TQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/max32620icq

Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.)

V_{DD18}	-0.3V to +1.89V
V_{DD12}	-0.3V to +1.26V
V_{DDA} with respect to V_{SSA}	-0.3V to +1.89V
V_{RTC}	-0.3V to +1.89V
V_{DDB}	-0.3V to +3.6V
V_{REF}	-0.3V to +3.6V
32KIN, 32KOUT	-0.3V to +3.6V
RSTN, SRSTN, GPIO, DP, DM, JTAG	-0.3V to +3.6V
AIN[1:0]	-0.3V to +5.5V
AIN[3:2]	-0.3V to +3.6V
V_{DDIO}	-0.3V to +3.6V
V_{DDIOH}	-0.3V to +3.6V
Total current V_{DD18}, V_{DDIO}(sink)	100mA
Total current V_{SS}	100mA
Output current (sink) by Any I/O pin	25mA
Output current (source) by Any I/O pin	-25mA
Continuous Power Dissipation (T_A = +70°C)	
TQFP (multilayer board)	
(derate 45.5mW/°C above +70°C)	3636.4mW
Operating Temperature Range	-30°C to +85°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Package Thermal Characteristics (Note 1)

TQFP

Junction-to-Ambient Thermal Resistance (θ_{JA})	22°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})	36°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD18}		1.71	1.8	1.89	V
	V_{DD12}		1.14	1.2	1.26	
	V_{DDA}		1.71	1.8	1.89	
	V_{RTC}		1.71	1.8	1.89	
	V_{DDB}		3.04	3.3	3.60	
	V_{DDIO}		1.71	1.8	3.60	
	V_{DDIOH}	V_{DDIOH} must be ≥ V_{DDIO}	1.71	1.8	3.60	
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD18}	1.1		1.70	V
Power On Reset Voltage	V_{POR}	Monitors V_{DD18}		1.5		V
RAM Data Retention Voltage	V_{DRV}	V_{DD12} supply, retention in LP1		0.93		V
V_{DD12} Dynamic Current, LP3 Mode	I_{DD12_DLP3}	Measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current, PMU disabled		102		µA/MHz

Electrical Characteristics (continued)

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD12} Current, LP3 Mode	I_{DD12_LP3}	96MHz oscillator selected as system clock, measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current		96		µA
		4MHz oscillator selected as system clock measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current		49		
V_{DD18} Current, LP3 Mode	I_{DD18_LP3}	96MHz oscillator selected as system clock, measured on the V_{DD18} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current		366		µA
		4MHz oscillator selected as system clock, measured on the VDD18 pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current.		33		
V_{RTC} Current, LP3 Mode	I_{RTC_LP3}	RTC disabled		1.15		µA
		RTC enabled		1.55		µA
V_{DD12} Dynamic Current, LP2 Mode	I_{DD12_DLP2}	Measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active		23		µA/ MHz
V_{DD12} Current, LP2 Mode	I_{DD12_LP2}	96MHz oscillator selected as system clock, measured on the V_{DD12} pin, ARM in sleep mode, system clock stopped		96		µA
		4MHz oscillator selected as system clock, measured on the V_{DD12} pin, ARM in sleep mode, system clock stopped		49		
V_{DD18} Current, LP2 Mode	I_{DD18_LP2}	96MHz oscillator selected as system clock, ARM in sleep mode, PMU with two channels active, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current		366		µA
		4MHz oscillator selected as system clock, ARM in sleep mode, PMU with two channels active, all inputs are tied to V_{SS} or V_{DDIO}, outputs do not source/sink any current		33		
V_{RTC} Current, LP2 Mode	I_{RTC_LP2}	RTC disabled		1.15		µA
		RTC enabled		1.55		µA

Electrical Characteristics (continued)

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD12} Current, LP1 Mode	I_{DD12_LP1}	Standby state with full data retention		1.11		µA
V_{DD18} Current, LP1 Mode	I_{DD18_LP1}	Standby state with full data retention		120		nA
V_{RTC} Current, LP1 Mode	I_{RTC_LP1}	RTC disabled		244		nA
		RTC enabled		594		nA
V_{DD12} Current, LP0 Mode	I_{DD12_LP0}			14		nA
V_{DD18} Current, LP0 Mode	I_{DD18_LP0}			120		nA
V_{RTC} Current, LP0 Mode	I_{RTC_LP0}	RTC disabled		105		nA
		RTC enabled		505		nA
RTC Operating Current	I_{RTC_LP23}	LP3, LP2 modes		0.7		µA
	I_{RTC_LP01}	LP1, LP0 modes		0.35		µA
LP2 Mode Resume Time	t_{LP2_ON}			0		µs
LP1 Mode Resume Time	tLP1_ON			5		µs
LP0 Mode Resume Time	t_{LP0_ON}			11		µs
CLOCKS						
Internal Relaxation Oscillator Frequency	f_{INTCLK}	Factory default	94	96.0	98	MHz
		Firmware trimmed, required for USB compliance	95.76	96.0	96.24	MHz
Internal RC Oscillator Frequency	f_{RCCLK}		0.001	4	4.1	MHz
System Clock Frequency	f_{CK}		0.371		97.92	MHz
System Clock Period	t_{CK}			$1/f_{CK}$		
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, 6pF, ESR < 70kΩ		32.768		kHz
RTC Power Up Time	t_{RTC_ON}			250		ms
GENERAL PURPOSE I/O						
Input Low Voltage for $\overline{\text{SRSTN}}$, and All Port Pins	V_{IL}	Legacy V_{DD18} I/O supply, includes JTAG			0.3 x V_{DD18}	V
		V_{DDIO} selected as I/O supply, includes JTAG			0.3 x V_{DDIO}	
		V_{DDIOH} selected as I/O supply			0.3 x V_{DDIOH}	
Input Low Voltage for $\overline{\text{RSTN}}$	V_{IL}	Legacy V_{DD18} I/O supply			0.3 x V_{RTC}	V
		V_{DDIO} or V_{DDIOH} selected as I/O supply			0.3 x V_{RTC}	

Electrical Characteristics (continued)

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage for $\overline{\text{SRSTN}}$, and All Port Pins	V_{IH}	Legacy V_{DD18} I/O supply, includes JTAG	0.7 x V_{DD18}			V
		V_{DDIO} selected as I/O supply, includes JTAG	0.7 x V_{DDIO}			
		V_{DDIOH} selected as I/O supply	0.7 x V_{DDIOH}			
Input High Voltage for $\overline{\text{RSTN}}$	V_{IH}	Legacy V_{DD18} I/O supply	0.7 x V_{RTC}			V
		V_{DDIO} or V_{DDIOH} selected as I/O supply	0.7 x V_{RTC}			
Input Hysteresis (Schmitt)	V_{IHYS}			100		mV
Output Low Voltage for All Port Pins	V_{OL}	I_{OL} = 4mA (normal drive), legacy V_{DD18} I/O supply, includes JTAG		0.2	0.4	V
		I_{OL} = 24mA (high drive), legacy V_{DD18} I/O supply, includes JTAG		0.2	0.4	
		I_{OL} = 4mA (normal drive), V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, includes JTAG		0.2	0.4	
		I_{OL} = 24mA (high drive), V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply		0.2	0.4	
		I_{OL} = 900µA, V_{DDIO} = 1.71V, V_{DDIOH} = 2.97V, V_{DDIOH} selected as I/O supply		0.2	0.45	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All Port Pins	V_{OH}	I_{OH} = -2mA (normal drive), legacy V_{DD18} I/O supply, includes JTAG	V_{DD18} - 0.4			V
		I_{OH} = -8mA (high drive), legacy V_{DD18} I/O supply, includes JTAG	V_{DD18} - 0.4			
		I_{OH} = -2mA (normal drive), V_{DDIO} = V_{DDIOH} = 1.7V, V_{DDIO} selected as I/O supply, includes JTAG	V_{DDIO} - 0.4			
		I_{OH} = -8mA (high drive), V_{DDIO} = V_{DDIOH} = 1.7V, V_{DDIO} selected as I/O supply, includes JTAG	V_{DDIO} - 0.4			
		I_{OH} = -300µA, V_{DDIOH} = 2.97V, V_{DDIOH} selected as I/O supply	V_{DDIO} - 0.4			
		I_{OH} = -2mA, V_{DDIO} = 1.71V, V_{DDIOH} = 2.97V, V_{DDIO} selected as I/O supply	V_{DDIO} - 0.45			

Electrical Characteristics (continued)

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				48	mA
Input/Output Pin Capacitance for All Port Pins	C_{IO}			3		pF
Input Leakage Current Low	I_{IL}	V_{DD18} = 1.89V V_{IN} = 0V, internal pullup disabled, legacy V_{DD18} I/O supply	-100		+100	nA
		V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-100		+100	
Input Leakage Current High	I_{IH}	V_{DD18} = 1.89V, V_{IN} = 1.89V, internal pulldown disabled, legacy V_{DD18} I/O supply	-100		+100	nA
		V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{IN} = 3.6V, internal pulldown disabled, V_{DDIOH} selected as I/O supply	-100		+100	
	I_{OFF}	V_{DD18} = 0V, V_{IN} < 1.89V, legacy V_{DD18} I/O supply	-1		+1	µA
		V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	
	I_{IH3V}	V_{DD18} = 1.71V, V_{IN} = 3.60V, legacy V_{DD18} I/O supply	-2		+2	µA
		V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} =3.6V	-2		+2	
Input Pullup Resistor, $\overline{\text{SRSTN}}$, TMS, TCK, TDI	R_{PU_VDDIO}	Pullup to V_{DDIO}		25		kΩ
Input Pullup Resistor $\overline{\text{RSTN}}$	R_{PU_VRTC}	Pullup to V_{RTC}		25		kΩ
Input Pullup/Pulldown All GPIO	R_{PU_GPIO}	Normal resistance mode		25		kΩ
		Highest resistance mode		1		MΩ
FLASH MEMORY						
Page Size				8		kB
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		ms
Flash Programming Time Per Word	t_{PROG}			60		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +85°C	10			years

USB Electrical Characteristics

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Input High Voltage DP, DM	V_{IHD}		2.0			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to V_{SS}	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Single-Ended Receiver Threshold	V_{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF, GBD	1.3		2.0	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R_{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.090	
USB TIMING						
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF, GBD	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF, GBD	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R, t_F	C_L = 50pF, GBD	90		110	%

ADC Electrical Characteristics

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution				10		bits
ADC Clock Rate	f_{ACLK}		0.1		8	MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_CHSEL = 0–3, BUF_BYPASS = 1	V_{SSA}		V_{DDA}	V
		AIN[1:0], ADC_CHSEL = 4–5, BUF_BYPASS = 1	V_{SSA}		5.5V	
		AIN[3:0], ADC_CHSEL = 0–3, BUF_BYPASS = 0	50mV		V_{DDA} - 50mV	
		AIN[1:0], ADC_CHSEL = 4-5, BUF_BYPASS = 0	50mV		5.5V	

ADC Electrical Characteristics (continued)

(Limits are tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	R_{AIN}	AIN[1:0], ADC_HSEL = 4–5, ADC active		45		kΩ
Input Dynamic Current, Switched Capacitance	I_{AIN}	ADC active, ADC buffer bypassed		4.5		µA
		ADC active, ADC buffer enabled		50		nA
Analog Input Capacitance	C_{AIN}	Fixed capacitance to ground		1		pF
		Dynamically switched capacitance		250		nF
Integral Nonlinearity	INL				±2	LSb
Differential Nonlinearity	DNL				±1	LSb
Offset Error	V_{OS}			±1		LSb
Gain Error	GE			±2		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		240		µA
Input Buffer Active Current	I_{INBUF}			53		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of: ADC clock, ADC bias, reference buffer, or input buffer to CpuAdcStart			10	µs
		Any power-up of: ADC clock or ADC bias to CpuAdcStart			48	t_{ACLK}
ADC Output Latency	t_{ADC}			1025		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.80	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.12	4	nA
		AIN2 or AIN3, ADC inactive or channel not selected		0.02	1.0	nA
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/gain error		±2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.20		V
Signal to Noise Ratio	SNR			58.5		dB
Signal to Noise and Distortion	SINAD			58.5		dB
Total Harmonic Distortion	THD			-68.5		dB
Spurious Free Dynamic Range	SFDR			74		dB
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm/°C
Reference Input Capacitance	C_{REF_IN}	Dynamically switched capacitance, ADC_XREF=1, ADC active		250		fF
External Reference Voltage	V_{REF_EXT}	ADC_XREF = 1	1.17	1.23	1.29	V
Reference Dynamic Current	I_{REF_EXT}	ADC_XREF=1, ADC active		4.1		µA

Electrical Characteristics—SPI Master/SPIX Master

(Timing specifications are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Master Operating Frequency	f_{MCK}				48	MHz
Master SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High	t_{MCH}		$t_{MCK}/2$			ns
SCLK Output Pulse-Width Low	t_{MCL}		$(t_{MCK}/2) - 4$			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$(t_{MCK}/2) - 4$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$(t_{MCK}/2) - 4$			ns
MISO Input Valid to SCLK Sample Edge Setup	t_{MIS}		1			ns
MISO Input to SCLK Sample Edge	t_{MIH}				1	ns

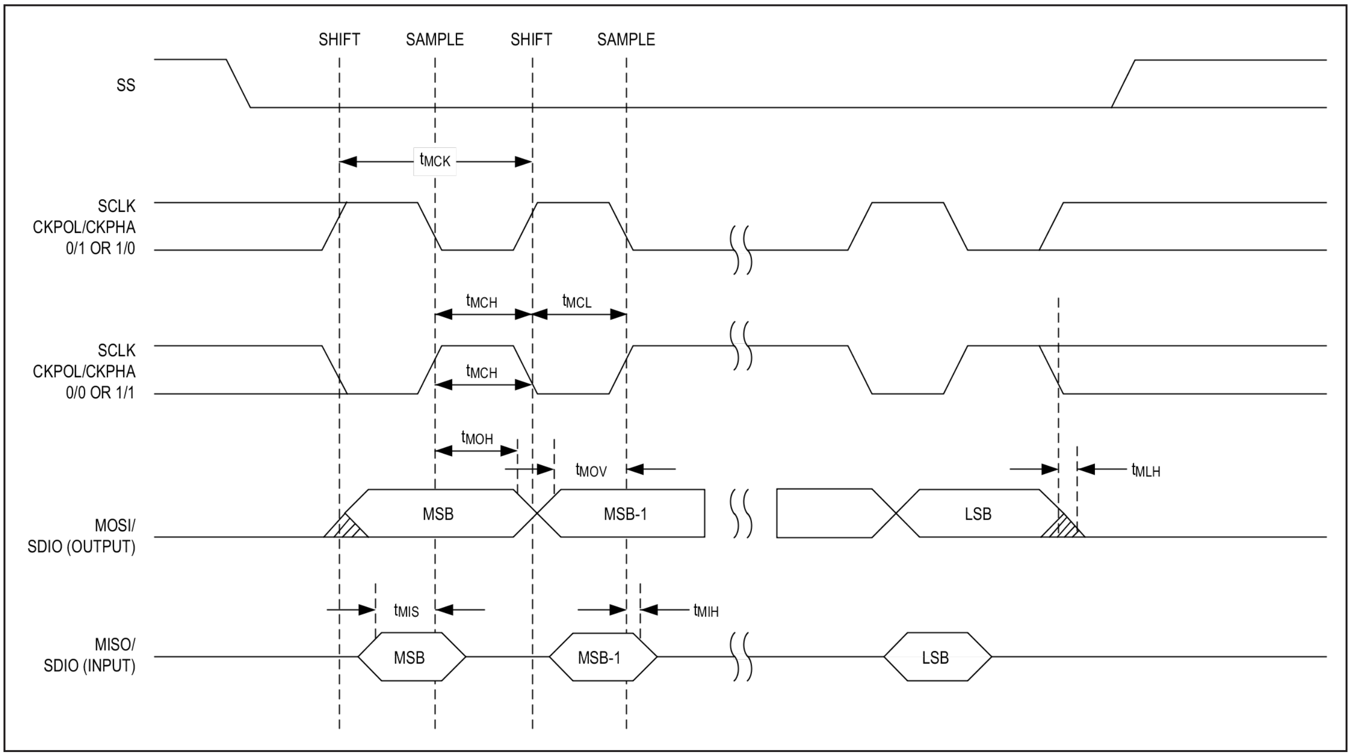
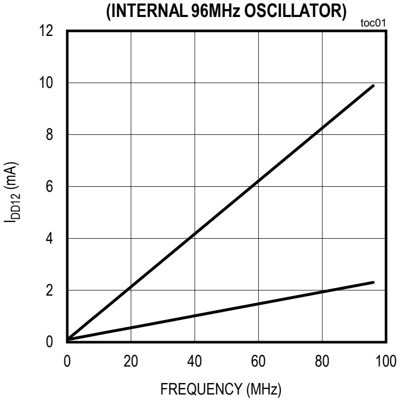


Figure 1. SPI Master and SPI XIP Master Timing

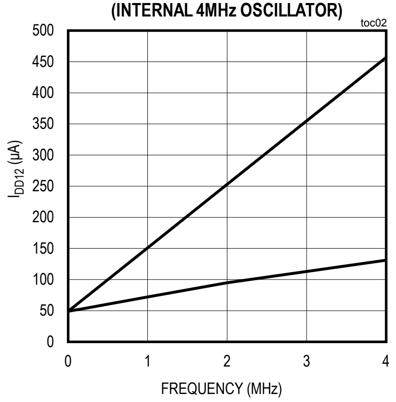
Typical Operating Characteristics

(V_{DD18} = 1.8V, V_{DD18} = 1.8V.)

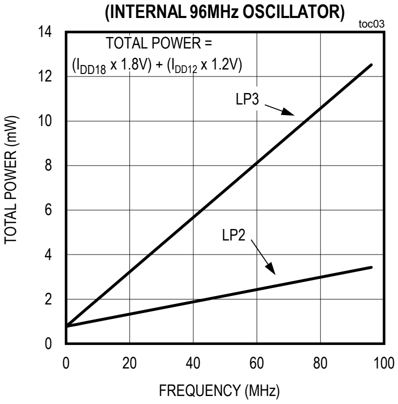
I_{DD12} vs. FREQUENCY (INTERNAL 96MHz OSCILLATOR)



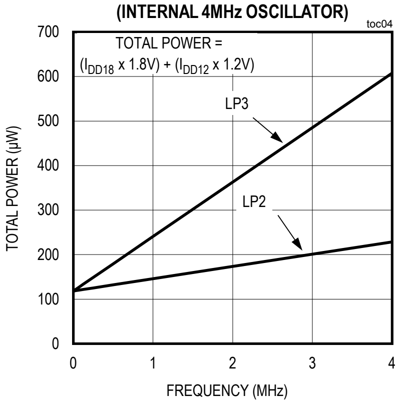
I_{DD12} vs. FREQUENCY (INTERNAL 4MHz OSCILLATOR)



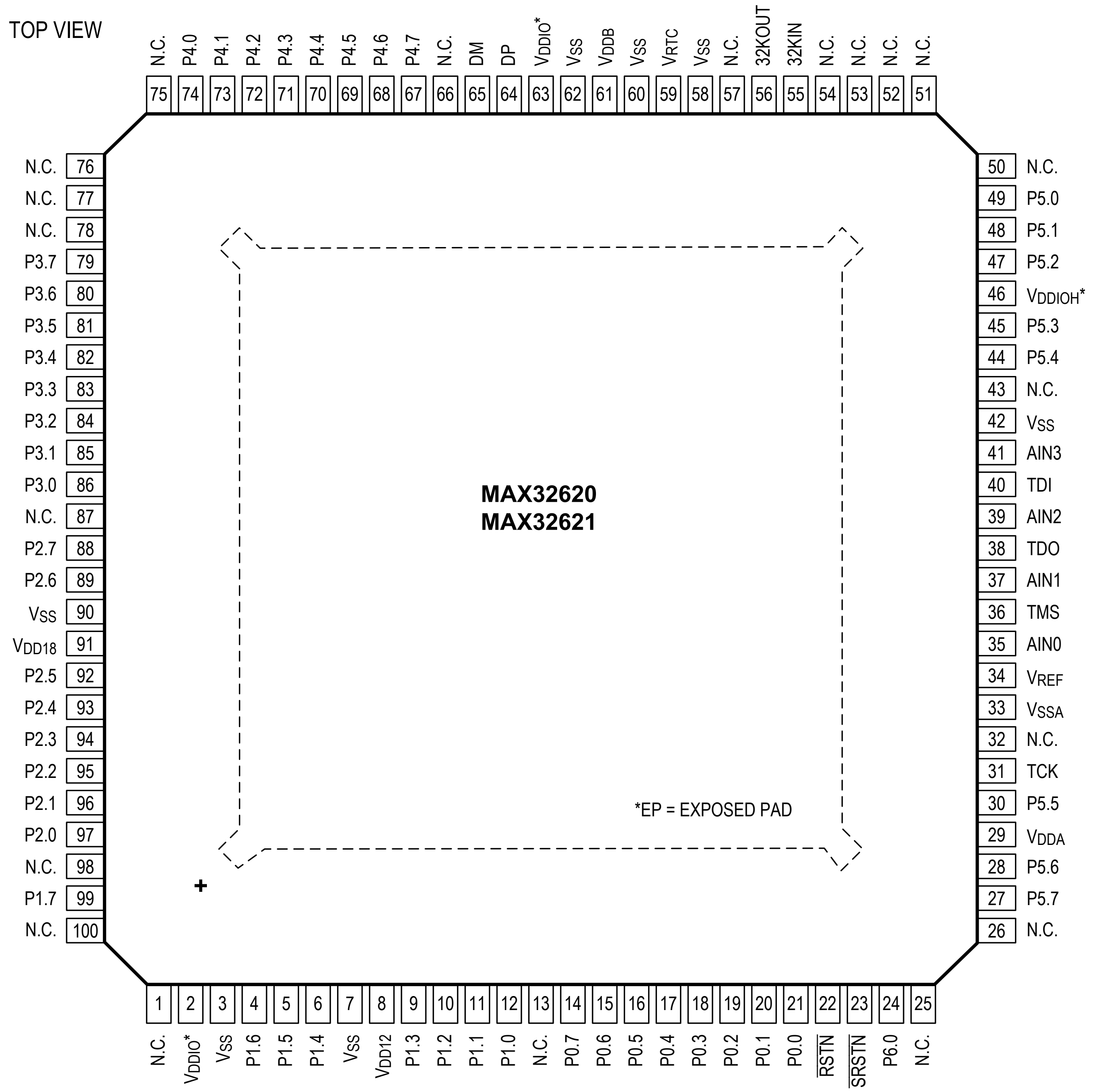
TOTAL POWER vs. FREQUENCY (INTERNAL 96MHz OSCILLATOR)



TOTAL POWER vs. FREQUENCY (INTERNAL 4MHz OSCILLATOR)



Pin Configuration



100 TQFP-EP

* V_{DD18} in legacy mode

Pin Configuration (continued)

TOP VIEW (BUMP SIDE DOWN)

MAX32620
MAX32621

	1	2	3	4	5	6	7	8	9
A	N.C.	V_{SSA}	V_{REF}	AIN0	AIN1	AIN2	AIN3	V_{DDIOH}*	N.C.
B	$\overline{SRSTN}$	$\overline{RSTN}$	V_{DDA}	TCK	TMS	TDO	TDI	V_{SS}	32KIN
C	P0.1	P0.0	P6.0	P5.7	P5.5	P5.4	P5.2	V_{RTC}	32KOUT
D	P0.4	P0.5	P0.3	P0.2	P5.6	P5.3	P5.0	V_{DDB}	V_{SS}
E	P1.0	P0.7	P0.6	P1.1	P1.5	P3.1	P5.1	DP	V_{DDIO}*
F	V_{DD12}	P1.3	P1.2	P1.4	P3.0	P3.5	P3.7	DM	P4.7
G	V_{SS}	P1.6	P1.7	P2.4	P2.6	P3.4	P4.4	P4.6	P4.5
H	V_{DDIO}*	P2.1	P2.2	P2.5	P2.7	P3.2	P4.1	P4.3	P4.2
J	N.C.	P2.0	P2.3	V_{DD18}	V_{SS}	P3.3	P3.6	P4.0	N.C.

100 WLP

* V_{DD18} in legacy mode

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
97	J2	P2.0	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 1 for details.
96	H2	P2.1	
95	H3	P2.2	
94	J3	P2.3	
93	G4	P2.4	
92	H4	P2.5	
89	G5	P2.6	
88	H5	P2.7	
86	F5	P3.0	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 1 for details.
85	E6	P3.1	
84	H6	P3.2	
83	J6	P3.3	
82	G6	P3.4	
81	F6	P3.5	
80	J7	P3.6	
79	F7	P3.7	
74	J8	P4.0	General-Purpose I/O, Port 4. Most port pins have multiple special functions. See Table 1 for details.
73	H7	P4.1	
72	H9	P4.2	
71	H8	P4.3	
70	G7	P4.4	
69	G9	P4.5	
68	G8	P4.6	
67	F9	P4.7	
49	D7	P5.0	General-Purpose I/O, Port 5. Most port pins have multiple special functions. See Table 1 for details.
48	E7	P5.1	
47	C7	P5.2	
45	D6	P5.3	
44	C6	P5.4	
30	C5	P5.5	
28	D5	P5.6	
27	C4	P5.7	
24	C3	P6.0	General-Purpose I/O, Port 6.0. Most port pins have multiple special functions. See Table 1 for details.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
ANALOG INPUT PINS			
35	A4	AIN0	ADC Input 0. 5V-tolerant input.
37	A5	AIN1	ADC Input 1. 5V-tolerant input.
39	A6	AIN2	ADC Input 2
41	A7	AIN3	ADC Input 3
NO CONNECTS			
1, 13, 25, 26, 32, 43, 50–54, 57, 66, 75–78, 87, 98, 100	A1, A9, J1, J9	N.C.	No Connection

Table 1. MAX32620/MAX32621 GPIO Special Function Cross Reference

GPIO	PRIMARY FUNCTION	SECONDARY FUNCTION	PULSE TRAIN OUTPUT	TIMER INPUT	GPIO OUTPUT	TERTIARY FUNCTION	QUATERNARY FUNCTION
P0.0	UART0A_RX	UART0B_TX	PT_PT0	TIMER_TMR0	GPIO_INT(P0)		
P0.1	UART0A_TX	UART0B_RX	PT_PT1	TIMER_TMR1	GPIO_INT(P0)		
P0.2	UART0A_CTS	UART0B_RTS	PT_PT2	TIMER_TMR2	GPIO_INT(P0)		
P0.3	UART0A_RTS	UART0B_CTS	PT_PT3	TIMER_TMR3	GPIO_INT(P0)		
P0.4	SPIM0_SCK		PT_PT4	TIMER_TMR4	GPIO_INT(P0)		
P0.5	SPIM0_MOSI/ SDIO0		PT_PT5	TIMER_TMR5	GPIO_INT(P0)		
P0.6	SPIM0_MISO/ SDIO1		PT_PT6	TIMER_TMR0	GPIO_INT(P0)		
P0.7	SPIM0_SS0		PT_PT7	TIMER_TMR1	GPIO_INT(P0)		
P1.0	SPIM1_SCK	SPIX_SCK	PT_PT8	TIMER_TMR2	GPIO_INT(P1)		
P1.1	SPIM1_MOSI/ SDIO0	SPIX_SDIO0	PT_PT9	TIMER_TMR3	GPIO_INT(P1)		
P1.2	SPIM1_MISO/ SDIO1	SPIX_SDIO1	PT_PT10	TIMER_TMR4	GPIO_INT(P1)		
P1.3	SPIM1_SS0	SPIX_SS	PT_PT11	TIMER_TMR5	GPIO_INT(P1)		
P1.4	SPIM1_SDIO2	SPIX_SDIO2	PT_PT12	TIMER_TMR0	GPIO_INT(P1)		
P1.5	SPIM1_SDIO3	SPIX_SDIO3	PT_PT13	TIMER_TMR1	GPIO_INT(P1)		
P1.6	I2CM0/SA_SDA		PT_PT14	TIMER_TMR2	GPIO_INT(P1)		
P1.7	I2CM0/SA_SCL		PT_PT15	TIMER_TMR3	GPIO_INT(P1)		
P2.0	UART1A_RX	UART1B_TX	PT_PT0	TIMER_TMR4	GPIO_INT(P2)		
P2.1	UART1A_TX	UART1B_RX	PT_PT1	TIMER_TMR5	GPIO_INT(P2)		

MAX32620/MAX32621 Detailed Description

The MAX32620/MAX32621 is a low-power, mixed signal microcontroller that includes the ARM Cortex-M4 with FPU core with a maximum operating frequency of 96MHz. An internal 4MHz oscillator supports minimal power consumption for applications requiring always-on monitoring. The MAX32621 is a secure version, incorporating a trust protection unit (TPU) with encryption and advanced security features.

Application code executes from an onboard 2MB/1MB program flash memory, with 256KB SRAM available for general application use. An 8KB instruction cache improves execution throughput, and a transparent code scrambling scheme protects customer intellectual property residing in the program flash memory. Additionally, a SPI execute in place (SPIX) external memory interface allows application code and data (up to 16MB) to be accessed from an external SPI memory device.

A 10-bit sigma-delta ADC is provided with a multiplexer front end for four external input channels (two of which are 5.5V tolerant) and internal channels to monitor supply voltages. Built-in limit monitors allow converted input samples to be compared against user-configurable high and low limits, with an option to trigger an interrupt and wake the CPU from a low power mode if attention is required.

A wide variety of communications and interface peripherals are provided, including a USB 2.0-compliant slave interface, three master SPI interfaces, four UART interfaces with multidrop support, three master I^2C interfaces, and a slave I^2C interface.

ARM Cortex-M4 with FPU Core

The ARM Cortex-M4 with FPU core is ideal for the emerging category of wearable medical and wellness applications. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

- Floating Point Unit (FPU)
- Memory Protection Unit
- Full debug support level
  - Debug Access Port (DAP)
  - Breakpoints
  - DWT
  - Flash patch
  - Halting debug
- Debug access port : JTAG or serial wire
- NVIC support
  - 52 interrupts to be grouped by firmware into 8 levels of priority
- DSP supports Single Instruction Multiple Data (SIMD) Path DSP extensions, providing:
  - 4 parallel 8 bit add/sub
  - 2 parallel 16 bit add/sub
  - 2 parallel MACs
  - 32 or 64 bit accumulate
  - Signed, unsigned, data with or without saturation

Power Operating Modes

Low Power Mode 0 (LP0)

This mode places the core and peripheral logic in a static, low-power state. All features of the device are disabled except:

- Power sequencer
- RTC (if enabled)
- Key data retention registers
- Power-on reset
- Voltage supply monitoring

Data retention in this mode can be maintained using only the V_{RTC} supply, with all other voltage supplies disabled.

Low Power Mode 1 (LP1)

This mode places the core logic in a static, low-power state which supports a fast wakeup feature. Data retention in this mode can be maintained using only the V_{RTC} supply, with all other voltage supplies disabled.

Low Power Mode 2 (LP2)

This configuration allows the ADC and some peripherals to operate while the ARM core is in sleep mode. The peripheral management unit provides intelligent, dynamic clocking of any enabled peripherals, ensuring the lowest power consumption possible.

Low Power Mode 3 (LP3)

During this state, the CPU is executing application code and all digital and analog peripherals are fully powered and awake. Dynamic clocking disables peripherals not in use, providing the optimal mix of high-performance and low power consumption.

Analog to Digital Converter (ADC)

The 10-bit sigma-delta ADC provides 4 external inputs and can also be configured to measure all internal power supplies. It operates at a maximum of 7.8ksps. AIN0 and AIN1 are 5.5V tolerant, making them suitable for monitoring batteries.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low-power mode.

The ADC reference can be the internal 1.2V bandgap or an external reference.

The ADC measures:

- AIN[3:2] (up to 3.3V)
- AIN[1:0] (up to 5.5V)
- V_{DD12}
- V_{DD18}
- V_{DDB}
- V_{RTC}
- V_{DDIO}
- V_{DDIOH}

Pulse Train Engine

Sixteen independent pulse train generators provide either a square wave or a repeating pattern from 2 bits to 32 bits in length.

Each pulse train generator is independently configurable. The pulse train generators provide the following:

- Independently enabled
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Multiple repetition options for pulse train mode
  - Single shot (nonrepeating pattern of 2-32 bits)
  - Pattern repeats user-configurable number of times or indefinitely
  - End of one pulse train's loop count can restart one or more other pulse trains

Clocking Scheme

The high-frequency internal relaxation oscillator operates at a nominal frequency of 96MHz. It is the primary clock source for the digital logic and peripherals. The 4MHz internal oscillator can be selected to optimize active power consumption. Wakeup is possible from either the 4MHz or the 96MHz internal oscillator.

An external 32.768kHz timebase is required when using the RTC or USB features of the device. The time base can be generated by attaching a 32kHz crystal. An external clock source can also be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the EC table.

Interrupt Sources

The ARM nested vector interrupt controller (NVIC) provides high speed, deterministic interrupt response, interrupt masking, and multiple interrupt sources. Each peripheral is connected to the NVIC and can have multiple interrupt flags to indicate the specific source of the interrupt within the peripheral.

The NVIC provides:

- Up to 52 distinct interrupt sources (including internal and external interrupts)
- Eight priority levels
- A dedicated interrupt for each port

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The time base can be generated by connecting a 32kHz crystal between 32KIN and 32KOUT or an external clock source can be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the EC table. The 32kHz output can be directed to a GPIO for observation and use.

The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode.

The wake-up timer allows the device to remain in low power mode for extended periods of time. The minimum wake-up interval is 244µs.

General Purpose I/O and Special Function Pins

General-purpose I/O (GPIO) pins are controlled directly by firmware or one or more peripheral modules connected to that pin. GPIO are logically divided into 8-pin ports. Each 8-bit port provides a dedicated interrupt.

The alternate functions for each pin are shown in Table 1.

The following features are independently configurable for each GPIO pin:

- GPIO or special function mode operation
- V_{DDIO} or V_{DDIOH} supply voltage
- V_{DDI18} GPIO supply voltage supported for legacy operation
- Normal and fast output drive strength
- Open-drain output or high-impedance input
- Configurable strong or weak internal pullup/pulldown resistors
- Simple output-only functions
  - Output from pulse trains (0 through 15)
  - Output from timers running in 32-bit mode

Some peripherals have optional pin assignments, allowing for greater flexibility during PCB layout. These optional pin assignments are identified with the letter B, C, or D after the peripheral name. On the MAX32620/MAX32621, the UART0_RX signal is mapped to the P0.0 pin. If the B configuration is chosen, the UART0_RX signal is mapped to the P0.1 pin.

CRC Module

The CRC hardware module provides fast calculations and data integrity checks by application software. The CRC module supports both the CRC-16-CCITT and CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$)polynomials.

Watchdog Timers

Two independent watchdog timers (WDT0 and WDT1) with window support are provided. The WDT has multiple clock source options to ensure system security. It uses a 32-bit timer with prescaler to generate the watchdog reset. When enabled, the WDT must be reset prior to timeout or within a window of time if window mode is enabled. Failure to reset the WDT during the programmed timing window results in a watchdog timeout. WDT resets can cause firmware or power-on resets. The WDT0 or WDT1 flags are set on reset if a watchdog expiration caused the system reset. The clock source options for the WDT include:

- Scaled-system clock
- RTC clock
- Power management clock

A third watchdog timer (WDT2) is provided for recovery from runaway code or system unresponsiveness. When enabled, this watchdog must be reset prior to timeout, resulting in a watchdog timeout. The WDT2 flag is set on reset if a watchdog expiration caused the system reset.

WDT2 is unique in that is in the always-on domain, and continues to run even in LP1 or LP0. The timeout period for WDT2 can be programmed as long as 8 seconds. The granularity of the timeout period is intended only for system recovery.

Programmable Timers

Six 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals. Each timer can be split into 2 16-bit timers, enabling 12 standard 16-bit timers.

32-bit timer features:

- 32-bit up/down auto-reload
- Programmable 16-bit prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External input pin for timer input, clock gating or capture, limited to an input frequency of ¼ of the peripheral clock frequency
- Timer output pin
- Configurable as 2x 16-bit general purpose timers
- Timer interrupt

Serial Peripherals

USB Controller

The integrated USB controller is compliant with the full-speed (12Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator allows for smart switching between the main supply and V_{DDB} when connected to a USB host controller.

The USB controller supports DMA for the endpoint buffers. A total of 7 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

1-Wire Master

Maxim's DeepCover® 1-Wire security solutions provide a cost-effective solution to authenticate medical sensors and peripherals, preventing counterfeit products. The integrated 1-Wire master communicates with slave devices via the bidirectional, multidrop 1-Wire bus. All of the devices on the 1-Wire bus share one signal which carries data communication and also supplies power to the slave devices. The single contact serial interface is ideal for communication networks requiring minimal interconnect. Features of the 1-Wire bus include:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Power is distributed to all slave device (parasitic power)
- Multiple device capability on a single line
- Supports 1-Wire standard (15.6kbps) and overdrive (110 kbps) speeds

The incorporation of the 1-Wire master enables the creation of 1-Wire enhanced of consumable and reusable accessories. The following benefits can be added to products by the addition of only one contact:

- OEM authenticity is verifiable with SHA-256 and ECDSA
- External tracking is eliminated because calibration data can be securely stored within accessory
- Reuse of single-use accessories can be prevented
- Counterfeit products can be identified and use denied using the unique, factory identifier
- Environmental temperature and humidity sensing

Trust Protection Unit (TPU) (MAX32621 Only)

The TPU enhances cryptographic data security for valuable intellectual property (IP) and data. A high-speed, dedicated, hardware-based math accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms including:

- AES-128
- AES-192
- AES-256
- 1024-bit DSA
- 2048-bit (CRT)

The device provides a pseudo-random number generator which can be used to create cryptographic keys for any application. A user-selectable entropy source further increases the randomness and key strength.

The secure bootloader protects against unauthorized access to program memory.

DeepCover is a registered trademark of Maixm Integrated Products, Inc.

Peripheral Management Unit (PMU)

The PMU is a DMA-based link list processing engine that performs operations and data transfers involving memory and/or peripherals in the advanced peripheral bus (APB) and advanced high-performance bus (AHB) peripheral memory space while the main CPU is in a sleep state. This allows low-overhead peripheral operations to be performed without the CPU, significantly reducing overall power consumption. Using the PMU with the CPU in a sleep state provides a lower-noise environment critical for obtaining optimum ADC performance.

Key features of the PMU engine include:

- Six independent channels with round-robin scheduling allows for multiple parallel operations
- Programmed using SRAM-based PMU opcodes
- PMU action can be initiated from interrupt conditions from peripherals without CPU
- Integrated AHB bus master
- Coprocessor-like state machine

Additional Documentation

Engineers must have the following documents to fully use this device:

- This data sheet, containing pin descriptions, feature overviews, and electrical specifications
- The device-appropriate user guide, containing detailed information and programming guidelines for core features and peripherals
- Errata sheets for specific revisions noting deviations from published specifications.

For information regarding these documents, visit Technical Support at **support.maximintegrated.com/micro**.

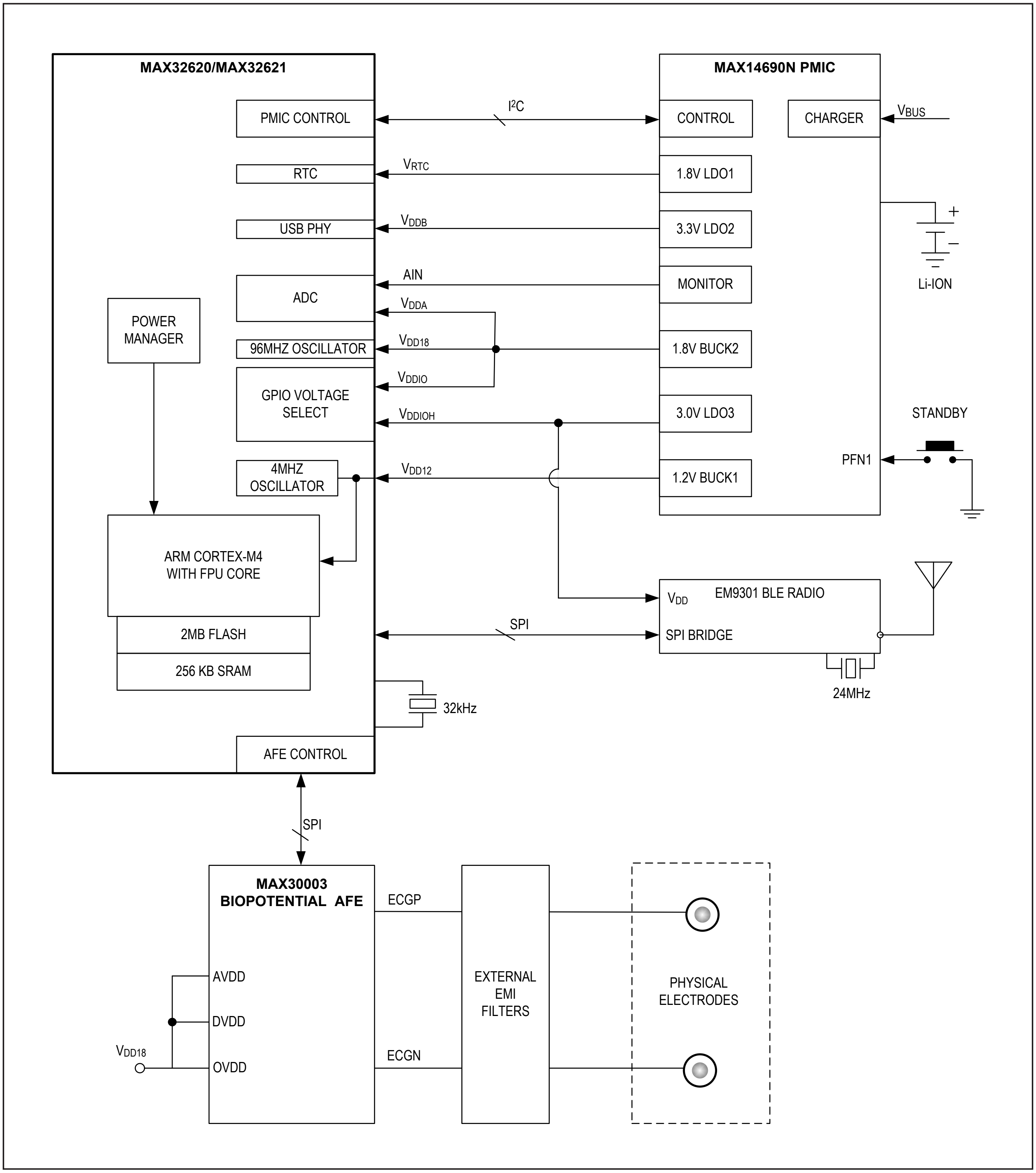
Development and Technical Support

Contact technical support for information about highly versatile, affordable development tools, available from Maxim Integrated and third-party vendors.

- Evaluation kits
- Software development kit
- Compilers
- Integrated development environments (IDEs)
- USB interface modules for programming and debugging

For technical support, go to **support.maximintegrated.com/micro**.

Typical Application Circuit—Wearable Cardiac Monitor



Ordering Information

PART	FLASH (MB)	SRAM (KB)	TRUST PROTECTION UNIT	PIN-PACKAGE
MAX32620ICQ+	2	256	No	100 TQFP
MAX32620IWG+	2	256	No	81 WLP
MAX32620IWG+T	2	256	No	81 WLP
MAX32620IWGL+*	1	256	No	81 WLP
MAX32620IWGL+T*	1	256	No	81 WLP
MAX32621ICQ+	2	256	Yes	100 TQFP
MAX32621IWG+	2	256	Yes	81 WLP
MAX32621IWG+T	2	256	Yes	81 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
81 WLP	W813D3+1	**21-0776**	Refer to **Application Note 1891**
100 TQFP-EP	C100E+3	**21-0116**	**90-0154**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—
1	1/17	Added 4MHz clock option to EC table, added new GPIO V_{DDIO}/V_{DDIOH} option while supporting legacy V_{DD18} I/O supply to EC table, pin configuration, and pin description, absolute maximum rating for V_{RTC} changed from 3.6V to 1.89V, $V_{AIN(MIN)}$ typo corrected from V_{SS} to V_{SSA}, $\overline{\text{RSTN}}$ pin supply corrected from V_{DD18} to V_{RTC}, added I^2C and SPI timings, updated feature descriptions to conform to MAX32625/MAX32626 style, corrected Table 1 title, corrected part number in detailed description, added text in General Description describing differences between “C” and “A” revisions of the device, corrected RTC frequency to 32.768kHz, changed instances of WTD to WDT, corrected instances of T_A = +20°C to T_A = +25°C, changed page 1 typical values from current to power, updated I_{DDxx} typical values, removed redundant feature list on page 26, removed references to SPI bridge from I/O Matrix as the feature was never implemented, recommended V_{DD12} bypass capacitor changed from 100nF to 1.0µF, corrected ARM Cortex trademark usage in text and figures, IIH3V min/max from ±1 to ±2, $V_{RST(MIN)}$ from 1.62V to 1.61V, f_{INTCLK} min/max from 94.08/97.92 to 94/98MHz, corrected $f_{RCCLK(MIN)}$ from 3.9 to 0.001MHz to clarify effect of clock divider option, but no change to device, moved 1-Wire Master I/O to Table 1, added MAX32620IWGL+ and MAX32620IWGL+T part numbers	1–8, 10–16, 18–26