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What is "[Embedded - Microcontrollers](#)"?

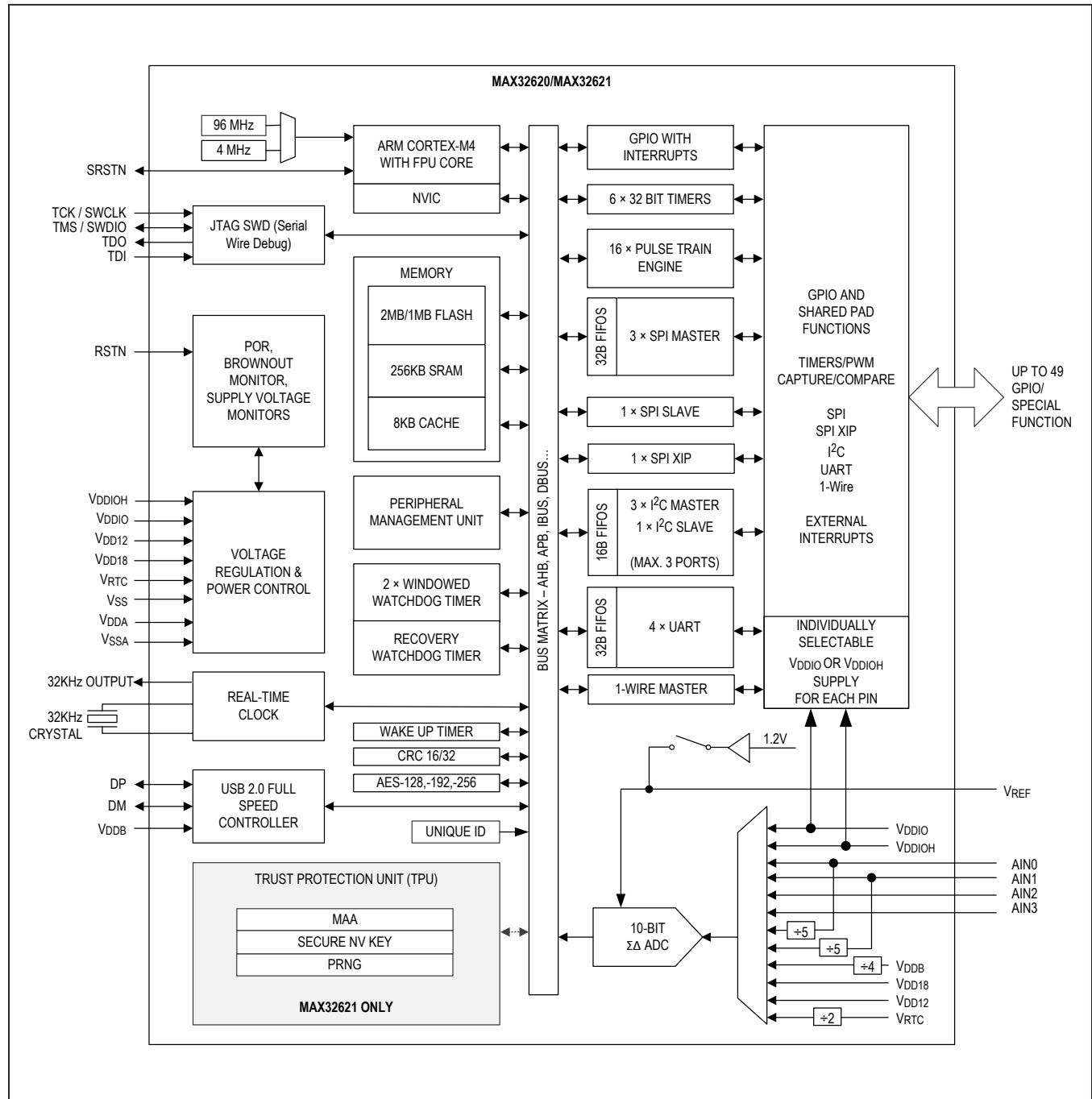
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	96MHz
Connectivity	1-Wire, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	49
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	81-WFBGA, WLBGA
Supplier Device Package	81-WLP (3.95x4.11)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/max32620iwgc-t

MAX32620/MAX32621 Block Diagram



Absolute Maximum Ratings

(All voltages with respect to V_{SS} , unless otherwise noted.)

V_{DD18}-0.3V to +1.89V	V_{DDIOH}-0.3V to +3.6V
V_{DD12}-0.3V to +1.26V	Total current V_{DD18} , $V_{DDIO}(\text{sink})$100mA
V_{DDA} with respect to V_{SSA}-0.3V to +1.89V	Total current V_{SS}100mA
V_{RTC}-0.3V to +1.89V	Output current (sink) by Any I/O pin25mA
V_{DDB}-0.3V to +3.6V	Output current (source) by Any I/O pin-25mA
V_{REF}-0.3V to +3.6V	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
32KIN, 32KOUT-0.3V to +3.6V	TQFP (multilayer board)	
RSTN, SRSTN, GPIO, DP, DM, JTAG-0.3V to +3.6V	(derate 45.5mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)3636.4mW
AIN[1:0]-0.3V to +5.5V	Operating Temperature Range -30°C to $+85^\circ\text{C}$
AIN[3:2]-0.3V to +3.6V	Storage Temperature Range -65°C to $+150^\circ\text{C}$
V_{DDIO}-0.3V to +3.6V	Soldering Temperature (reflow) $+260^\circ\text{C}$

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Package Thermal Characteristics (Note 1)

TQFP

Junction-to-Ambient Thermal Resistance (θ_{JA})22 $^\circ\text{C}/\text{W}$

Junction-to-Case Thermal Resistance (θ_{JC})2 $^\circ\text{C}/\text{W}$

WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})36 $^\circ\text{C}/\text{W}$

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Limits are tested at $T_A = +25^\circ\text{C}$ and $T_A = +85^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD18}		1.71	1.8	1.89	V
	V_{DD12}		1.14	1.2	1.26	
	V_{DDA}		1.71	1.8	1.89	
	V_{RTC}		1.71	1.8	1.89	
	V_{DDB}		3.04	3.3	3.60	
	V_{DDIO}		1.71	1.8	3.60	
	V_{DDIOH}	V_{DDIOH} must be $\geq V_{DDIO}$	1.71	1.8	3.60	
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD18}	1.1		1.70	V
Power On Reset Voltage	V_{POR}	Monitors V_{DD18}		1.5		V
RAM Data Retention Voltage	V_{DRV}	V_{DD12} supply, retention in LP1		0.93		V
V_{DD12} Dynamic Current, LP3 Mode	I_{DD12_DLP3}	Measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current, PMU disabled		102		$\mu\text{A}/\text{MHz}$

Electrical Characteristics (continued)

(Limits are tested at $T_A = +25^{\circ}\text{C}$ and $T_A = +85^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD12} Current, LP3 Mode	I_{DD12_LP3}	96MHz oscillator selected as system clock, measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current		96		μA
		4MHz oscillator selected as system clock measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current		49		
V_{DD18} Current, LP3 Mode	I_{DD18_LP3}	96MHz oscillator selected as system clock, measured on the V_{DD18} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current		366		μA
		4MHz oscillator selected as system clock, measured on the V_{DD18} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current.		33		
V_{RTC} Current, LP3 Mode	I_{RTC_LP3}	RTC disabled		1.15		μA
		RTC enabled		1.55		μA
V_{DD12} Dynamic Current, LP2 Mode	I_{DD12_DLP2}	Measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active		23		$\mu\text{A}/\text{MHz}$
V_{DD12} Current, LP2 Mode	I_{DD12_LP2}	96MHz oscillator selected as system clock, measured on the V_{DD12} pin, ARM in sleep mode, system clock stopped		96		μA
		4MHz oscillator selected as system clock, measured on the V_{DD12} pin, ARM in sleep mode, system clock stopped		49		
V_{DD18} Current, LP2 Mode	I_{DD18_LP2}	96MHz oscillator selected as system clock, ARM in sleep mode, PMU with two channels active, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current		366		μA
		4MHz oscillator selected as system clock, ARM in sleep mode, PMU with two channels active, all inputs are tied to V_{SS} or V_{DDIO} , outputs do not source/sink any current		33		
V_{RTC} Current, LP2 Mode	I_{RTC_LP2}	RTC disabled		1.15		μA
		RTC enabled		1.55		μA

Electrical Characteristics (continued)

(Limits are tested at $T_A = +25^\circ\text{C}$ and $T_A = +85^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage for $\overline{\text{SRSTN}}$, and All Port Pins	V_{IH}	Legacy V_{DD18} I/O supply, includes JTAG	$0.7 \times V_{DD18}$			V
		V_{DDIO} selected as I/O supply, includes JTAG	$0.7 \times V_{DDIO}$			
		V_{DDIOH} selected as I/O supply	$0.7 \times V_{DDIOH}$			
Input High Voltage for $\overline{\text{RSTN}}$	V_{IH}	Legacy V_{DD18} I/O supply	$0.7 \times V_{RTC}$			V
		V_{DDIO} or V_{DDIOH} selected as I/O supply	$0.7 \times V_{RTC}$			
Input Hysteresis (Schmitt)	V_{IHYS}			100		mV
Output Low Voltage for All Port Pins	V_{OL}	$I_{OL} = 4\text{mA}$ (normal drive), legacy V_{DD18} I/O supply, includes JTAG		0.2	0.4	V
		$I_{OL} = 24\text{mA}$ (high drive), legacy V_{DD18} I/O supply, includes JTAG		0.2	0.4	
		$I_{OL} = 4\text{mA}$ (normal drive), $V_{DDIO} = V_{DDIOH} = 1.71\text{V}$, V_{DDIO} selected as I/O supply, includes JTAG		0.2	0.4	
		$I_{OL} = 24\text{mA}$ (high drive), $V_{DDIO} = V_{DDIOH} = 1.71\text{V}$, V_{DDIO} selected as I/O supply		0.2	0.4	
		$I_{OL} = 900\mu\text{A}$, $V_{DDIO} = 1.71\text{V}$, $V_{DDIOH} = 2.97\text{V}$, V_{DDIOH} selected as I/O supply		0.2	0.45	
Combined I_{OL} , All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All Port Pins	V_{OH}	$I_{OH} = -2\text{mA}$ (normal drive), legacy V_{DD18} I/O supply, includes JTAG	$V_{DD18} - 0.4$			V
		$I_{OH} = -8\text{mA}$ (high drive), legacy V_{DD18} I/O supply, includes JTAG	$V_{DD18} - 0.4$			
		$I_{OH} = -2\text{mA}$ (normal drive), $V_{DDIO} = V_{DDIOH} = 1.7\text{V}$, V_{DDIO} selected as I/O supply, includes JTAG	$V_{DDIO} - 0.4$			
		$I_{OH} = -8\text{mA}$ (high drive), $V_{DDIO} = V_{DDIOH} = 1.7\text{V}$, V_{DDIO} selected as I/O supply, includes JTAG	$V_{DDIO} - 0.4$			
		$I_{OH} = -300\mu\text{A}$, $V_{DDIOH} = 2.97\text{V}$, V_{DDIOH} selected as I/O supply	$V_{DDIO} - 0.4$			
		$I_{OH} = -2\text{mA}$, $V_{DDIO} = 1.71\text{V}$, $V_{DDIOH} = 2.97\text{V}$, V_{DDIO} selected as I/O supply	$V_{DDIO} - 0.45$			

Electrical Characteristics (continued)

(Limits are tested at $T_A = +25^\circ\text{C}$ and $T_A = +85^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined I _{OH} , All GPIO	I _{OH_TOTAL}				48	mA
Input/Output Pin Capacitance for All Port Pins	C _{IO}			3		pF
Input Leakage Current Low	I _{IL}	V _{DD18} = 1.89V, V _{IN} = 0V, internal pullup disabled, legacy V _{DD18} I/O supply	-100		+100	nA
		V _{DDIO} = 1.89V, V _{DDIOH} = 3.6V, V _{DDIOH} selected as I/O supply, V _{IN} = 0V, internal pullup disabled	-100		+100	
Input Leakage Current High	I _{IH}	V _{DD18} = 1.89V, V _{IN} = 1.89V, internal pulldown disabled, legacy V _{DD18} I/O supply	-100		+100	nA
		V _{DDIO} = 1.89V, V _{DDIOH} = 3.6V, V _{IN} = 3.6V, internal pulldown disabled, V _{DDIOH} selected as I/O supply	-100		+100	
	I _{OFF}	V _{DD18} = 0V, V _{IN} < 1.89V, legacy V _{DD18} I/O supply	-1		+1	μA
		V _{DDIO} = 0V, V _{DDIOH} = 0V, V _{DDIO} selected as I/O supply, V _{IN} < 1.89V	-1		+1	
	I _{IH3V}	V _{DD18} = 1.71V, V _{IN} = 3.60V, legacy V _{DD18} I/O supply	-2		+2	μA
		V _{DDIO} = V _{DDIOH} = 1.71V, V _{DDIO} selected as I/O supply, V _{IN} =3.6V	-2		+2	
Input Pullup Resistor, $\overline{\text{SRSTN}}$, TMS, TCK, TDI	R _{PU_VDDIO}	Pullup to V _{DDIO}		25		kΩ
Input Pullup Resistor $\overline{\text{RSTN}}$	R _{PU_VRTC}	Pullup to V _{RTC}		25		kΩ
Input Pullup/Pulldown All GPIO	R _{PU_GPIO}	Normal resistance mode		25		kΩ
		Highest resistance mode		1		MΩ
FLASH MEMORY						
Page Size				8		kB
Flash Erase Time	t _{M_ERASE}	Mass erase		30		ms
	t _{P_ERASE}	Page erase		30		ms
Flash Programming Time Per Word	t _{PROG}			60		μs
Flash Endurance			10			kcycles
Data Retention	t _{RET}	T _A = +85°C	10			years

ADC Electrical Characteristics (continued)

(Limits are tested at $T_A = +25^{\circ}\text{C}$ and $T_A = +85^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	R_{AIN}	AIN[1:0], ADC_HSEL = 4–5, ADC active		45		k Ω
Input Dynamic Current, Switched Capacitance	I_{AIN}	ADC active, ADC buffer bypassed		4.5		μA
		ADC active, ADC buffer enabled		50		nA
Analog Input Capacitance	C_{AIN}	Fixed capacitance to ground		1		pF
		Dynamically switched capacitance		250		nF
Integral Nonlinearity	INL				± 2	LSb
Differential Nonlinearity	DNL				± 1	LSb
Offset Error	V_{OS}			± 1		LSb
Gain Error	GE			± 2		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		240		μA
Input Buffer Active Current	I_{INBUF}			53		μA
ADC Setup Time	t_{ADC_SU}	Any power-up of: ADC clock, ADC bias, reference buffer, or input buffer to CpuAdcStart			10	μs
		Any power-up of: ADC clock or ADC bias to CpuAdcStart			48	t_{CLK}
ADC Output Latency	t_{ADC}			1025		t_{CLK}
ADC Sample Rate	f_{ADC}				7.80	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.12	4	nA
		AIN2 or AIN3, ADC inactive or channel not selected		0.02	1.0	nA
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/gain error		± 2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.20		V
Signal to Noise Ratio	SNR			58.5		dB
Signal to Noise and Distortion	SINAD			58.5		dB
Total Harmonic Distortion	THD			-68.5		dB
Spurious Free Dynamic Range	SFDR			74		dB
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm/ $^{\circ}\text{C}$
Reference Input Capacitance	C_{REF_IN}	Dynamically switched capacitance, ADC_XREF=1, ADC active		250		fF
External Reference Voltage	V_{REF_EXT}	ADC_XREF = 1	1.17	1.23	1.29	V
Reference Dynamic Current	I_{REF_EXT}	ADC_XREF=1, ADC active		4.1		μA

Electrical Characteristics—SPI Master/SPIX Master

(Timing specifications are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Master Operating Frequency	f_{MCK}				48	MHz
Master SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High	t_{MCH}		$t_{MCK}/2$			ns
SCLK Output Pulse-Width Low	t_{MCL}		$(t_{MCK}/2) - 4$			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$(t_{MCK}/2) - 4$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$(t_{MCK}/2) - 4$			ns
MISO Input Valid to SCLK Sample Edge Setup	t_{MIS}		1			ns
MISO Input to SCLK Sample Edge	t_{MIH}				1	ns

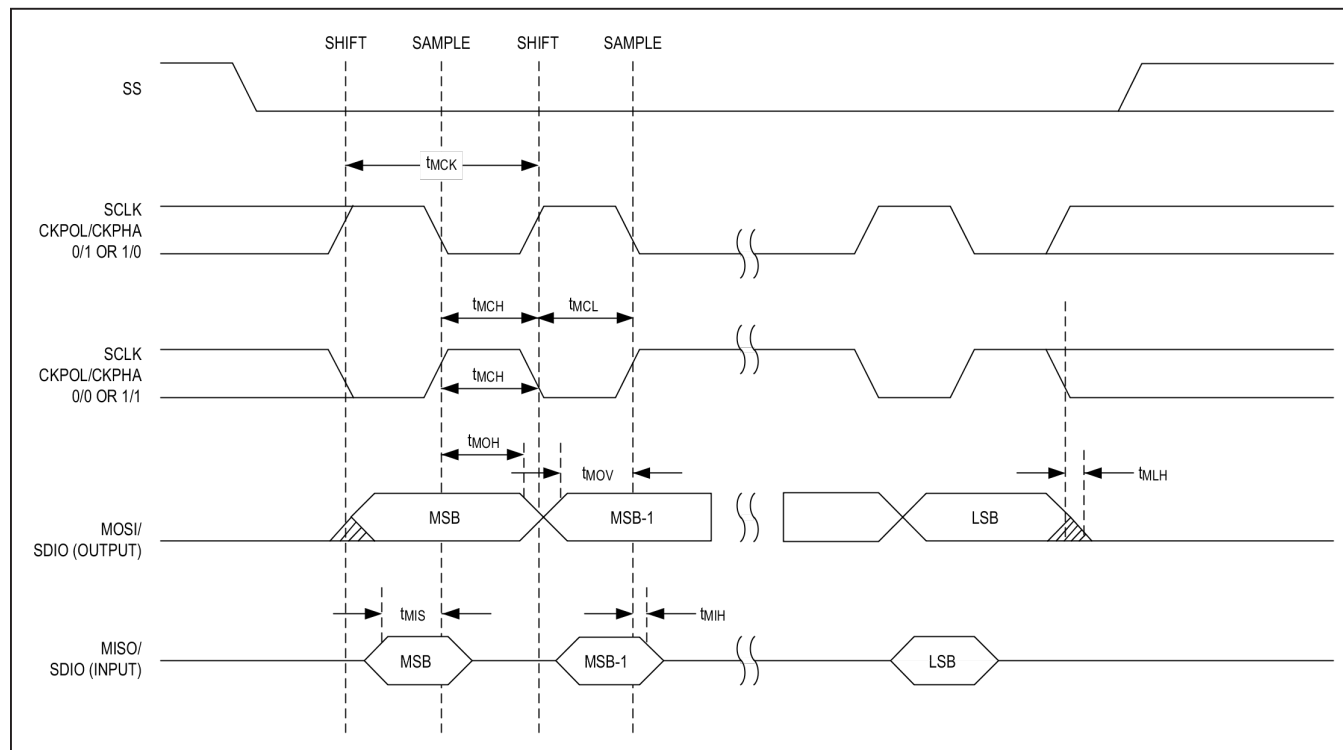


Figure 1. SPI Master and SPI XIP Master Timing

Electrical Characteristics—SPI Slave

(Timing specifications are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slave Operating Frequency, Write	$f_{\text{SCK_W}}$	Standard SPI mode			48	MHz
		Fast SPI mode			48	
Slave Operating Frequency	$f_{\text{SCK_R}}$	Standard SPI mode			22.7	MHz
		Fast SPI mode			45.5	
SCLK Period	t_{SCK}			$1/f_{\text{SCK}}$		ns

Electrical Characteristics—I²C Bus(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +85^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

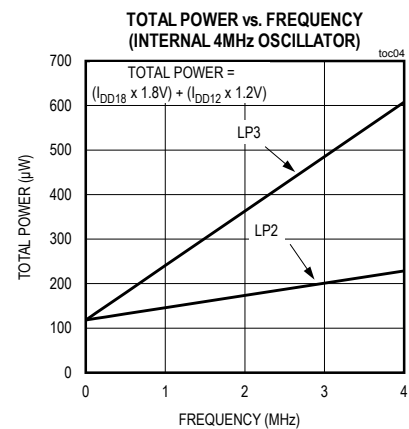
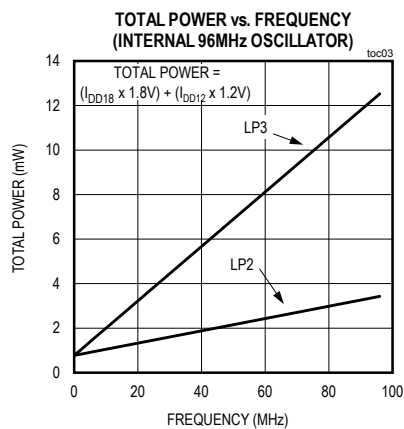
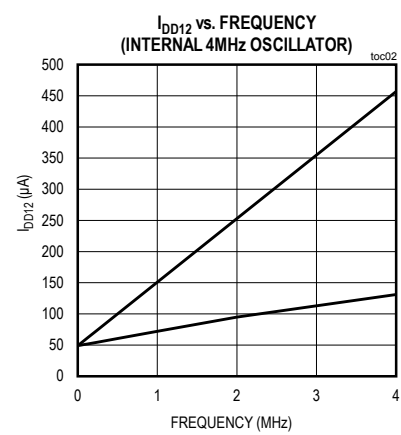
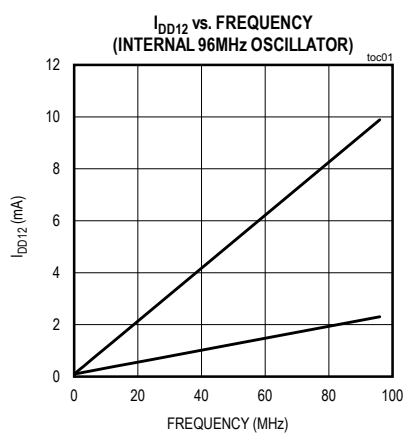
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I ² C BUS						
Input High Voltage	V _{IH_I2C}	Standard mode, V _{DDIO} selected as I/O supply	0.7 × V _{DDIO}			V
		Standard mode, V _{DDIOH} selected as I/O supply	0.7 × V _{DDIOH}			
		Fast mode, V _{DDIO} selected as I/O supply	0.7 × V _{DDIO}	V _{DDIO} + 0.5		
		Fast mode, V _{DDIOH} selected as I/O supply	0.7 × V _{DDIOH}	V _{DDIOH} + 0.5		
Input Low Voltage	V _{IL_I2C}	Standard mode, V _{DDIO} selected as I/O supply	-0.5		0.3 × V _{DDIO}	V
		Standard mode, V _{DDIOH} selected as I/O supply	-0.5		0.3 × V _{DDIOH}	
		Fast mode, V _{DDIO} selected as I/O supply	-0.5		0.3 × V _{DDIO}	
		Fast mode, V _{DDIOH} selected as I/O supply	-0.5		0.3 × V _{DDIOH}	
Input Hysteresis (Schmitt)	V _{IHYS_I2C}	Fast mode, V _{DDIO} selected as I/O supply	0.05 x V _{DDIO}			V
		Fast mode, V _{DDIOH} selected as I/O supply	0.05 x V _{DDIOH}			
Output Logic-Low (Open Drain or Open Collector)	V _{OL_I2C}	Standard mode, I _{IL} = 3mA	0		0.4	V
		Fast mode, I _{IL} = 3mA	0		0.4	
		Fast mode, I _{IL} = 2mA, V _{DDIO} selected as I/O supply	0		0.2 x V _{DDIO}	
		Fast mode, I _{IL} = 2mA, V _{DDIOH} selected as I/O supply	0		0.2 x V _{DDIOH}	
I ² C TIMING						
SCL Clock Frequency	f _{SCL}	Standard mode	0		100	kHz
		Fast mode	0		400	

MAX32620/MAX32621

High-Performance, Ultra-Low Power ARM Cortex-M4 with FPU-Based Microcontroller for Rechargeable Devices

Typical Operating Characteristics

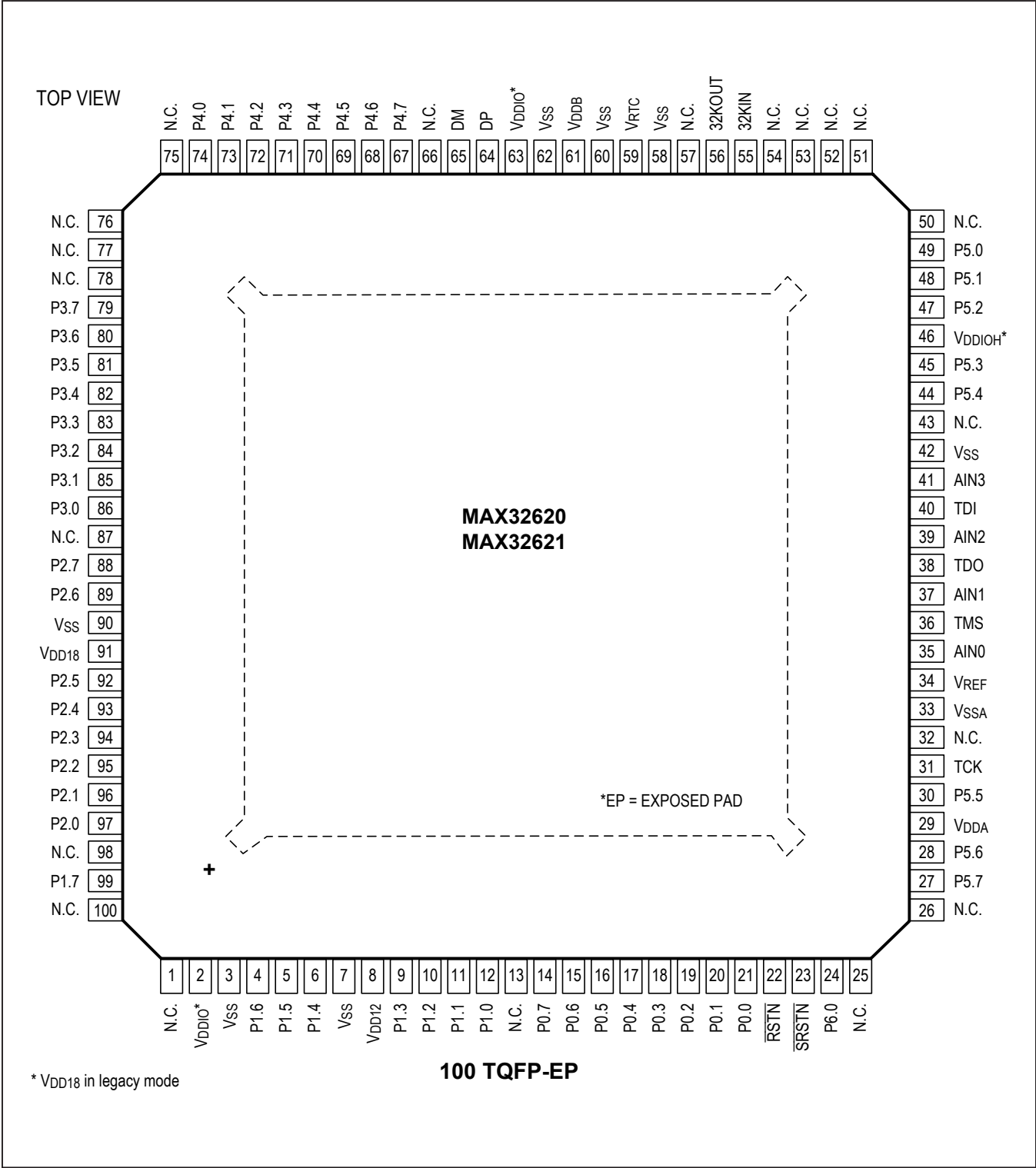
(VDD18 = 1.8V, VDD18 = 1.8V.)



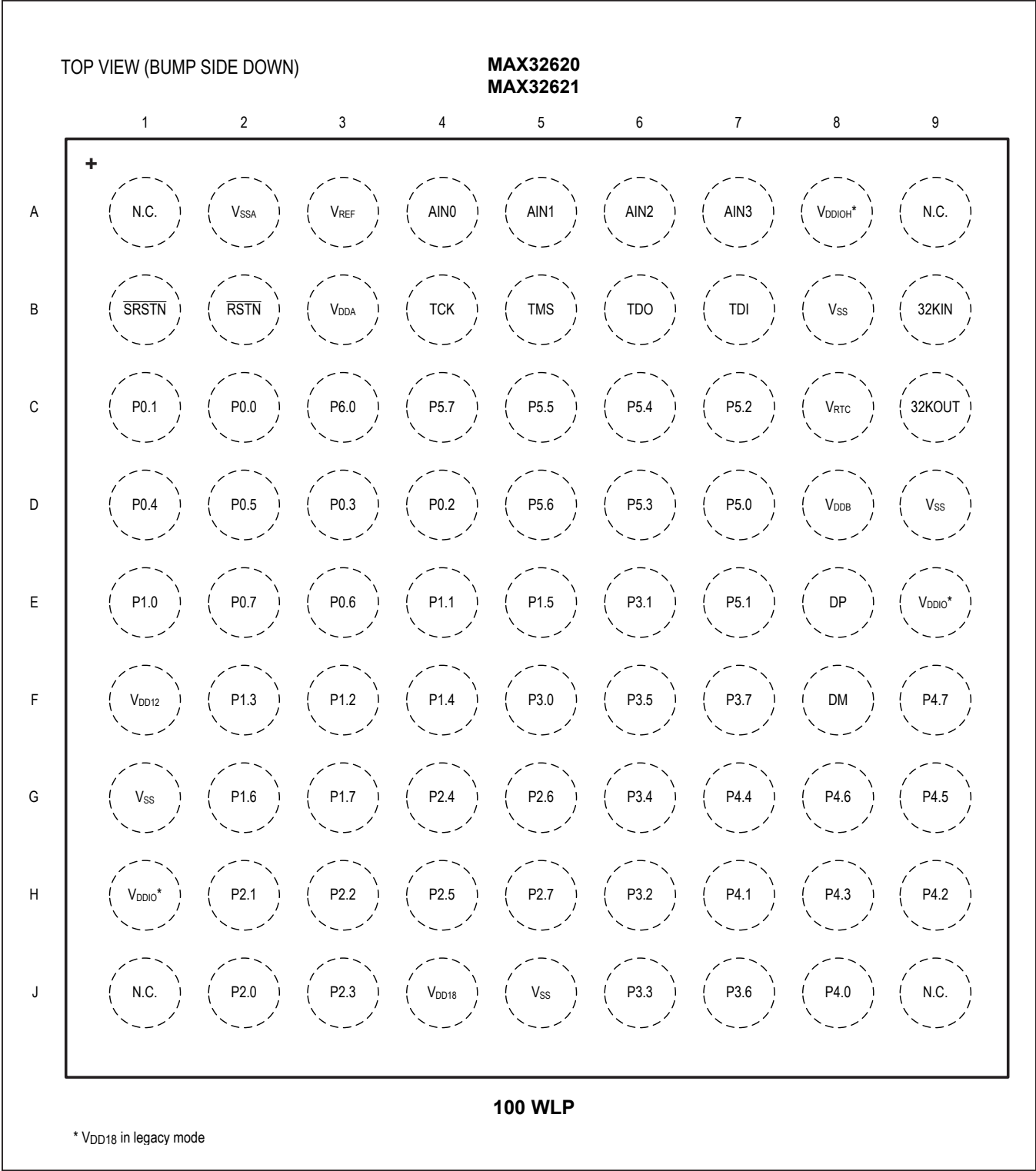
MAX32620/MAX32621

High-Performance, Ultra-Low Power ARM
Cortex-M4 with FPU-Based Microcontroller
for Rechargeable Devices

Pin Configuration



Pin Configuration (continued)



Pin Description

PIN		NAME	FUNCTION
TQFP	WLP		
POWER			
61	D8	V _{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V _{SS} with a 1.0μF capacitor as close as possible to this pin.
8	F1	V _{DD12}	1.2V Supply Voltage. This pin must be bypassed to V _{SS} with a 1.0μF capacitor as close as possible to this pin.
59	C8	V _{RTC}	RTC Supply Voltage. This pin must be bypassed to V _{SS} with a 1.0μF capacitor as close as possible to this pin.
29	B3	V _{DDA}	Analog Supply Voltage. This pin must be bypassed to V _{SSA} with a 1.0μF capacitor as close as possible to this pin.
91	J4	V _{DD18}	1.8V Supply Voltage. This pin must be bypassed to V _{SS} with a 1.0μF capacitor as close as possible to this pin.
2, 63	E9, H1	V _{DDIO}	I/O Supply Voltage. 1.8V ≤ V _{DDIO} ≤ 3.6V. See EC table for V _{DDIO} specification. This pin must be bypassed to V _{SS} with a 1.0μF capacitor as close as possible to the package. This pin can be connected to V _{DD18} for legacy I/O support.
46	A8	V _{DDIOH}	I/O Supply Voltage, High. 1.8V ≤ V _{DDIOH} ≤ 3.6V, always with V _{DDIO} ≤ V _{DDIOH} . See EC table for V _{DDIOH} specification. This pin must be bypassed to V _{SS} with a 1.0μF capacitor as close as possible to the package. This pin can be connected to V _{DD18} for legacy I/O support.
34	A3	V _{REF}	ADC Reference. This pin should be left unconnected if an external reference is not used.
3, 7, 42, 58, 60, 62, 90	B8, D9, G1, J5	V _{SS}	Digital Ground.
33	A2	V _{SSA}	Analog Ground. This pin must be connected to V _{SS} .
EP	—	EP	Exposed Pad (TQFP Only). This pad must be connected to V _{SS} . Refer to Application Note 3273: Exposed Pads: A Brief Introduction for additional information.
CLOCKS			
55	B9	32KIN	32kHz Crystal Oscillator Input/Output. Connect a 6pF 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected. A 32kHz crystal or external clock source is required for proper USB operation.
56	C9	32KOUT	
USB			
64	E8	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
65	F8	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
JTAG			
31	B4	TCK	JTAG Clock Serial Wire Debug Clock This pin has an internal 25kΩ pullup to V _{DDIO} .

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
36	B5	TMS	JTAG Test Mode Select Serial Wire Debug I/O This pin has an internal 25kΩ pullup to V _{DDIO} .
38	B6	TDO	JTAG Test Data Output
40	B7	TDI	JTAG Test Data Input. This pin has an internal 25kΩ pullup to V _{DDIO} .
RESET			
22	B2	$\overline{\text{RSTN}}$	Hardware Reset, Active-Low Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal 25kΩ pullup to the V _{RTC} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
23	B1	$\overline{\text{SRSTN}}$	Software Reset, Active-Low Input/Output. The device remains in software reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a reset to the ARM core, digital registers and peripherals (resetting most of the core logic on the V _{DD12} supply). This reset does not affect the POR only registers, RTC logic, ARM debug engine or JTAG debugger allowing for a soft reset without having to reconfiguring all registers. After the device senses $\overline{\text{SRSTN}}$ as a logic 0, the pin automatically reconfigures as an output sourcing a logic 0. The device continues to output for 6 system clock cycles and then repeats the input sensing/output driving until $\overline{\text{SRSTN}}$ is sensed inactive. This pin is internally connected with an internal 25kΩ pullup to the V _{RTC} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
GENERAL-PURPOSE I/O AND SPECIAL FUNCTIONS			
21	C2	P0.0	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 1 for details.
20	C1	P0.1	
19	D4	P0.2	
18	D3	P0.3	
17	D1	P0.4	
16	D2	P0.5	
15	E3	P0.6	
14	E2	P0.7	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 1 for details.
12	E1	P1.0	
11	E4	P1.1	
10	F3	P1.2	
9	F2	P1.3	
6	F4	P1.4	
5	E5	P1.5	
4	G2	P1.6	
99	G3	P1.7	

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
97	J2	P2.0	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 1 for details.
96	H2	P2.1	
95	H3	P2.2	
94	J3	P2.3	
93	G4	P2.4	
92	H4	P2.5	
89	G5	P2.6	
88	H5	P2.7	
86	F5	P3.0	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 1 for details.
85	E6	P3.1	
84	H6	P3.2	
83	J6	P3.3	
82	G6	P3.4	
81	F6	P3.5	
80	J7	P3.6	
79	F7	P3.7	
74	J8	P4.0	General-Purpose I/O, Port 4. Most port pins have multiple special functions. See Table 1 for details.
73	H7	P4.1	
72	H9	P4.2	
71	H8	P4.3	
70	G7	P4.4	
69	G9	P4.5	
68	G8	P4.6	
67	F9	P4.7	
49	D7	P5.0	General-Purpose I/O, Port 5. Most port pins have multiple special functions. See Table 1 for details.
48	E7	P5.1	
47	C7	P5.2	
45	D6	P5.3	
44	C6	P5.4	
30	C5	P5.5	
28	D5	P5.6	
27	C4	P5.7	
24	C3	P6.0	General-Purpose I/O, Port 6.0. Most port pins have multiple special functions. See Table 1 for details.

Table 1. MAX32620/MAX32621 GPIO Special Function Cross Reference (continued)

GPIO	SPECIAL FUNCTIONS						
P2.2	UART1A_CTS	UART1B_RTS	PT_PT2	TIMER_TMR0	GPIO_INT(P2)		
P2.3	UART1A_RTS	UART1B_CTS	PT_PT3	TIMER_TMR1	GPIO_INT(P2)		
P2.4	SPIM2A_SCK		PT_PT4	TIMER_TMR2	GPIO_INT(P2)		
P2.5	SPIM2A_MOSI/ SDIO0		PT_PT5	TIMER_TMR3	GPIO_INT(P2)		
P2.6	SPIM2A_MISO/ SDIO1		PT_PT6	TIMER_TMR4	GPIO_INT(P2)		
P2.7	SPIM2A_SS0		PT_PT7	TIMER_TMR5	GPIO_INT(P2)		
P3.0	UART2A_RX	UART2B_TX	PT_PT8	TIMER_TMR0	GPIO_INT(P3)		
P3.1	UART2A_TX	UART2B_RX	PT_PT9	TIMER_TMR1	GPIO_INT(P3)		
P3.2	UART2A_CTS	UART2B_RTS	PT_PT10	TIMER_TMR2	GPIO_INT(P3)		
P3.3	UART2A_RTS	UART2B_CTS	PT_PT11	TIMER_TMR3	GPIO_INT(P3)		
P3.4	I2CM1/SB_SDA	SPIM2A_SS1	PT_PT12	TIMER_TMR4	GPIO_INT(P3)		
P3.5	I2CM1/SB_SCL	SPIM2A_SS2	PT_PT13	TIMER_TMR5	GPIO_INT(P3)		
P3.6	SPIM1_SS1	SPIX_SS1	PT_PT14	TIMER_TMR0	GPIO_INT(P3)		
P3.7	SPIM1_SS2	SPIX_SS2	PT_PT15	TIMER_TMR1	GPIO_INT(P3)		
P4.0	OWM_I/O	SPIM2A_SR0	PT_PT0	TIMER_TMR2	GPIO_INT(P4)		
P4.1	OWM_PUPEN	SPIM2A_SR1	PT_PT1	TIMER_TMR3	GPIO_INT(P4)		
P4.2	SPIM0_SDIO2		PT_PT2	TIMER_TMR4	GPIO_INT(P4)		
P4.3	SPIM0_SDIO3		PT_PT3	TIMER_TMR5	GPIO_INT(P4)		
P4.4	SPIM0_SS1		PT_PT4	TIMER_TMR0	GPIO_INT(P4)		
P4.5	SPIM0_SS2		PT_PT5	TIMER_TMR1	GPIO_INT(P4)		
P4.6	SPIM0_SS3		PT_PT6	TIMER_TMR2	GPIO_INT(P4)		
P4.7	SPIM0_SS4		PT_PT7	TIMER_TMR3	GPIO_INT(P4)		
P5.0	Reserved	SPIM2B_SCK	PT_PT8	TIMER_TMR4	GPIO_INT(P5)		
P5.1	Reserved	SPIM2B_MOSI/ SDIO0	PT_PT9	TIMER_TMR5	GPIO_INT(P5)		
P5.2	Reserved	SPIM2B_MISO/ SDIO1	PT_PT10	TIMER_TMR0	GPIO_INT(P5)		
P5.3	Reserved	SPIM2B_SS0	PT_PT11	TIMER_TMR1	GPIO_INT(P5)	UART3A_RX	UART3B_TX
P5.4	Reserved	SPIM2B_SDIO2	PT_PT12	TIMER_TMR2	GPIO_INT(P5)	UART3A_TX	UART3B_RX
P5.5	Reserved	SPIM2B_SDIO3	PT_PT13	TIMER_TMR3	GPIO_INT(P5)	UART3A_CTS	UART3B_RTS
P5.6	Reserved	SPIM2B_SR	PT_PT14	TIMER_TMR4	GPIO_INT(P5)	UART3A_RTS	UART3B_CTS
P5.7	I2CM2/SC_SDA	SPIM2B_SS1	PT_PT15	TIMER_TMR5	GPIO_INT(P5)		
P6.0	I2CM2/SC_SCL	SPIM2B_SS2	PT_PT0	TIMER_TMR0	GPIO_INT(P5)		

Analog to Digital Converter (ADC)

The 10-bit sigma-delta ADC provides 4 external inputs and can also be configured to measure all internal power supplies. It operates at a maximum of 7.8ksps. AIN0 and AIN1 are 5.5V tolerant, making them suitable for monitoring batteries.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low-power mode.

The ADC reference can be the internal 1.2V bandgap or an external reference.

The ADC measures:

- AIN[3:2] (up to 3.3V)
- AIN[1:0] (up to 5.5V)
- V_{DD12}
- V_{DD18}
- V_{ddb}
- V_{RTC}
- V_{DDIO}
- V_{DDIOH}

Pulse Train Engine

Sixteen independent pulse train generators provide either a square wave or a repeating pattern from 2 bits to 32 bits in length.

Each pulse train generator is independently configurable. The pulse train generators provide the following:

- Independently enabled
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Multiple repetition options for pulse train mode
 - Single shot (nonrepeating pattern of 2-32 bits)
 - Pattern repeats user-configurable number of times or indefinitely
 - End of one pulse train's loop count can restart one or more other pulse trains

Clocking Scheme

The high-frequency internal relaxation oscillator operates at a nominal frequency of 96MHz. It is the primary clock source for the digital logic and peripherals. The 4MHz internal oscillator can be selected to optimize active power consumption. Wakeup is possible from either the 4MHz or the 96MHz internal oscillator.

An external 32.768kHz timebase is required when using the RTC or USB features of the device. The time base can be generated by attaching a 32kHz crystal. An external clock source can also be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the EC table.

Interrupt Sources

The ARM nested vector interrupt controller (NVIC) provides high speed, deterministic interrupt response, interrupt masking, and multiple interrupt sources. Each peripheral is connected to the NVIC and can have multiple interrupt flags to indicate the specific source of the interrupt within the peripheral.

The NVIC provides:

- Up to 52 distinct interrupt sources (including internal and external interrupts)
- Eight priority levels
- A dedicated interrupt for each port

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The time base can be generated by connecting a 32kHz crystal between 32KIN and 32KOUT or an external clock source can be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the EC table. The 32kHz output can be directed to a GPIO for observation and use.

The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode.

The wake-up timer allows the device to remain in low power mode for extended periods of time. The minimum wake-up interval is 244μs.

General Purpose I/O and Special Function Pins

General-purpose I/O (GPIO) pins are controlled directly by firmware or one or more peripheral modules connected to that pin. GPIO are logically divided into 8-pin ports. Each 8-bit port provides a dedicated interrupt.

The alternate functions for each pin are shown in [Table 1](#).

The following features are independently configurable for each GPIO pin:

- GPIO or special function mode operation
- V_{DDIO} or V_{DDIOH} supply voltage
- V_{DDI18} GPIO supply voltage supported for legacy operation
- Normal and fast output drive strength
- Open-drain output or high-impedance input
- Configurable strong or weak internal pullup/pulldown resistors
- Simple output-only functions
 - Output from pulse trains (0 through 15)
 - Output from timers running in 32-bit mode

Some peripherals have optional pin assignments, allowing for greater flexibility during PCB layout. These optional pin assignments are identified with the letter B, C, or D after the peripheral name. On the MAX32620/MAX32621, the UART0_RX signal is mapped to the P0.0 pin. If the B configuration is chosen, the UART0_RX signal is mapped to the P0.1 pin.

CRC Module

The CRC hardware module provides fast calculations and data integrity checks by application software. The CRC module supports both the CRC-16-CCITT and CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$) polynomials.

Watchdog Timers

Two independent watchdog timers (WDT0 and WDT1) with window support are provided. The WDT has multiple clock source options to ensure system security. It uses a 32-bit timer with prescaler to generate the watchdog reset. When enabled, the WDT must be reset prior to timeout or within a window of time if window mode is enabled. Failure to reset the WDT during the programmed timing window results in a watchdog timeout. WDT resets can cause firmware or power-on resets. The WDT0 or WDT1 flags are set on reset if a watchdog expiration

caused the system reset. The clock source options for the WDT include:

- Scaled-system clock
- RTC clock
- Power management clock

A third watchdog timer (WDT2) is provided for recovery from runaway code or system unresponsiveness. When enabled, this watchdog must be reset prior to timeout, resulting in a watchdog timeout. The WDT2 flag is set on reset if a watchdog expiration caused the system reset.

WDT2 is unique in that it is in the always-on domain, and continues to run even in LP1 or LP0. The timeout period for WDT2 can be programmed as long as 8 seconds. The granularity of the timeout period is intended only for system recovery.

Programmable Timers

Six 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals. Each timer can be split into 2 16-bit timers, enabling 12 standard 16-bit timers.

32-bit timer features:

- 32-bit up/down auto-reload
- Programmable 16-bit prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External input pin for timer input, clock gating or capture, limited to an input frequency of $\frac{1}{4}$ of the peripheral clock frequency
- Timer output pin
- Configurable as 2x 16-bit general purpose timers
- Timer interrupt

Serial Peripherals

USB Controller

The integrated USB controller is compliant with the full-speed (12Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator allows for smart switching between the main supply and V_{DDB} when connected to a USB host controller.

The USB controller supports DMA for the endpoint buffers. A total of 7 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

An external 32kHz crystal or clock source is required for USB operation, even if the RTC function is not used. Although the USB timing is derived from the internal 96MHz oscillator, the default accuracy is not sufficient for USB operation. Firmware trimming of the 96MHz oscillator using the 32kHz timebase as a reference is necessary to comply with USB timing requirements.

I²C Master and Slave Ports

The I²C interface is a bidirectional, 2-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium.

Three I²C interfaces allow for up to three I²C master engines and one I²C-selectable slave engine which interface to a wide variety of I²C-compatible peripherals. These engines support both Standard-mode and Fast-mode I²C standards. The slave engine shares the same I/O port as the master engines and is selectable through the I/O configuration settings. It provides the following features:

- Master or slave mode operation
- Supports standard (7-bit) or expanded (10-bit) addressing
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates:
 - Standard-mode: 100kbps
 - Fast-mode: 400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 16 bytes
- Transmitter FIFO depth of 16 bytes

Serial Peripheral Interface—Master

The SPI master-mode-only (SPIM) interface operates independently in a single or multiple slave system and is fully accessible to the user application.

The SPI ports provide a highly configurable, flexible and efficient interface to communicate with a wide variety of SPI slave devices. The three SPI master ports (SPI0, SPI1, SPI2) support the following features:

- Supports all four SPI modes (0,1,2,3) for single-bit communication
- 3 or 4 wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad I/O supported
- Up to 5 slave select lines per port

- Up to 2 slave ready lines
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- Programmable SCK alternate timing
- SS (slave select) assertion and deassertion timing with respect to leading/trailing SCK edge

Serial Peripheral Interface—Execute in Place (SPIX) Master

The SPIX allows the CPU to transparently execute instructions stored in an external SPI flash. Instructions fetched through the SPIX master are cached just like instructions fetched from internal program memory. The SPIX master can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

Serial Peripheral Interface—Slave

The SPI slave (SPIS) port provides a highly configurable, flexible, and efficient interface to communicate with a wide variety of SPI master devices. The SPI slave interface provides the following features:

- Supports SPI modes 0 and 3
- Full-duplex operation in single-bit, 4-wire mode
- Slave select polarity fixed (active low)
- Dual and Quad I/O supported
- High-speed AHB access to transmit and receive using 32-byte FIFOs
- Four interrupts to monitor FIFO levels

UART

All four universal asynchronous receiver-transmitter (UART) interfaces support full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) methodology. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 2x 32-byte send/receive FIFOs, one for transmit and receive
- Full-duplex operation for asynchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator
- Programmable 9th bit parity support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Maximum baud rate 1843.2kB

Ordering Information

PART	FLASH (MB)	SRAM (KB)	TRUST PROTECTION UNIT	PIN-PACKAGE
MAX32620ICQ+	2	256	No	100 TQFP
MAX32620IWG+	2	256	No	81 WLP
MAX32620IWG+T	2	256	No	81 WLP
MAX32620IWGL+*	1	256	No	81 WLP
MAX32620IWGL+T*	1	256	No	81 WLP
MAX32621ICQ+	2	256	Yes	100 TQFP
MAX32621IWG+	2	256	Yes	81 WLP
MAX32621IWG+T	2	256	Yes	81 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
81 WLP	W813D3+1	21-0776	Refer to Application Note 1891
100 TQFP-EP	C100E+3	21-0116	90-0154

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—
1	1/17	Added 4MHz clock option to EC table, added new GPIO V_{DDIO}/V_{DDIOH} option while supporting legacy V_{DD18} I/O supply to EC table, pin configuration, and pin description, absolute maximum rating for V_{RTC} changed from 3.6V to 1.89V, $V_{AIN(MIN)}$ typo corrected from V_{SS} to V_{SSA} , \overline{RSTN} pin supply corrected from V_{DD18} to V_{RTC} , added I ² C and SPI timings, updated feature descriptions to conform to MAX32625/MAX32626 style, corrected Table 1 title, corrected part number in detailed description, added text in General Description describing differences between “C” and “A” revisions of the device, corrected RTC frequency to 32.768kHz, changed instances of WTD to WDT, corrected instances of $T_A = +20^{\circ}\text{C}$ to $T_A = +25^{\circ}\text{C}$, changed page 1 typical values from current to power, updated I_{DDXX} typical values, removed redundant feature list on page 26, removed references to SPI bridge from I/O Matrix as the feature was never implemented, recommended V_{DD12} bypass capacitor changed from 100nF to 1.0 μF , corrected ARM Cortex trademark usage in text and figures, I ² H3V min/max from ± 1 to ± 2 , $V_{RST(MIN)}$ from 1.62V to 1.61V, f_{INTCLK} min/max from 94.08/97.92 to 94/98MHz, corrected $f_{RCCLK(MIN)}$ from 3.9 to 0.001MHz to clarify effect of clock divider option, but no change to device, moved 1-Wire Master I/O to Table 1, added MAX32620IWGL+ and MAX32620IWGL+T part numbers	1–8, 10–16, 18–26

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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