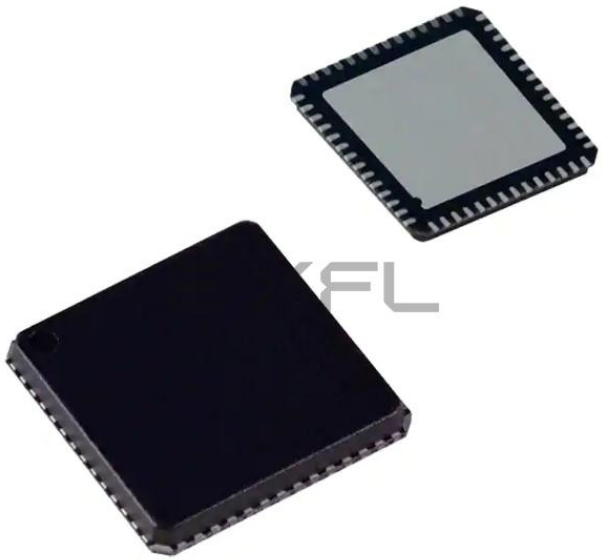

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-WFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc816bcpz-reel

ADuC816–SPECIFICATIONS[1]

Parameter	ADuC816BS	Unit	Test Conditions/Comments
LOGIC OUTPUTS (Not Including XTAL2)[2]			
V_{OH}, Output High Voltage	2.4	V min	V_{DD} = 5 V, I_{SOURCE} = 80 μA
	2.4	V min	V_{DD} = 3 V, I_{SOURCE} = 20 μA
V_{OL}, Output Low Voltage[12]	0.4	V max	I_{SINK} = 8 mA, SCLOCK, SDATA/MOSI
	0.4	V max	I_{SINK} = 10 mA, P1.0 and P1.1
	0.4	V	I_{SINK} = 1.6 mA, All Other Outputs max
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance	5	pF typ	
POWER SUPPLY MONITOR (PSM)			
AV_{DD} Trip Point Selection Range	2.63	V min	Four Trip Points Selectable in This Range
	4.63	V max	Programmed via TPA1–0 in PSMCON
AV_{DD} Power Supply Trip Point Accuracy	±3.5	% max	
DV_{DD} Trip Point Selection Range	2.63	V min	Four Trip Points Selectable in This Range
	4.63	V max	Programmed via TPD1–0 in PSMCON
DV_{DD} Power Supply Trip Point Accuracy	±3.5	% max	
WATCHDOG TIMER (WDT)			
Timeout Period	0	ms min	Nine Timeout Periods in This Range
	2000	ms max	Programmed via PRE3–0 in WDCON
MCU CORE CLOCK RATE			Clock Rate Generated via On-Chip PLL
MCU Clock Rate[2]	98.3	kHz min	Programmable via CD2–0 Bits in PLLCON SFR
	12.58	MHz max	
START-UP TIME			
At Power-On	300	ms typ	
From Idle Mode	1	ms typ	
From Power-Down Mode			
Oscillator Running			OSC_PD Bit = 0 in PLLCON SFR
Wake Up with $\overline{INT0}$ Interrupt	1	ms typ	
Wake Up with SPI/I^2C Interrupt	1	ms typ	
Wake Up with TIC Interrupt	1	ms typ	
Wake Up with External RESET	3.4	ms typ	
Oscillator Powered Down			OSC_PD Bit = 1 in PLLCON SFR
Wake Up with External RESET	0.9	sec typ	
After External RESET in Normal Mode	3.3	ms typ	
After WDT Reset in Normal Mode	3.3	ms typ	Controlled via WDCON SFR
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[13]			
Endurance[14]	100,000	Cycles min	
Data Retention[15]	100	Years min	
POWER REQUIREMENTS			DV_{DD} and AV_{DD} Can Be Set Independently
Power Supply Voltage			
AV_{DD}, 3 V Nominal Operation	2.7	V min	
	3.6	V max	
AV_{DD}, 5 V Nominal Operation	4.75	V min	
	5.25	V max	
DV_{DD}, 3 V Nominal Operation	2.7	V min	
	3.6	V max	
DV_{DD}, 5 V Nominal Operation	4.75	V min	
	5.25	V max	

Parameter	ADuC816BS	Unit	Test Conditions/Comments
POWER REQUIREMENTS (continued)			
Power Supply Currents Normal Mode[16, 17]			
DV_{DD} Current	4	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 1.57 MHz
	2.1	mA max	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 1.57 MHz
AV_{DD} Current	170	μA max	AV_{DD} = 5.25 V, Core CLK = 1.57 MHz
DV_{DD} Current	15	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 12.58 MHz
	8	mA max	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 12.58 MHz
AV_{DD} Current	170	μA max	AV_{DD} = 5.25 V, Core CLK = 12.58 MHz
Power Supply Currents Idle Mode[16, 17]			
DV_{DD} Current	1.2	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 1.57 MHz
	750	μA typ	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 1.57 MHz
AV_{DD} Current	140	μA typ	Measured @ AV_{DD} = 5.25 V, Core CLK = 1.57 MHz
DV_{DD} Current	2	mA typ	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 12.58 MHz
	1	mA typ	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 12.58 MHz
AV_{DD} Current	140	μA typ	Measured at AV_{DD} = 5.25 V, Core CLK = 12.58 MHz
Power Supply Currents Power-Down Mode[16, 17]			Core CLK = 1.57 MHz or 12.58 MHz
DV_{DD} Current	50	μA max	DV_{DD} = 4.75 V to 5.25 V, Osc. On, TIC On
	20	μA max	DV_{DD} = 2.7 V to 3.6 V, Osc. On, TIC On
AV_{DD} Current	1	μA max	Measured at AV_{DD} = 5.25 V, Osc. On or Osc. Off
DV_{DD} Current	20	μA max	DV_{DD} = 4.75 V to 5.25 V, Osc. Off
	5	μA typ	DV_{DD} = 2.7 V to 3.6 V, Osc. Off
Typical Additional Power Supply Currents (AI_{DD} and DI_{DD})			Core CLK = 1.57 MHz, AV_{DD} = DV_{DD} = 5 V
PSM Peripheral	50	μA typ	
Primary ADC	1	mA typ	
Auxiliary ADC	500	μA typ	
DAC	150	μA typ	
Dual Current Sources	400	μA typ	

NOTES

[1]Temperature Range –40°C to +85°C.

[2]These numbers are not production tested but are guaranteed by Design and/or Characterization data on production release.

[3]The primary ADC is factory-calibrated at 25°C with AV_{DD} = DV_{DD} = 5 V yielding this full-scale error. If user power supply or temperature conditions are significantly different from these, an Internal Full-Scale Calibration will restore this error to this level.

[4]Gain Error Drift is a span drift. To calculate Full-Scale Error Drift, add the Offset Error Drift to the Gain Error Drift times the full-scale input.

[5]The auxiliary ADC is factory-calibrated at 25°C with AV_{DD} = DV_{DD} = 5 V yielding this full-scale error of –2.5 LSB. A system zero-scale and full-scale calibration will remove this error altogether.

[6]DAC linearity and AC Specifications are calculated using:
reduced code range of 48 to 4095, 0 to V_{REF}
reduced code range of 48 to 3995, 0 to V_{DD}.

[7]Gain Error is a measure of the span error of the DAC.

[8]In general terms, the bipolar input voltage range to the primary ADC is given by $Range_{ADC} = \pm(V_{REF}\ 2^{RN})/125$, where:
V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected.
RN = decimal equivalent of RN2, RN1, RN0, e.g., V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0 the $Range_{ADC} = \pm 1.28$ V.
In unipolar mode the effective range is 0 V to 1.28 V in our example.

[9]1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0 and XREF1 bits in ADC0CON and ADC1CON respectively.

[10]In bipolar mode, the Auxiliary ADC can only be driven to a minimum of A_{GND} – 30 mV as indicated by the Auxiliary ADC absolute AIN voltage limits. The bipolar range is still $-V_{REF}$ to $+V_{REF}$; however, the negative voltage is limited to –30 mV.

[11]Pins configured in I²C-compatible mode or SPI mode, pins configured as digital inputs during this test.

[12]Pins configured in I²C-compatible mode only.

[13]Flash/EE Memory Reliability Characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

[14]Endurance is qualified to 100 Kcycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C and +85°C, typical endurance at 25°C is 700 Kcycles.

[15]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature as shown in Figure 27 in the Flash/EE Memory description section of this data sheet.

[16]Power Supply current consumption is measured in Normal, Idle, and Power-Down Modes under the following conditions:
Normal Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, Core Executing internal software loop.
Idle Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, PCON.0 = 1, Core Execution suspended in idle mode.
Power-Down Mode: Reset = 0.4 V, All P0 pins and P1.2–P1.7 pins = 0.4 V, All other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core Execution suspended in power-down mode, OSC turned ON or OFF via OSC_PD bit (PLLCON.7) in PLLCON SFR.

[17]DV_{DD} power supply current will typically increase by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice

TIMING SPECIFICATIONS[1, 2, 3] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter		32.768 kHz External Crystal Min	Typ	Max	Unit	Figure
CLOCK INPUT (External Clock Driven XTAL1)						
t_{CK}	XTAL1 Period		30.52		µs	1
t_{CKL}	XTAL1 Width Low		15.16		µs	1
t_{CKH}	XTAL1 Width High		15.16		µs	1
t_{CKR}	XTAL1 Rise Time		20		ns	1
t_{CKF}	XTAL1 Fall Time		20		ns	1
$1/t_{CORE}$	ADuC816 Core Clock Frequency[4]	0.098		12.58	MHz	
t_{CORE}	ADuC816 Core Clock Period[5]		0.636		µs	
t_{CYC}	ADuC816 Machine Cycle Time[6]	0.95	7.6	122.45	µs	

NOTES

[1]AC inputs during testing are driven at DV_{DD} – 0.5 V for a Logic 1, and 0.45 V for a Logic 0. Timing measurements are made at V_{IH} min for a Logic 1, and V_{IL} max for a Logic 0 as shown in Figure 2.

[2]For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 2.

[3]C_{LOAD} for Port0, ALE, $\overline{PSEN}$ outputs = 100 pF; C_{LOAD} for all other outputs = 80 pF unless otherwise noted.

[4]ADuC816 internal PLL locks onto a multiple (384 times) the external crystal frequency of 32.768 kHz to provide a Stable 12.583 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.

[5]This number is measured at the default Core_Clk operating frequency of 1.57 MHz.

[6]ADuC816 Machine Cycle Time is nominally defined as 12/Core_CLK.

Specifications subject to change without notice.

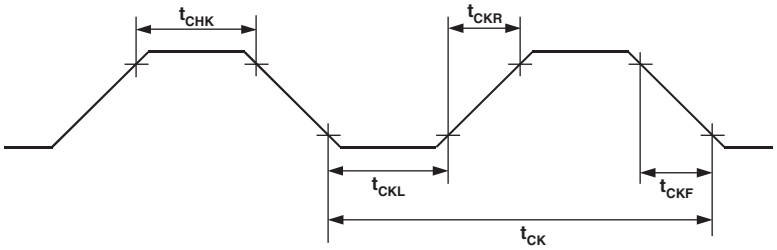


Figure 1. XTAL1 Input

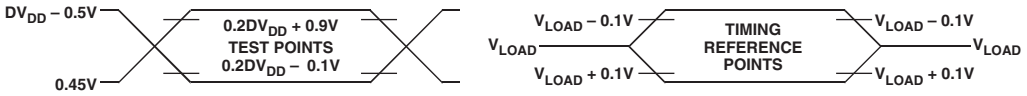


Figure 2. Timing Waveform Characteristics

Parameter		Min	Max	Unit	Figure
I^2C-COMPATIBLE INTERFACE TIMING					
t_L	SCLOCK Low Pulsewidth	4.7		μs	7
t_H	SCLOCK High Pulsewidth	4.0		μs	7
t_{SHD}	Start Condition Hold Time	0.6		μs	7
t_{DSU}	Data Setup Time	100		μs	7
t_{DHD}	Data Hold Time		0.9	μs	7
t_{RSU}	Setup Time for Repeated Start	0.6		μs	7
t_{PSU}	Stop Condition Setup Time	0.6		μs	7
t_{BUF}	Bus Free Time between a STOP Condition and a START Condition	1.3		μs	7
t_R	Rise Time of Both SCLOCK and SDATA		300	ns	7
t_F	Fall Time of Both SCLOCK and SDATA		300	ns	7
t_{SUP}*	Pulsewidth of Spike Suppressed		50	ns	7

*Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

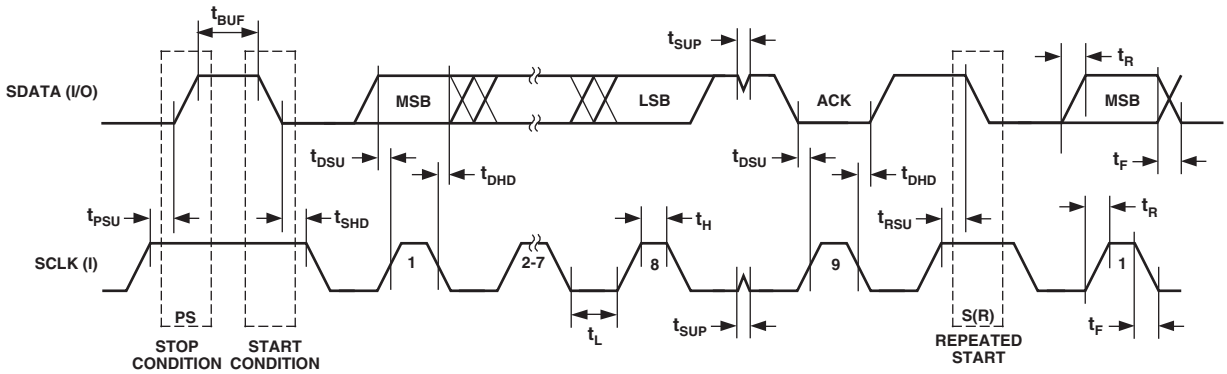


Figure 7. I^2C-Compatible Interface Timing

Parameter		Min	Typ	Max	Unit	Figure
SPI MASTER MODE TIMING (CPHA = 1)						
t_{SL}	SCLOCK Low Pulsewidth*		630		ns	8
t_{SH}	SCLOCK High Pulsewidth*		630		ns	8
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns	8
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns	8
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns	8
t_{DF}	Data Output Fall Time		10	25	ns	8
t_{DR}	Data Output Rise Time		10	25	ns	8
t_{SR}	SCLOCK Rise Time		10	25	ns	8
t_{SF}	SCLOCK Fall Time		10	25	ns	8

*Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 bits in PLLCON SFR set to 0, 1, and 1 respectively, i.e., core clock frequency = 1.57 MHz and
b. SPI bit-rate selection bits SPR1 and SPR0 bits in SPICON SFR set to 0 and 0 respectively.

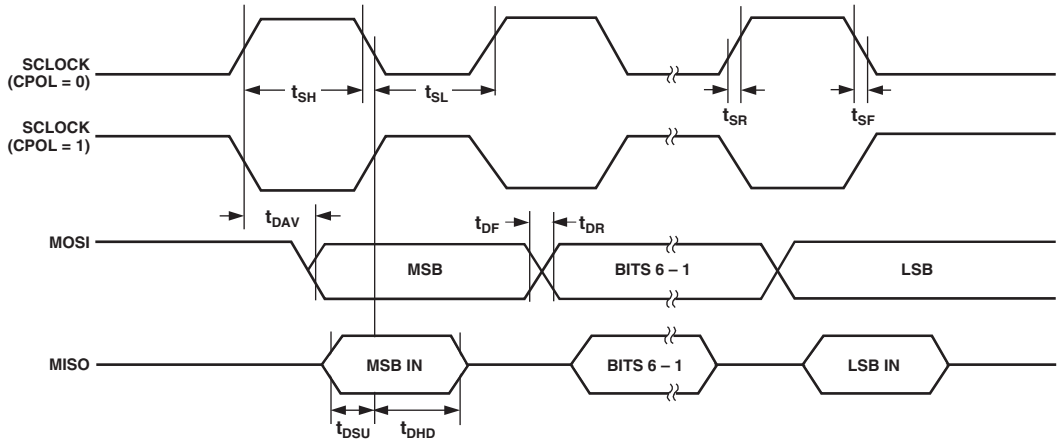


Figure 8. SPI Master Mode Timing (CPHA = 1)

Parameter		Min	Typ	Max	Unit	Figure
SPI MASTER MODE TIMING (CPHA = 0)						
t_{SL}	SCLOCK Low Pulsewidth*		630		ns	9
t_{SH}	SCLOCK High Pulsewidth*		630		ns	9
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns	9
t_{DOSU}	Data Output Setup before SCLOCK Edge			150	ns	9
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns	9
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns	9
t_{DF}	Data Output Fall Time		10	25	ns	9
t_{DR}	Data Output Rise Time		10	25	ns	9
t_{SR}	SCLOCK Rise Time		10	25	ns	9
t_{SF}	SCLOCK Fall Time		10	25	ns	9

*Characterized under the following conditions:
a. Core clock divider bits CD2, CD1 and CD0 bits in PLLCON SFR set to 0, 1, and 1 respectively, i.e., core clock frequency = 1.57 MHz and
b. SPI bit-rate selection bits SPR1 and SPR0 bits in SPICON SFR set to 0 and 0 respectively.

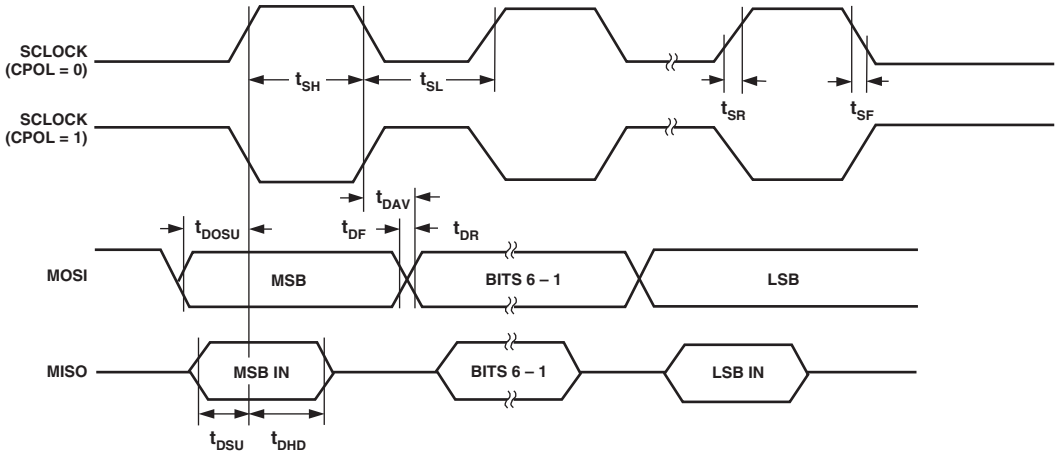


Figure 9. SPI Master Mode Timing (CPHA = 0)

Pin No. 52-Lead MQFP	Pin No. 56-Lead CSP	Mnemonic	Type[1]	Description
20, 34, 48	22, 36, 51,	DV_{DD}	S	Digital Supply, 3 V or 5 V
21, 35, 47	23, 37, 38, 50	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
26		SCLOCK	I/O	Serial Interface Clock for either the I2C or SPI Interface. As an input, this pin is a Schmitt-triggered input, and a weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be directly controlled in software as a digital output pin.
27		MOSI/SDATA	I/O	Serial Data I/O for the I^2C Interface or Master Output/Slave Input for the SPI Interface. A weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be directly controlled in software as a digital output pin.
28–31 36–39	30–33 39–42	P2.0–P2.7 (A8–A15) (A16–A23)	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the 24-bit external data memory space.
32	34	XTAL1	I	Input to the Crystal Oscillator Inverter
33	35	XTAL2	O	Output from the Crystal Oscillator Inverter. (See the ADuC816 Hardware Design Considerations section for description.)
40	43	$\overline{EA}$	I/O	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000h to F7FFh.When held low, this input enables the device to fetch all instructions from external program memory. To determine the mode of code execution, i.e., internal or external, the $\overline{EA}$ pin is sampled at the end of an external RESET assertion or as part of a device power cycle. $\overline{EA}$ may also be used as an external emulation I/O pin, and therefore the voltage level at this pin must not be changed during normal mode operation as it may cause an emulation interrupt that will halt code execution.
41	44	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. $\overline{PSEN}$ can also be used to enable Serial Download mode when pulled low through a resistor at the end of an external RESET assertion or as part of a device power cycle.
42	45	ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit data address space accesses) of the address to external memory during external code or data memory access cycles. It is activated every six oscillator periods except during an external data memory access. It can be disabled by setting the PCON.4 bit in the PCON SFR.
43–46 49–52	46–49 52–55	P0.0–P0.7 (AD0–AD3)	I/O	These pins are part of Port 0, which is an 8-bit, open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used (AD4–AD7)as high impedance inputs. An external pull-up resistor will be required on P0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s.

[1] I = Input, O = Output, S = Supply.

MEMORY ORGANIZATION

As with all 8051-compatible devices, the ADuC816 has separate address spaces for Program and Data memory as shown in Figure 13 and Figure 14.

If the user applies power or resets the device while the $\overline{EA}$ pin is pulled low, the part will execute code from the external program space, otherwise the part defaults to code execution from its internal 8 Kbyte Flash/EE program memory. This internal code space can be downloaded via the UART serial port while the device is in-circuit.

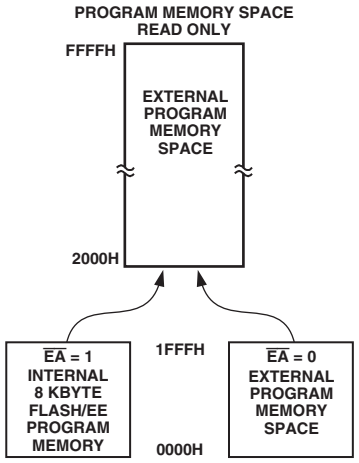


Figure 13. Program Memory Map

The data memory address space consists of internal and external memory space. The internal memory space is divided into four physically separate and distinct blocks, namely the lower 128 bytes of RAM, the upper 128 bytes of RAM, the 128 bytes of special function register (SFR) area, and a 640-byte Flash/EE Data memory. While the upper 128 bytes of RAM, and the SFR area share the same address locations, they are accessed through different address modes.

The lower 128 bytes of data memory can be accessed through direct or indirect addressing, the upper 128 bytes of RAM can be accessed through indirect addressing, and the SFR area is accessed through direct addressing.

Also, as shown in Figure 13, the additional 640 Bytes of Flash/EE Data Memory are available to the user and can be accessed indirectly via a group of control registers mapped into the Special Function Register (SFR) area. Access to the Flash/EE Data Memory is discussed in detail later as part of the Flash/EE Memory section in this data sheet.

The external data memory area can be expanded up to 16 MBytes. This is an enhancement of the 64 KByte external data memory space available on standard 8051-compatible cores.

The external data memory is discussed in more detail in the ADuC816 Hardware Design Considerations section.

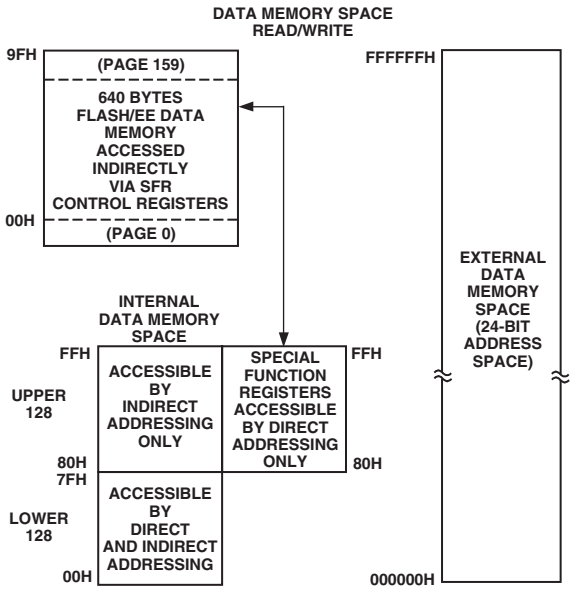


Figure 14. Data Memory Map

The lower 128 bytes of internal data memory are mapped as shown in Figure 15. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits), locations 20Hex through 2FHex above the register banks, form a block of directly addressable bit locations at bit addresses 00H through 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 256 bytes.

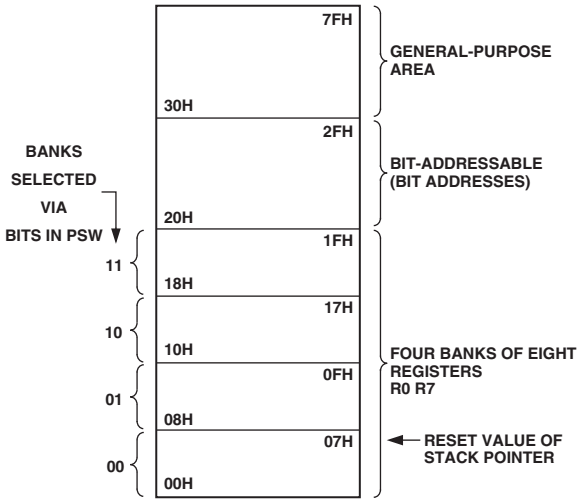


Figure 15. Lower 128 Bytes of Internal Data Memory

SPECIAL FUNCTION REGISTERS

All registers except the program counter and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

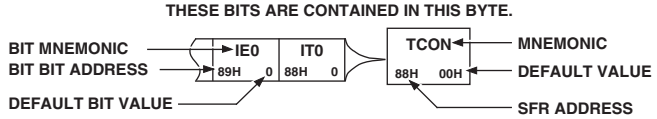
Figure 17 shows a full SFR memory map and SFR contents on RESET; NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented; i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations reserved for future use are shaded (RESERVED) and should not be accessed by user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RSI D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH	PT0 B9H 0	PX0 B8H 0	BITS
$\overline{RD}$ B7H 1	$\overline{WR}$ B6H 1	T1 B5H 1	T0 B4H 1	$\overline{INT1}$ B3H 1	$\overline{INT0}$ B2H 1	TXD B1H 1	RXD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	T1 99H 0	R1 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

SPICON F8H 04H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B F0H 00H	RESERVED	RESERVED	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON E8H 00H	RESERVED	GN0M* EAH 55H	GN0H* EBH 53H	GN1L* ECH 9AH	GN1H* EDH 59H	RESERVED	RESERVED
ACC E0H 00H	RESERVED	OF0M* E2H 00H	OF0H* E3H 80H	OF1L* E4H 00H	OF1H* E5H 80H	RESERVED	RESERVED
ADCSTAT D8H 00H	RESERVED	ADC0M DAH 00H	ADC0H DBH 00H	ADC1L DCH 00H	ADC1H DDH 00H	RESERVED	PSMCON DFH DEH
PSW D0H 00H	ADCMODE D1H 00H	ADC0CON D2H 07H	ADC1CON D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 03H
T2CON C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON C0H 10H	RESERVED	CHIPID C2H 16H	RESERVED	RESERVED	RESERVED	EADRL C6H 00H	RESERVED
IP B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3 B0H FFH	NOT USED	NOT USED	NOT USED	NOT USED	RESERVED	RESERVED	NOT USED
IE A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
P2 A0H FFH	TIMECON A1H 00H	HTHSEC A2H 00H	SEC A3H 00H	MIN A4H 00H	HOUR A5H 00H	INTVAL A6H 00H	NOT USED
SCON 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CDAT 9BH 00H	NOT USED	NOT USED	NOT USED	NOT USED
P1 90H FFH	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
TCON 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

*CALIBRATION COEFFICIENTS ARE PRECONFIGURED AT POWER-UP TO FACTORY-CALIBRATED VALUES.

SFR MAP KEY:



SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT-ADDRESSABLE.

Figure 17. Special Function Register Locations and Reset Values

ADCMODE (ADC Mode Register)
Used to control the operational mode of both ADCs.

SFR Address	D1H
Power-On Default Value	00H
Bit Addressable	No

---	---	ADC0EN	ADC1EN	---	MD2	MD1	MD0

Table IV. ADCMODE SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	---	Reserved for Future Use.
5	ADC0EN	Primary ADC Enable. *Set* by the user to enable the Primary ADC and place it in the mode selected in MD2-MD0 below *Cleared* by the user to place the Primary ADC in power-down mode.
4	ADC1EN	Auxiliary ADC Enable. *Set* by the user to enable the Auxiliary ADC and place it in the mode selected in MD2-MD0 below *Cleared* by the user to place the Auxiliary ADC in power-down mode.
3	---	Reserved for Future Use.
2	MD2	Primary and Auxiliary ADC Mode bits.
1	MD1	These bits select the operational mode of the enabled ADC as follows:
0	MD0	MD2 MD1 MD0 0 0 0 Power-Down Mode (Power-On Default) 0 0 1 Idle Mode In Idle Mode the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode In Single Conversion Mode, a single conversion is performed on the enabled ADC. On completion of the conversion, the ADC data registers (ADC0H/M and/or ADC1H/L) are updated, the relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000. 0 1 1 Continuous Conversion In continuous conversion mode the ADC data registers are regularly updated at the selected update rate (see SF register) 1 0 0 Internal Zero-Scale Calibration Internal short automatically connected to the enabled ADC(s) 1 0 1 Internal Full-Scale Calibration Internal or External V_{REF} (as determined by XREF0 and XREF1 bits in ADC0/1CON) is automatically connected to the ADC input for this calibration. 1 1 0 System Zero-Scale Calibration User should connect system zero-scale input to the ADC input pins as selected by CH1/CH0 and ACH1/ACH0 bits in the ADC0/1CON register. 1 1 1 System Full-Scale Calibration User should connect system full-scale input to the ADC input pins as selected by CH1/CH0 and ACH1/ACH0 bits in the ADC0/1CON register.

NOTES
1. Any change to the MD bits will immediately reset both ADCs. A write to the MD2–0 bits with no change is also treated as a reset. (See exception to this in Note 3 below.)
2. If ADC0CON is written when AD0EN = 1, or if AD0EN is changed from 0 to 1, then both ADCs are also immediately reset. In other words, the Primary ADC is given priority over the Auxiliary ADC and any change requested on the primary ADC is immediately responded to.
3. On the other hand, if ADC1CON is written or if ADC1EN is changed from 0 to 1, only the Auxiliary ADC is reset. For example, if the Primary ADC is continuously converting when the Auxiliary ADC change or enable occurs, the primary ADC continues undisturbed. Rather than allow the Auxiliary ADC to operate with a phase difference from the primary ADC, the Auxiliary ADC will fall into step with the outputs of the primary ADC. The result is that the first conversion time for the Auxiliary ADC will be delayed up to three outputs while the Auxiliary ADC update rate is synchronized to the Primary ADC.
4. Once ADCMODE has been written with a calibration mode, the RDY0/1 bits (ADCSTAT) are immediately reset and the calibration commences. On completion, the appropriate calibration registers are written, the relevant bits in ADCSTAT are written, and the MD2–0 bits are reset to 000 to indicate the ADC is back in power-down mode.
5. Any calibration request of the Auxiliary ADC while the temperature sensor is selected will fail to complete. Although the RDY1 bit will be set at the end of the calibration cycle, no update of the calibration SFRs will take place and the ERR1 bit will be set.
6. Calibrations are performed at maximum SF (see SF SFR) value guaranteeing optimum calibration operation.

ADC0CON (Primary ADC Control Register)

Used to configure the Primary ADC for range, channel selection, external Ref enable, and unipolar or bipolar coding.

SFR Address D2H
Power-On Default Value 07H
Bit Addressable No

---	XREF0	CH1	CH0	UNI0	RN2	RN1	RN0

Table V. ADC0CON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	XREF0	Primary ADC External Reference Select Bit. *Set* by user to enable the Primary ADC to use the external reference via REFIN(+)/REFIN(–). *Cleared* by user to enable the Primary ADC to use the internal bandgap reference (V_{REF} = 1.25 V).
5	CH1	Primary ADC Channel Selection Bits.
4	CH0	Written by the user to select the differential input pairs used by the Primary ADC as follows: CH1 CH0 Positive Input Negative Input 0 0 AIN1 AIN2 0 1 AIN3 AIN4 1 0 AIN2 AIN2 (Internal Short) 1 1 AIN3 AIN2
3	UNI0	Primary ADC Unipolar Bit. *Set* by user to enable unipolar coding, i.e., zero differential input will result in 000000 hex output. *Cleared* by user to enable bipolar coding, zero differential input will result in 800000 hex output.
2	RN2	Primary ADC Range Bits.
1	RN1	Written by the user to select the Primary ADC input range as follows:
0	RN0	RN2 RN1 RN0 Selected Primary ADC Input Range (V_{REF} = 2.5 V) 0 0 0 ±20 mV 0 0 1 ±40 mV 0 1 0 ±80 mV 0 1 1 ±160 mV 1 0 0 ±320 mV 1 0 1 ±640 mV 1 1 0 ±1.28 V 1 1 1 ±2.56 V

ICON (Current Sources Control Register)
Used to control and configure the various excitation and burnout current source options available on-chip.

SFR Address D5H
Power-On Default Value 00H
Bit Addressable No

---	BO	ADC1IC	ADC0IC	I2PIN	I1PIN	I2EN	I1EN

Table VIII. ICON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	BO	Burnout Current Enable Bit. *Set* by user to enable both transducer burnout current sources in the primary ADC signal paths. *Cleared* by user to disable both transducer burnout current sources.
5	ADC1IC	Auxiliary ADC Current Correction Bit. *Set* by user to allow scaling of the Auxiliary ADC by an internal current source calibration word.
4	ADC0IC	Primary ADC Current Correction Bit. *Set* by user to allow scaling of the Primary ADC by an internal current source calibration word.
3	I2PIN*	Current Source-2 Pin Select Bit. *Set* by user to enable current source-2 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1). *Cleared* by user to enable current source-2 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2).
2	I1PIN*	Current Source-1 Pin Select Bit. *Set* by user to enable current source-1 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2). *Cleared* by user to enable current source-1 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1).
1	I2EN	Current Source-2 Enable Bit. *Set* by user to turn on excitation current source-2 (200 μA). *Cleared* by user to turn off excitation current source-2 (200 μA).
0	I1EN	Current Source-1 Enable Bit. *Set* by user to turn on excitation current source-1 (200 μA). *Cleared* by user to turn off excitation current source-1 (200 μA).

*Both current sources can be enabled to the same external pin, yielding a 400 μA current source.

ADC0H/ADC0M (Primary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the Primary ADC.

SFR Address	ADC0H	High Data Byte	DBH
	ADC0M	Middle Data Byte	DAH
Power-On Default Value	00H	Both Registers	
Bit Addressable	No	Both Registers	

ADC1H/ADC1L (Auxiliary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the Auxiliary ADC.

SFR Address	ADC1H	High Data Byte	DDH
	ADC1L	Low Data Byte	DCH
Power-On Default Value	00H	Both Registers	
Bit Addressable	No	Both Registers	

PRIMARY AND AUXILIARY ADC CIRCUIT DESCRIPTION

OVERVIEW

The ADuC816 incorporates two independent sigma-delta ADCs (Primary and Auxiliary) with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer or temperature measurement applications.

Primary ADC

This ADC is intended to convert the primary sensor input. The input is buffered and can be programmed for one of 8 input ranges from ±20 mV to ±2.56 V being driven from one of three differential input channel options AIN1/2, AIN3/4, or AIN3/2. The input channel is internally buffered allowing the part to handle significant source impedances on the analog input, allowing R/C filtering (for noise rejection or RFI reduction) to be placed on the analog inputs if required. On-chip burnout currents can also be turned on. These currents can be used to check that a transducer on the selected channel is still operational before attempting to take measurements.

The ADC employs a sigma-delta conversion technique to realize up to 16 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc3 programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A Chopping scheme is also employed to minimize ADC offset errors. A block diagram of the Primary ADC is shown in Figure 18.

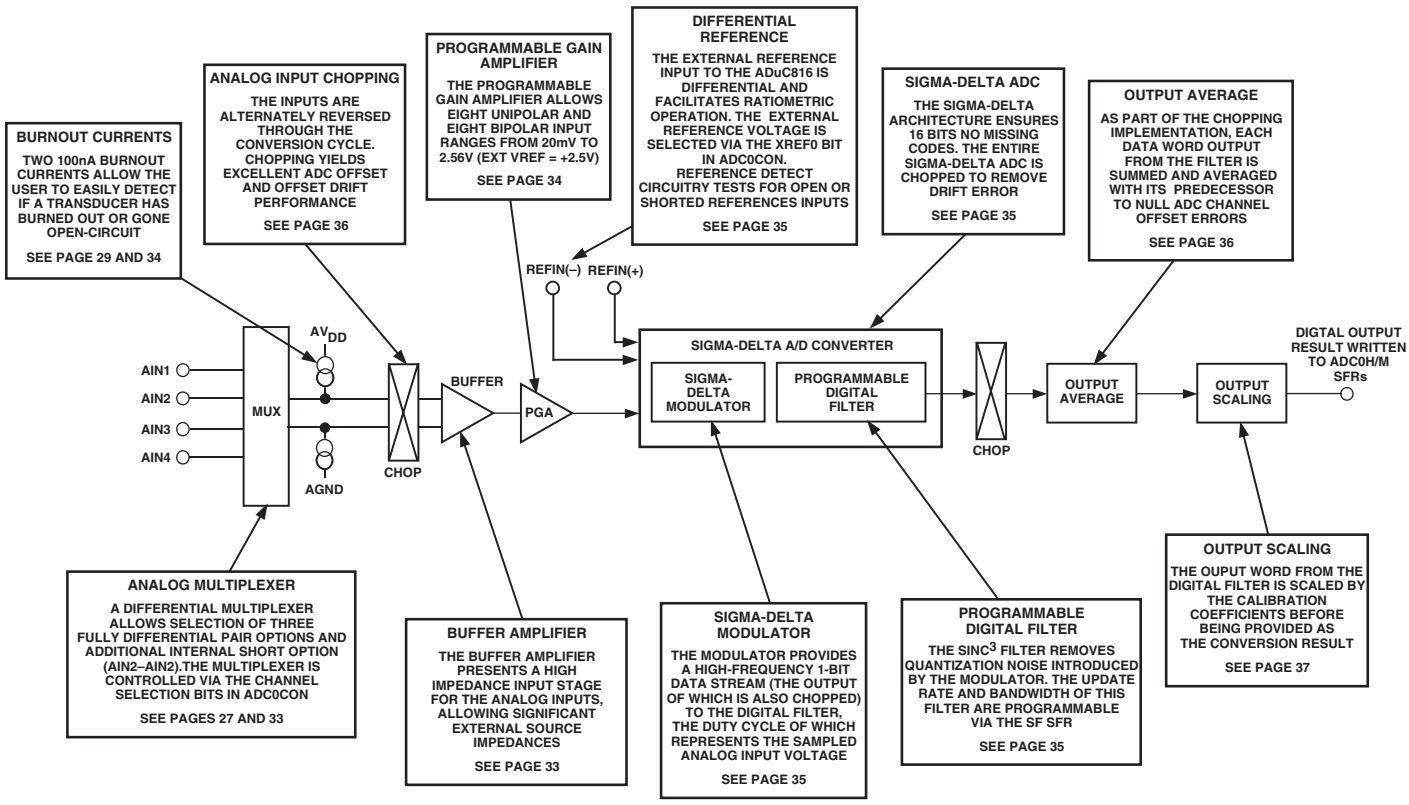


Figure 18. Primary ADC Block Diagram

Auxiliary ADC

The Auxiliary ADC is intended to convert supplementary inputs such as those from a cold junction diode or thermistor. This ADC is not buffered and has a fixed input range of 0 V to 2.5 V (assuming an external 2.5 V reference). The single-ended inputs can be driven from AIN3, AIN4 or AIN5 pins or directly from the on-chip temperature sensor voltage. A block diagram of the Auxiliary ADC is shown in Figure 19.

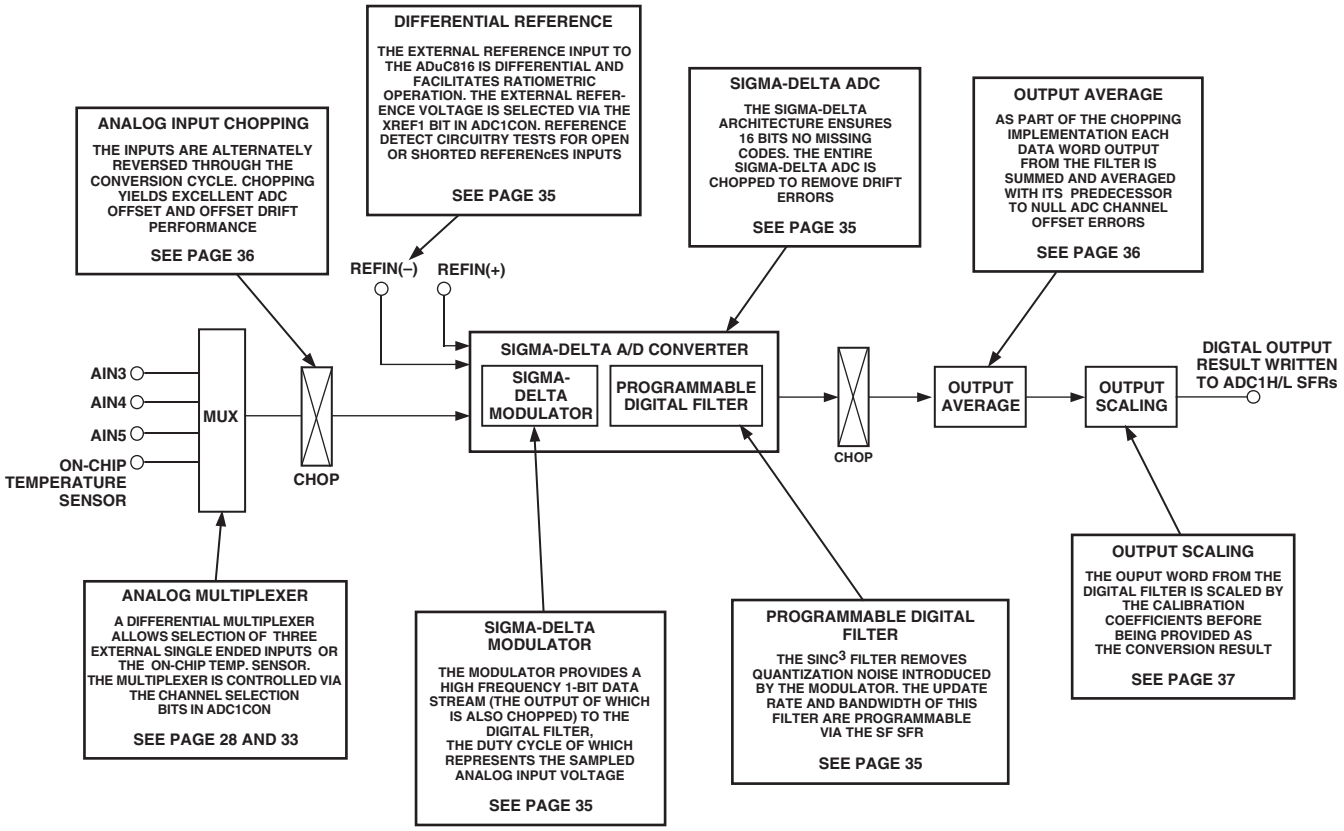


Figure 19. Auxiliary ADC Block Diagram

PRIMARY AND AUXILIARY ADC NOISE PERFORMANCE

Tables IX, X and XI below show the output rms noise in μV and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates on both the Primary and Auxiliary ADCs. The numbers are typical and are generated at a differential input voltage of 0 V. The output update rate is selected via the SF7–SF0 bits in the Sinc Filter (SF) SFR. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit.

Table IX. Primary ADC, Typical Output RMS Noise (μV)

Typical Output RMS Noise vs. Input Range and Update Rate; Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	Input Range ±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table X. Primary ADC, Peak-to-Peak Resolution (Bits)

Peak-to-Peak Resolution vs. Input Range and Update Rate; Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	Input Range ±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13	14	15	16	16[1]	16[1]	16[1]	16[1]
255	5.35	14	15	16	16[1]	16[1]	16[1]	16[1]	16[1]

NOTE
[1]Peak-to-peak resolution at these range/update rate settings is limited only by the number of bits available from the ADC. Effective resolution at these range/update rate settings is greater than 16 bits as indicated by the rms noise table shown in Table IX.

Table XI. Auxiliary ADC

Typical Output RMS Noise vs. Update Rate[1]
Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range 2.5 V
13	105.3	10.75
69	19.79	2.00
255	5.35	1.15

NOTE
[1]ADC converting in bipolar mode.

Peak-to-Peak Resolution vs. Update Rate[1]
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range 2.5 V
13	105.3	16[2]
69	19.79	16
255	5.35	16

NOTES
[1]ADC converting in bipolar mode.
[2]In unipolar mode peak-to-peak resolution at 105 Hz is 15 bits.

Analog Input Channels

The primary ADC has four associated analog input pins (labelled AIN1 to AIN4) which can be configured as two fully differential input channels. Channel selection bits in the ADC0CON SFR detailed in Table V allow three combinations of differential pair selection as well as an additional shorted input option (AIN2–AIN2).

The auxiliary ADC has three external input pins (labelled AIN3 to AIN5) as well as an internal connection to the internal on-chip temperature sensor. All inputs to the auxiliary ADC are single-ended inputs referenced to the AGND on the part. Channel selection bits in the ADC1CON SFR detailed previously in Table VI allow selection of one of four inputs.

Two input multiplexers switch the selected input channel to the on-chip buffer amplifier in the case of the primary ADC and directly to the sigma-delta modulator input in the case of the auxiliary ADC. When the analog input channel is switched, the settling time of the part must elapse before a new valid word is available from the ADC.

Primary and Auxiliary ADC Inputs

The output of the primary ADC multiplexer feeds into a high impedance input stage of the buffer amplifier. As a result, the primary ADC inputs can handle significant source impedances and are tailored for direct connection to external resistive-type sensors like strain gauges or Resistance Temperature Detectors (RTDs).

The auxiliary ADC, however, is unbuffered resulting in higher analog input current on the auxiliary ADC. It should be noted that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors depending on the output impedance of the source that is driving the ADC inputs.

Analog Input Ranges

The absolute input voltage range on the primary ADC is restricted to between AGND + 100 mV to AVDD – 100 mV. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded, otherwise there will be a degradation in linearity performance.

Figures 23 and 24 show the NMR for 50 Hz and 60 Hz across the full range of SF word, i.e., SF = 13 dec to SF = 255 dec.

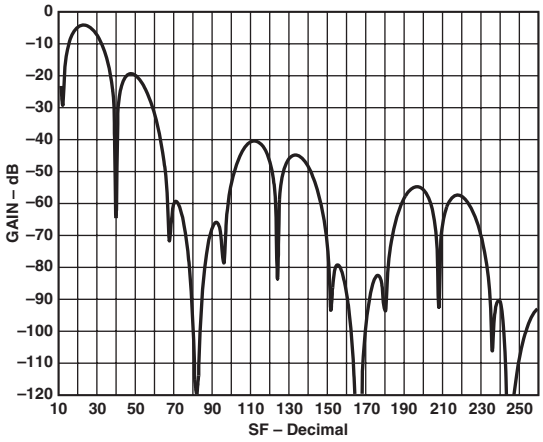


Figure 23. 50 Hz Normal Mode Rejection vs. SF

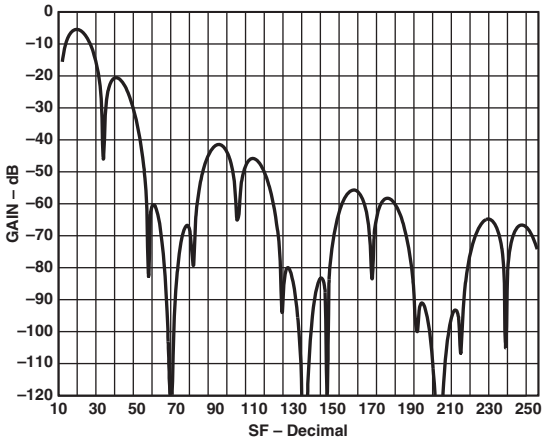


Figure 24. 60 Hz Normal Mode Rejection vs. SF

ADC Chopping

Both ADCs on the ADuC816 implement a chopping scheme whereby the ADC repeatability reverses its inputs. The decimated digital output words from the $Sinc^3$ filters therefore have a positive offset and negative offset term included.

As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data SFRs. In this way, while the ADC throughput or update rate is as discussed earlier and illustrated in Table VII, the full settling time through the ADC (or the time to a first conversion result), will actually be given by $2 \times t_{ADC}$.

The chopping scheme incorporated in the ADuC816 ADC results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors.

Calibration

The ADuC816 provides four calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table IV. In fact, every ADuC816 has already been factory calibrated. The resultant Offset and Gain calibration coefficients for both the primary and auxiliary ADCs are stored on-chip in manufacturing-specific Flash/EE memory locations. At power-on, these factory calibration coefficients are automatically downloaded to the calibration registers in the ADuC816 SFR space. Each ADC (primary and auxiliary) has dedicated calibration SFRs, these have been described earlier as part of the general ADC SFR description. However, the factory calibration values in the ADC calibration SFRs will be overwritten if any one of the four calibration options are initiated and that ADC is enabled via the ADC enable bits in ADCMODE.

Even though an internal offset calibration mode is described below, it should be recognized that both ADCs are chopped. This chopping scheme inherently minimizes offset and means that an internal offset calibration should never be required. Also, because factory 5 V/25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration will only be required if the part is being operated at 3 V or at temperatures significantly different from 25°C.

The ADuC816 offers "internal" or "system" calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. The result of the "zero-scale" calibration conversion is stored in the Offset Calibration Registers for the appropriate ADC. The result of the "full-scale" calibration conversion is stored in the Gain Calibration Registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an "internal" zero-scale or full-scale calibration, the respective "zero" input and "full-scale" input are automatically connected to the ADC input pins internally to the device. A "system" calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the external ADC pins before the calibration mode is initiated. In this way external ADC errors are taken into account and minimized as a result of system calibration. It should also be noted that to optimize calibration accuracy, all ADuC816 ADC calibrations are carried out automatically at the slowest update rate.

Internally in the ADuC816, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient. All ADuC816 ADC specifications will only apply after a zero-scale and full-scale calibration at the operating point (supply voltage/temperature) of interest.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the ADCSTAT SFR to determine end of calibration via a polling sequence or interrupt driven routine.

INTVAL **User Time Interval Select Register**

Function	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) bit is set and generates an interrupt if enabled. (See IEIP2 SFR description under Interrupt System later in this data sheet.)
SFR Address	A6H
Power-On Default Value	00H
Bit Addressable	No
Valid Value	0 to 255 decimal

HTHSEC **Hundredths Seconds Time Register**

Function	This register is incremented in (1/128) second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address	A2H
Power-On Default Value	00H
Bit Addressable	No
Valid Value	0 to 127 decimal

SEC **Seconds Time Register**

Function	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address	A3H
Power-On Default Value	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

MIN **Minutes Time Register**

Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address	A4H
Power-On Default Value	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

HOUR **Hours Time Register**

Function	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.
SFR Address	A5H
Power-On Default Value	00H
Bit Addressable	No
Valid Value	0 to 23 decimal

Table XIX. SPICON SFR Bit Designations (*continued*)

Bit	Name	Description
1 0	SPR1 SPR0	SPI Bit-Rate Select Bits. These bits select the SCLOCK rate (bit-rate) in Master Mode as follows: SPR1 SPR0 Selected Bit Rate 0 0 $f_{CORE}/2$ 0 1 $f_{CORE}/4$ 1 0 $f_{CORE}/8$ 1 1 $f_{CORE}/16$ In SPI Slave Mode, i.e., SPIM = 0, the logic level on the external $\overline{SS}$ pin (Pin 13), can be read via the SPR0 bit.

NOTE
The CPOL and CPHA bits should both contain the same values for master and slave devices.

SPIDAT **SPI Data Register**

Function: The SPIDAT SFR is written by the user to transmit data over the SPI interface or read by user code to read data just received by the SPI interface.

SFR Address: F7H

Power-On Default Value: 00H

Bit Addressable: No

Using the SPI Interface

Depending on the configuration of the bits in the SPICON SFR shown in Table XIX, the ADuC816 SPI interface will transmit or receive data in a number of possible modes. Figure 32 shows all possible ADuC816 SPI configurations and the timing relationships and synchronization between the signals involved. Also shown in this figure is the SPI interrupt bit (ISPI) and how it is triggered at the end of each byte-wide communication.

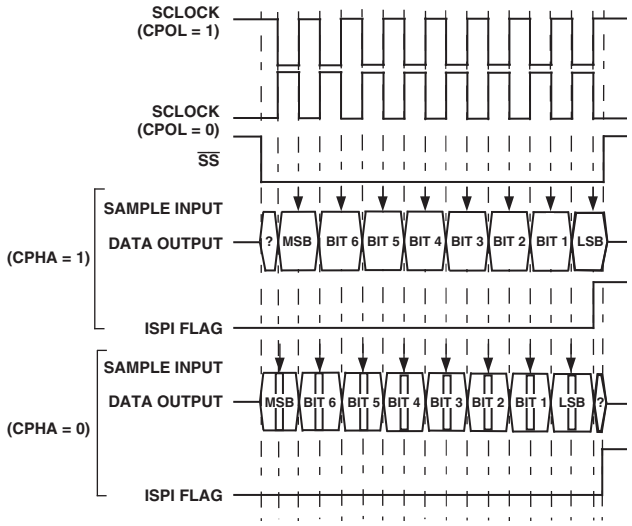


Figure 32. SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. It should also be noted that the $\overline{SS}$ pin is not used in master mode. If the ADuC816 needs to assert the $\overline{SS}$ pin on an external slave device, a Port digital output pin should be used.

In master mode a byte transmission or reception is initiated by a write to SPIDAT. Eight clock periods are generated via the SCLOCK pin and the SPIDAT byte being transmitted via MOSI. With each SCLOCK period a data bit is also sampled via MISO. After eight clocks, the transmitted byte will have been completely transmitted and the input byte will be waiting in the input shift register. The ISPI flag will be set automatically and an interrupt will occur if enabled. The value in the shift register will be latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication.

Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO and a data bit is received via MOSI through each input SCLOCK period. After eight clocks, the transmitted byte will have been completely transmitted and the input byte will be waiting in the input shift register. The ISPI flag will be set automatically and an interrupt will occur if enabled. The value in the shift register will be latched into SPIDAT only when the transmission/reception of a byte has been completed. The end of transmission occurs after the eighth clock has been received, if CPHA = 1 or when $\overline{SS}$ returns high if CPHA = 0.

User configuration and control of all Timer operating modes is achieved via three SFRs namely:

TMOD, TCON: Control and configuration for Timers 0 and 1.
T2CON: Control and configuration for Timer 2.

TMOD **Timer/Counter 0 and 1 Mode Register**
SFR Address 89H
Power-On Default Value 00H
Bit Addressable No

Gate	C/$\overline{T}$	M1	M0	Gate	C/$\overline{T}$	M1	M0

Table XXIII. TMOD SFR Bit Designations

Bit	Name	Description
7	Gate	Timer 1 Gating Control. *Set* by software to enable timer/counter 1 only while $\overline{INT1}$ pin is high and TR1 control bit is set. *Cleared* by software to enable timer 1 whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer 1 Timer or Counter Select Bit. *Set* by software to select counter operation (input from T1 pin). *Cleared* by software to select timer operation (input from internal system clock).
5	M1	Timer 1 Mode Select Bit 1 (Used with M0 Bit).
4	M0	Timer 1 Mode Select Bit 0. M1 M0 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Auto-Reload Timer/Counter. TH1 holds a value which is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. *Set* by software to enable timer/counter 0 only while $\overline{INT0}$ pin is high and TR0 control bit is set. *Cleared* by software to enable Timer 0 whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer 0 Timer or Counter Select Bit. *Set* by software to select counter operation (input from T0 pin). *Cleared* by software to select timer operation (input from internal system clock).
1	M1	Timer 0 Mode Select Bit 1.
0	M0	Timer 0 Mode Select Bit 0. M1 M0 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler 1 0 8-Bit Auto-Reload Timer/Counter. TH0 holds a value which is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

UART SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the first byte will be lost. The physical interface to the serial data network is via Pins RXD(P3.0) and TXD(P3.1) while the SFR interface to the UART is comprised of the following registers.

SBUF

The serial port receive and transmit registers are both accessed through the SBUF SFR (SFR address = 99 hex). Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON **UART Serial Port Control Register**

SFR Address 98H
Power-On Default Value 00H
Bit Addressable Yes

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table XXVII. SCON SFR Bit Designations

Bit	Name	Description
7	SM0	UART Serial Mode Select Bits.
6	SM1	These bits select the Serial Port operating mode as follows: SM0 SM1 Selected Operating Mode 0 0 Mode 0: Shift Register, fixed baud rate (Core_Clk/2) 0 1 Mode 1: 8-bit UART, variable baud rate 1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/64) or (Core_Clk/32) 1 1 Mode 3: 9-bit UART, variable baud rate
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI will not be activated if a valid stop bit was not received. If SM2 is cleared, RI will be set as soon as the byte of data has been received. In Modes 2 or 3, if SM2 is set, RI will not be activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI will be set as soon as the byte of data has been received.
4	REN	Serial Port Receive Enable Bit. *Set* by user software to enable serial port reception. *Cleared* by user software to disable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 will be the ninth data bit that will be transmitted in Modes 2 and 3.
2	RB8	Serial port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1 the stop bit is latched into RB8.
1	TI	Serial Port Transmit Interrupt Flag. *Set* by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. TI must be cleared by user software.
0	RI	Serial Port Receive Interrupt Flag. *Set* by hardware at the end of the eighth bit in mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by software.