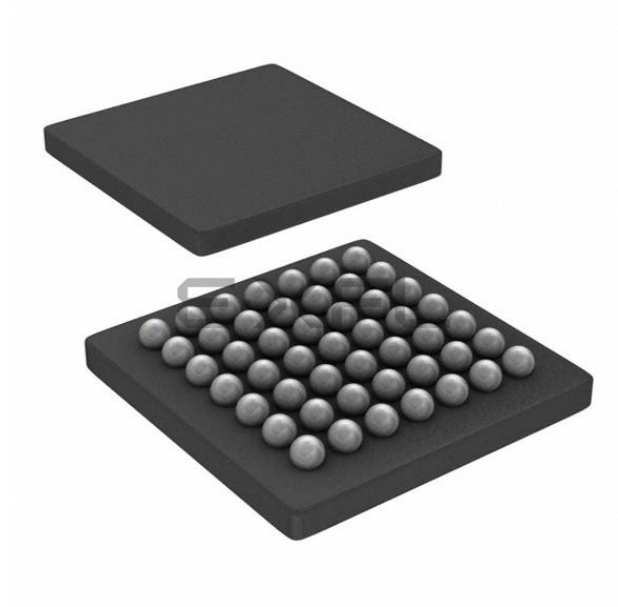
Lattice Semiconductor Corporation - LCMXO3LF-2100E-5UWG49CTR50 Datasheet



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Applications of Embedded - FPGAs

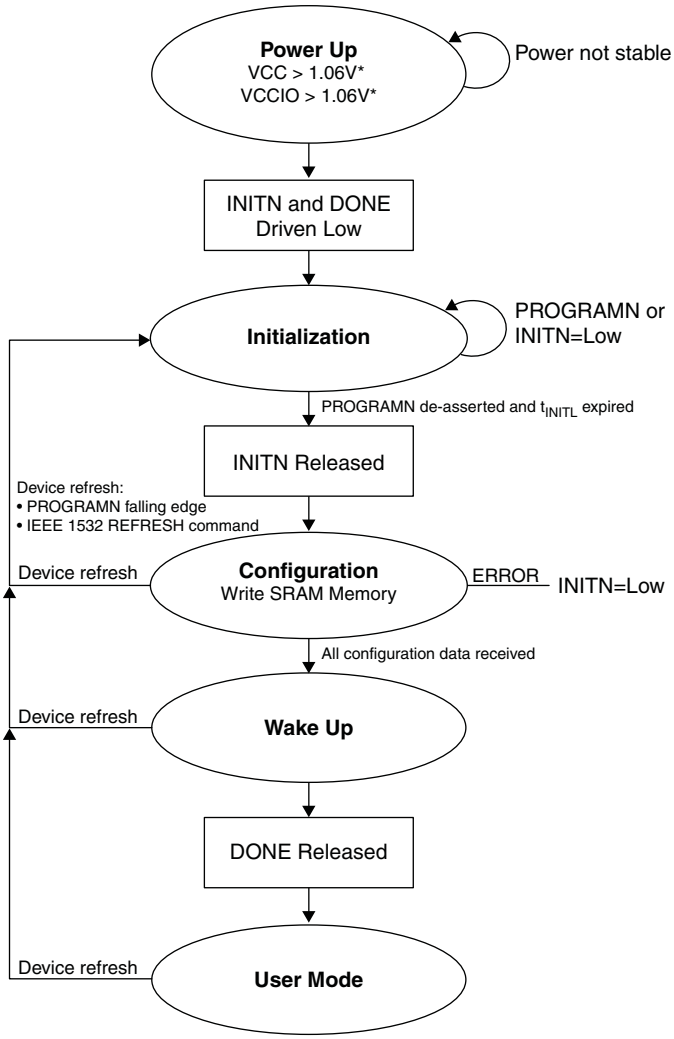
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	38
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.11x3.19)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-2100e-5uwg49ctr50

Configuration Process and Flow

Prior to becoming operational, the FPGA goes through a sequence of states, including initialization, configuration and wake-up.

Figure 1. Configuration Flow



* The voltage level is for the MachXO3 E device. Voltage level may vary for other devices.

The MachXO3L/LF sysCONFIG ports provide industry standard communication protocols for programming and configuring the FPGA. Each of the protocols shown in Table 1 provides a way to access the MachXO3L/LF device's internal NVCM/Flash, or to load its configuration SRAM. The Memory Space Accessibility section provides information about the capabilities of each sysCONFIG port.

The sysCONFIG ports capable of accessing the SRAM have a priority order. The operation of the Configuration Logic is not defined when a low priority sysCONFIG port is interrupted by a higher priority sysCONFIG port. Do not permit simultaneous access to the Configuration Logic using a sysCONFIG port.

A relationship of Feature Row option and Diamond Spreadsheet View is shown in Table 3 and Table 4.

Table 3. Feature Row Option and Diamond Spreadsheet View

MASTER_SPI_PORT	CONFIGURATION	BOOT_SEL[2:1], MSPI_Persistent_Enable
ENABLE	CFG[1]	101
ENABLE	EXTERNAL	011
EFB_USER	CFG[1]	000
DISABLE	CFG[1]	000

1. "CFG" includes CFG or CFG_EBR.

A full list of the functions controlled by the Feature Row and their default values for MachXO3L are shown in Table 4.

Table 4. MachXO3L Feature Row Elements

Feature	SW Default Mode State (Programmed)	HW Default Mode State (Erased)
PROGRAMN Persistence	Disabled	Enabled
INITn Persistence	Disabled	Disabled
DONE Persistence	Disabled	Disabled
Custom IDCODE	0x00000000	0x00000000
TraceID™	00000000	00000000
Security[1]	OFF	OFF
JTAG Port Persistence	Enabled	Enabled
SSPI Port Persistence	Enabled	Enabled
I^2C Port Persistence	Disabled	Enabled
MSPI Port Persistence	Disabled	Disabled
I^2C Programmable Primary Configuration Address[2, 3]	yyyxxxxx00	1111000000
SRAM OTP	OFF	OFF
Config NVCM/Flash OTP	OFF	OFF
my_ASSP Enable	OFF	OFF
Password Enable Flash	OFF	OFF
Password Enable All	OFF	OFF

1. Enabled/disabled using the CONFIG_SECURE preference.
2. "y" and "x" are user programmable from IPexpress™.
3. 1111000001 is a reserved address when the device is erased.

It is strongly recommended that the Feature Row only be modified during development, and rarely, if ever, upgraded in the field. The reason for this recommendation is the Feature Row is responsible for controlling the availability of the Configuration Ports. It is possible to cause active Configuration Ports to become unavailable, preventing future updates.

Changing the Feature Row can also prevent the MachXO3L/LF from configuring. The PROGRAMN, INITN, and DONE control and status pins are enabled and disabled using the Feature Row. The PROGRAMN input pin may be recovered for use as a general purpose I/O. Erasing Feature Row state causes the PROGRAMN input to act as PROGRAMN, not as a general purpose I/O. If the general purpose I/O is driven active low the MachXO3L will never be allowed to complete its configuration process.

Feature Row can be erased or altered by Diamond Programmer under Advanced Security Keys Programming. Feature Row settings can be altered using the Diamond Spreadsheet View. Spreadsheet View allows you to edit

the configuration settings for the MachXO3L/LF, and then saves your settings in the Lattice Preference File (LPF). These settings are applied to the MachXO3L/LF configuration data during the Map, Place, and Route build phases.

Key Features

- Not intended to be modified in the field; only for development.
- Change in Feature Row settings may cause active configuration ports to become unavailable.
- Can be altered using Diamond Programmer or Diamond Spreadsheet View.
- Can be altered independently under Advanced Security Keys Programming in Programmer.
- Will be erased and re-programmed during On-Chip Memory updates. So keep Feature Row contents consistent.
- MachXO3 only can be altered a total of eight times.

sysCONFIG™ Ports

Table 5. MachXO3L/LF Programming and Configuration Ports

Interface	Port	Description
JTAG	JTAG (IEEE 1149.1 and IEEE 1532 compliant)	4-wire or 5-wire JTAG Interface
sysCONFIG	SSPI	Slave Serial Peripheral Interface (SPI)
	MSPI	Master Serial Peripheral Interface (SPI)
	I^2C	Inter-integrated Circuit (I^2C) Interface
Internal	WISHBONE Internal	WISHBONE bus interface

sysCONFIG Pins

The MachXO3L/LF provides a set of sysCONFIG I/O pins that you use to program and configure the FPGA. The sysCONFIG pins are grouped together to create ports (i.e. JTAG, SSPI, I^2C, MSPI) that are used to interact with the FPGA for programming, configuration, and access of resources inside the FPGA. The sysCONFIG pins in a configuration port group may be active, and used for programming the FPGA, or they can be reconfigured to act as general purpose I/O.

Recovering the configuration port pins for use as general purpose I/O requires you to adhere to the following guidelines:

- You must DISABLE the unused port. You can accomplish this by using the Diamond Spreadsheet View's Global Preferences tab. Each configuration port is listed in the sysCONFIG options tree.
- You must prevent external logic from interfering with device programming. Make sure that recovered sysCONFIG pins are not asserted when the MachXO3L/LF is in Feature Row HW Default Mode state. One example is driving PROGRAMN with an active low signal after the MachXO3L/LF is in Feature Row HW Default Mode state. Failure to reprogram the Feature Row with PROGRAMN disabled prevents the FPGA from configuring and entering user mode.
- Use care when using JTAGENB to selectively enable and disable the JTAG port. Any external logic connected to the JTAG I/O must not contend with the JTAG programming port.

Table 6 lists the default state of the shared sysCONFIG pins. As you can see, an HW Default Mode Feature Row device has the JTAG, SPI Slave and I^2C ports enabled. Upon entry to User Mode the MachXO3L, the default state of the SSPI, and I^2C sysCONFIG pins become general purpose I/O. This means you lose the ability to program the MachXO3L using I^2C when using the default sysCONFIG port settings. To retain the I^2C sysCONFIG pins in user mode, be sure to ENABLE them using the Diamond Spreadsheet View editor.

Unless specified otherwise, the sysCONFIG pins are powered by the VCCIO0 voltage. It is crucial you take this into consideration when provisioning other logic attached to Bank 0.

The function of each sysCONFIG pin is described in detail.

Table 6. Default State of the sysCONFIG Pins

Pin Name	Associated sysCONFIG Port	Pin Function in Feature Row Erased Mode (Configuration/HW Mode)	Pin Direction (Configuration Mode)	Default Function in User Mode (SW default Mode)
PROGRAMN	SDM	PROGRAMN	Input with weak pull up	User-defined I/O
INITN	SDM	I/O	I/O with weak pull up	User-defined I/O
DONE	SDM	I/O	I/O with weak pull up	User-defined I/O
MCLK/CCLK	SSPI/MSPI	SSPI	Input with weak pull up	SSPI
SN	SSPI/MSPI	SSPI	Input with weak pull up	SSPI
SI/SISPI	SSPI/MSPI	SSPI	Input	SSPI
SO/SPISO	SSPI/MSPI	SSPI	Output	SSPI
CSSPIN	MSPI	I/O	I/O with weak pull up	User-defined I/O
SCL	I^2C	I^2C	Bi-Directional	User-defined I/O
SDA	I^2C	I^2C	Bi-Directional	User-defined I/O

Table 7. Default State in Diamond for Each Port

sysConfig Port	Diamond Default [1]
SDM_PORT	Disable
SLAVE_SPI_PORT	Enable
I2C_PORT	Disable
MASTER_SPI_PORT	Disable
JTAG_PORT	Enable

1. This Default setting can be modified in the Diamond Spreadsheet View, Global Preferences tab.

Self Download Port Pins

PROGRAMN: The PROGRAMN is an input used to configure the FPGA. The PROGRAMN pin, when enabled, is sensitive to a high-to-low transition, and has an internal weak pull-up. When PROGRAMN is asserted low, the FPGA exits user mode and starts a device configuration sequence at the Initialization phase, as described earlier. Holding the PROGRAMN pin low prevents the MachXO3L from leaving the Initialization phase. The PROGRAMN has a minimum pulse width assertion period in order for it to be recognized by the FPGA. You can find this minimum time in DS1047, MachXO3 Family Data Sheet in the AC timing section.

Be aware of the following special cases when the PROGRAMN pin is active:

- If the device is currently being programmed via JTAG then PROGRAMN will be ignored until the JTAG mode programming sequence is complete.
- Toggling the PROGRAMN pin during device configuration will interrupt the process and restart the configuration cycle.
- Asserting PROGRAMN on a device in Feature Row HW Default Mode state disables the SSPI and I^2C ports. Start SSPI or I^2C programming operations after PROGRAMN is deasserted.
- PROGRAMN is active during power-up, even when PROGRAMN has been reserved as a general purpose I/O. Do not allow any input signal attached to PROGRAMN to transition from high to low at a frequency greater than the VCC (min) to INITN rising edge time period. High to low PROGRAMN assertions more frequently prevent the MachXO3L from configuring, causing the FPGA to remain in a continuous RESET condition. See Figure 5.

Master and Slave SPI Configuration Port Pins

Table 8. Master SPI Configuration Port Pins

Pin Name	Function	Direction	Description
MCLK/CCLK	MCLK	Output with weak pullup	Master clock used to time data transmission/reception from the MachXO3L Configuration Logic to a slave SPI PROM. A 1K pull-up resistor is recommended on MCLK for External and Dual Boot configuration modes.
CSSPIN	CSSPIN	Output	Chip select used to enable an external SPI PROM containing configuration data
SI/SISPI	SISPI	Output	SISPI carries output data from the MachXO3L Configuration Logic to the slave SPI PROM
SO/SPISO	SPISO	Input	SPISO carries output data from the slave SPI PROM to the MachXO3L Configuration Logic
SN	SN/IO	Input	MachXO3L Configuration Logic slave SPI chip select input. Pull high externally whenever the MSPI port is active.

Table 9. Slave SPI Configuration Port Pins

Pin name	Function	Direction	Description
MCLK/CCLK	CCLK	Input with weak pullup	Clock used to time data transmission/reception from an external SPI master device to the MachXO3L Configuration Logic.
SI/SISPI	SI	Input	SI carries output data from the external SPI master to the MachXO3L Configuration Logic
SO/SPISO	SO	Output	SO carries output data from the MachXO3L Configuration Logic to the external SPI master
SN	SN	Input with weak pullup	MachXO3L Configuration Logic slave SPI chip select input. SN is an active low input.

MCLK/CCLK: The MCLK/CCLK, when active, are clocks used to sequentially load the configuration data for the FPGA. The pin functions as:

The MCLK/CCLK pin's default state for a MachXO3L in the Feature Row HW Default Mode state is to act as the configuration clock (i.e., CCLK). This allows an external SPI master controller to program the MachXO3L/LF. The maximum CCLK frequency and the data setup/hold parameters can be found in the AC timing section of DS1047, MachXO3 Family Data Sheet. The Feature Row must be configured to ENABLE the Slave SPI Port if you want to use the port to reprogram the MachXO3L/LF after it enters user mode.

The MCLK/CCLK pin functions as a Master Clock (MCLK) when the MachXO3L/LF is configured in Dual Boot or External Boot modes. A 1K pull-up resistor is recommended when using these modes. The MCLK becomes an output and provides a reference clock for an SPI Flash attached to the MachXO3L/LF's Master SPI Configuration port. MCLK actively drives until all of the configuration data has been received. When the MachXO3L enters user mode the MCLK output tri-states. This allows the MCLK to become a general purpose I/O. The MCLK is reserved for use, in most post-configuration applications, as the reference clock for performing memory transactions with the external SPI PROM.

The MachXO3L/LF generates MCLK from an internal oscillator. The initial frequency of the MCLK is nominally 2.08 MHz. The MCLK frequency can be altered using the MCCLK_FREQ parameter. You can select the MCCLK_FREQ using the Diamond Spreadsheet View. For a complete list of the supported MCLK frequencies, see Table 10.

When the device is programmed through IEEE 1149.1 control, the sysCONFIG programming pins, such as DONE, cannot be used to determine programming progress. This is because the state of the boundary scan cell will drive the pin, per the IEEE JTAG standard, rather than normal internal logic.

Table 11. JTAG Port Pins

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
TDI	TDI	Input with weak pull-up	TDI
TDO	TDO	Output with weak pull-up	TDO
TCK	TCK	Input	TCK
TMS	TMS	Input with weak pull-up	TMS
JTAGENB	I/O	Input/output with weak pull-down	I/O

TDO: The Test Data Output (TDO) pin is used to shift out serial test instructions and data. When TDO is not being driven by the internal circuitry, the pin will be in a high impedance state. The only time TDO is not in a high impedance state is when the JTAG state machine is in the Shift IR or Shift DR state. This pin should be wired to TDO of the JTAG connector, or to TDI of a downstream device in a JTAG chain. An internal pull-up resistor on the TDO pin is provided. The internal resistor is pulled up to VCCIO Bank 0.

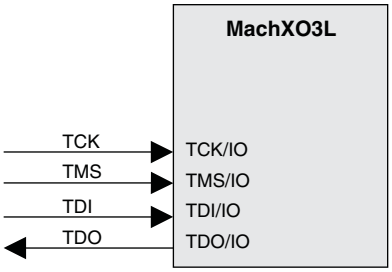
TDI: The Test Data Input (TDI) pin is used to shift in serial test instructions and data. This pin should be wired to TDI of the JTAG connector, or to TDO of an upstream device in a JTAG chain. An internal pull-up resistor on the TDI pin is provided. The internal resistor is pulled up to VCCIO of Bank 0.

TMS: The Test Mode Select (TMS) pin is an input pin that controls the progression through the 1149.1 compliant state machine states. The TMS pin is sampled on the rising edge of TCK. The JTAG state machine remains in or transitions to a new TAP state depending on the current state of the TAP, and the present state of the TMS input. An internal pull-up resistor is present on TMS per the JTAG specification. The internal resistor is pulled to the VCCIO of Bank 0.

TCK: The test clock pin (TCK) provides the clock used to time the other JTAG port pins. Data is shifted into the instruction or data registers on the rising edge of TCK and shifted out on the falling edge of TCK. The TAP is a static design permitting TCK to be stopped in either the high or low state. The maximum input frequency for TCK is specified in the DC and Switching Characteristics section of DS1047, MachXO3 Family Data Sheet. The TCK pin does not have a pull-up. An external pull-down resistor of 4.7 kOhms is recommended to avoid inadvertently clocking the TAP controller as power is applied to the MachXO3L/LF.

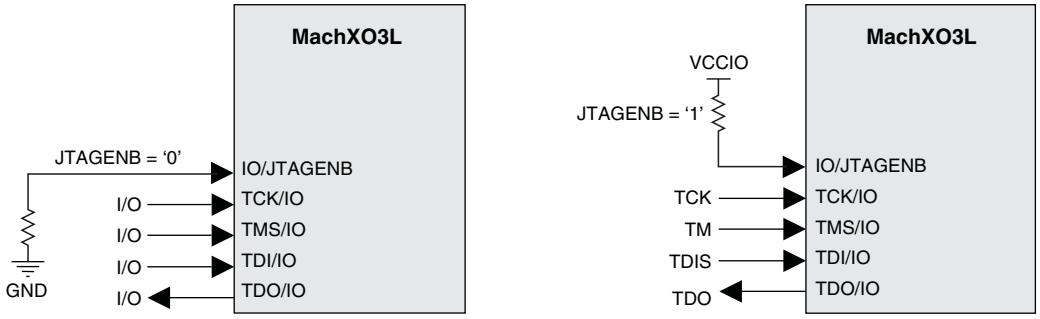
JTAGENB: The JTAG ENABLE pin, also known as the IEEE 1149.1 conformance pin, is an input pin that can be used to multiplex the JTAG port. The JTAGENB pin is only active in user mode. The JTAGENB pin is a user I/O while the JTAG port is in the ENABLE state. Figure 8 shows the default behavior of the JTAG port of a MachXO3L device.

Figure 8. Default JTAG Port with JTAG_PORT = ENABLE



The JTAG port can become general purpose I/O. By setting the JTAG_PORT preference in the Diamond Spreadsheet View to the DISABLE state. When the JTAG port is in the DISABLE state the JTAGENB pin becomes a dedicated input. Driving the JTAGENB low disables the JTAG port and the four JTAG pins become general purpose I/Os. Driving the JTAGENB input high enables the JTAG port. Figure 9 shows JTAG port behavior under the control of the JTAGENB.

Figure 9. JTAG Port Behavior with JTAG_PORT = DISABLE



It is critical when using the JTAGENB feature that logic attached to the JTAG I/O pins not contend with a JTAG programming system. The external logic must ignore any JTAG transactions performed by an external programming system.

Lattice parallel port or USB download cables provide an output called ispEN. The ispEN signal can be attached to the JTAGENB input to control the availability of the JTAG port. An alternate mechanism to control the JTAGENB input is to use a shunt that can be installed or removed as required.

Configuration Modes

The MachXO3L provides multiple options for loading the configuration SRAM from a non-volatile memory. The previous section described the physical interface necessary to interact with the MachXO3L configuration logic. This section focuses on describing the functionality of each of the different configuration modes. Descriptions of important settings required in the Diamond Spreadsheet View are also discussed.

SDM Mode

The advantages of Self Download Configuration Mode include:

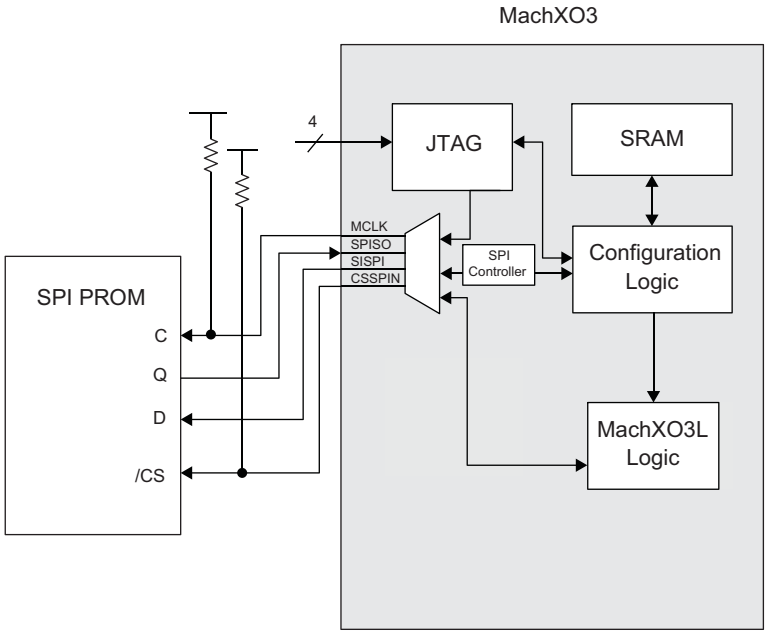
- **Speed**: The MachXO3L is ready to run in a few milliseconds depending on the density of the device.
- **Security**: The configuration data is never seen outside the device during the load to SRAM. You can prevent the internal memory from being read.
- **Reduced cost**: There is no need to purchase a PROM specifically reserved for programming the MachXO3L.
- **Reduced board space**: Elimination of an external PROM allows your board to be smaller.

The MachXO3L/LF retrieves the configuration data from the internal NVCM/Flash when it is using Self Download Mode. SDM is triggered when power is applied, a REFRESH command is received, or by asserting the PROGRAMN pin. Self Download Mode cannot be used when the Configuration Memory overflow occurs. Master SPI Configuration Mode must be used in the event of the Memory overflow.

Master SPI Configuration Mode (MSPI)

Master SPI Configuration Mode is the only other self-controlled configuration mode available to the MachXO3L/LF. When the MachXO3L/LF has the Master SPI Configuration mode (MSPI) enabled it is able to automatically retrieve the configuration data from an externally attached SPI Flash. The MSPI configuration port is not available when the MachXO3L/LF is in the Feature Row HW Default Mode state. Lattice recommends having a secondary configuration port available, one that is active when the MachXO3L/LF is in Feature Row HW Default Mode state, that allows you to recover the MachXO3L/LF in the event of a programming error.

Figure 11. Master SPI Configuration Mode



The MachXO3L/LF begins retrieving configuration data from the SPI Flash when power is applied, a REFRESH command is received, or the PROGRAMN pin is asserted and released. The MCLK/CCLK I/O takes on the Master Clock (MCLK) function, and begins driving a nominal 2.08 MHz clock to the SPI Flash's SCLK input. CSSPIN is asserted low, commands are transmitted to the PROM over the SI/SISPI output, and data is read from the PROM on the SO/SPISO input pin. When all of the configuration data is retrieved from the PROM the CSSPIN pin is deasserted, and the MSPI output pins are tri-stated.

The MCLK frequency always starts downloading the configuration data at the nominal 2.08 MHz frequency. The MCCLK_FREQ parameter, accessed using Spreadsheet View, can be used to increase the configuration frequency. The configuration data in the PROM has some padding bits, and then the data altering the MCLK base frequency is read. The MachXO3L reads the remaining configuration data bytes using the new MCLK frequency.

After the MachXO3L/LF enters user mode the Master SPI configuration port pins tri-state. This allows data transfers across the SPI. There are two primary methods available for transferring data across the SPI bus. The first method available to you is to enable the Embedded Function Block (EFB) in the MachXO3L/LF. Using IPexpress™ you instantiate the EFB, and you choose the features you want active. One of the features available in the EFB is an SPI Master Controller. The SPI Master Controller in the EFB attaches directly Master SPI configuration port pins. The controller provides a set of status, control, and data registers for initiating SPI bus transactions.

The second way to perform Master SPI configuration port transactions is to master them from the JTAG port. The MachXO3L/LF includes a JTAG to MSPI passthru circuit that allows the slave SPI Flash to be erased, programmed, and read. The primary method for programming the attached SPI Flash is to use Diamond Programmer to transfer a configuration data file from your personal computer. This is useful during board development and debug. *Note: To support JTAG to MSPI passthru programming mode a 1Kohm pull-up resister is required on MCLK*.

Another way to program an SPI Flash using the JTAG port is to use the Lattice ispVME solution. ispVME is C code written for an embedded microprocessor. The microprocessor reads a data file crafted by the Diamond Deployment Tool, and runs the ispVME code. The firmware uses port I/O to drive the JTAG port of the MachXO3L/LF, which in turn passes the data to the Master SPI port. Refer to the ispVME tool suite for information about updating an attached SPI Flash using a microprocessor.

To set the MachXO3L/LF for operation using the MSPI configuration mode you must:

- Store the entire configuration data in an external SPI Flash
- The data must start at offset 0x000000 within the PROM
- Set the preferences as shown in Table 13

Table 13. Master SPI Configuration Software Settings

Preference	Setting
MASTER_SPI_PORT	ENABLE
CONFIGURATION	EXTERNAL

The BIT file must be programmed into the external SPI Flash. There are several ways to get the data into the SPI Flash:

- Diamond Programmer can transmit the SPI Flash data using a JTAG download cable
- A microprocessor running ispVME
- Automatic Test Equipment can program the SPI Flash using JTAG
- Pre-programmed SPI Flash memories can be pre-assembled onto your printed-circuit board

Once the SPI Flash contains your configuration data, you can test the configuration. Assert the PROGRAMN, transmit a REFRESH command, or cycle power to the board, and the MachXO3L/LF will configure from the external SPI Flash.

Dual Boot Configuration Mode

Dual Boot Configuration Mode is a combination of Self Download Mode and Master SPI Configuration Mode. The MachXO3L, when set up in Dual Boot Mode, tries by default to configure first from external flash PROM using MSPI mode. If the configuration fails, the MachXO3L attempts to configure itself from the internal NVCM using SDM. The preset load order may be reversed if desired. The MachXO3LF, when set up in Dual Boot Mode, tries by default to configure first from the internal Flash memory using SDM. If the SDM configuration fails, the MachXO3LF attempts to configure itself using MSPI mode. The preset load order may be reversed if desired using the DUALBOOTGOLDEN configuration option in the Diamond software spreadsheet view.

Dual Boot Configuration Mode can be utilized in conjunction with the MachXO3LF Soft Error Detection (SED) feature without restriction. However, Soft Error Correction (SEC) use is limited to the primary image only. Refer to TN1292, MachXO3 Soft Error Detection/Correction Usage Guide for more information on the use of the SED and SEC features.

The first boot attempt is from the primary configuration image. If the primary configuration fails, the second boot attempt is from the golden/failsafe configuration image. The primary image can fail in one of two ways:

- A bitstream CRC error is detected
- A time-out error is encountered when loading

A CRC error is caused by incorrect or corrupt data. Data is read from the primary image in rows. As each row enters the Configuration Engine the data is checked for CRC consistency. Before the data enters the Configuration SRAM the CRC must be correct. Any incorrect CRC causes the device to erase the Configuration SRAM and retrieve configuration data from the golden/failsafe image location.

It is possible for the data to be correct from a CRC calculation perspective, but not be functionally correct. In this instance the internal DONE bit will never become active. The MachXO3L/LF counts the number of master clock pulses it has provided after the Power On Reset signal was released. When the count expires without DONE becoming active the FPGA attempts to get it's configuration data from the golden/failsafe image location.

Password

The MachXO3 supports a password-based security access feature also known as Flash Protect Key. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device.

The Flash Protect Key feature requires that a device accessing a MachXO3 device through a sysConfig port (JTAG, SSPI, I2C or WISHBONE) provide a valid digital Password, also known as the Flash Protect Key, to unlock the device and allow configuration or programming operations to proceed. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID.

The 64-bit Flash Protect Key is stored in the Feature Row. Two additional feature row fuses are specified for enabling the feature: PWD_Enable and PWD_Enable_all.

You can read more about the Password feature in TN1313, Using Password Security with MachXO3 Devices.

Software Selectable Options

The operation of the MachXO3L/LF configuration logic is managed by options selected in the Diamond design software. Other FPGAs provide dedicated I/O pins to select the configuration mode. The MachXO3L/LF uses the non-volatile Feature Row to select how it will configure. The Feature Row's default state needs to be modified in almost every design. You use the Diamond Spreadsheet View to make the changes to the operation of the MachXO3L/LF Feature Row which alters the operation of the configuration logic.

The configuration logic preferences are accessed using Spreadsheet View. Click on the Global Preferences tab, and look for the sysCONFIG tree. The sysCONFIG section is shown in Figure 17. The sysCONFIG preferences are divided into three categories:

- Configuration mode and port related
- Bitstream generation related
- Security related

sequence is complete. There is no external indication the device is ready to perform the last four state transitions. You must either provide a free running clock frequency, or you must wait until the device is guaranteed to be ready to wake up. Using the START macro provides another mechanism for holding off configuring one or more programmable devices and then starting them synchronously.

Verilog

```
module START (STARTCLK);
input  STARTCLK;
endmodule

START u1 (.STARTCLK(<clock_name>)) /* synthesis syn_noprune=1 */;
```

VHDL

```
COMPONENT START
    PORT(
          STARTCLK    :  IN STD_ULOGIC
        );
END COMPONENT;
attribute syn_noprune: boolean ;
attribute syn_noprune of START: component is true;

begin
u1: START port map (STARTCLK =><clock name>);
```

Advanced Configuration Information

NVCM/Flash Programming

The MachXO3's internal NVCM/Flash is the heart of the FPGA's configuration system. It is flexible, allowing you to store the FPGA's configuration data, as well as storing design specific data in the internal memory. It is also a resource that uses a precise erase and programming sequence. Lattice provides several methods for programming the MachXO3 NVCM/Flash:

- JTAG or Slave SPI programming
- **VMEmbedded**: 'C' source for use with an embedded microprocessor controlling the JTAG port
- **SSPIEmbedded**: 'C' source for use with an embedded microprocessor controlling the SSPI port
- **Custom**: The information in this section, and information from TN1294, Using Hardened Control Functions in MachXO3 Devices Reference Guide, permits creation of a custom solution.

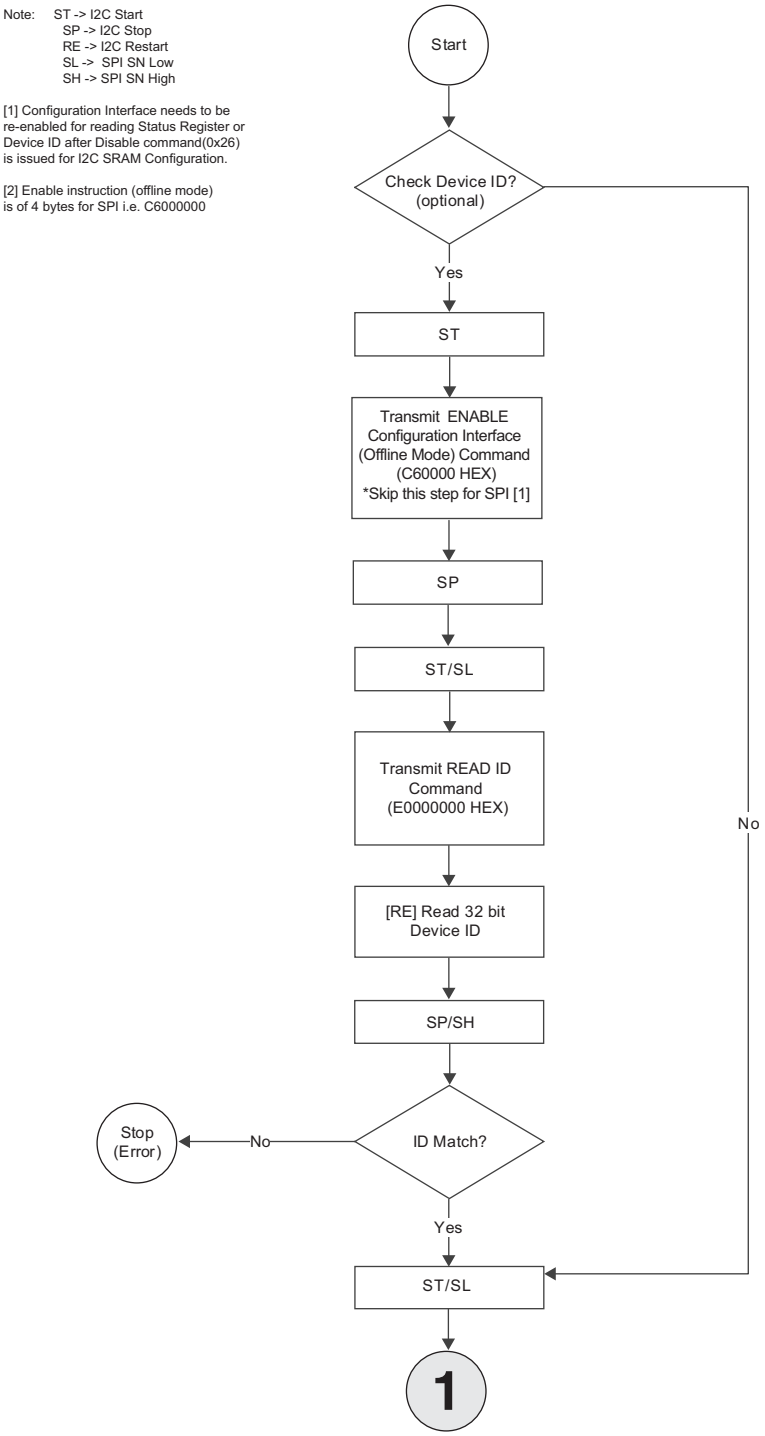
The NVCM (MachXO3L)/Flash(MachXO3LF) space can be accessed by the JTAG, I^2C, and SPI ports. These configuration ports may use offline or transparent modes to erase, program, and verify the MachXO3 NVCM (MachXO3L)/Flash(MachXO3LF) resources. The WISHBONE interface is only permitted to use transparent programming operations (MachXO3LF). The sequence and timing of the commands presented to the Configuration Logic are identical across all of the configuration ports. There are slight differences due to communication protocol standards when transmitting commands and data. The command and timing flow common to all configuration ports is described first. Protocol variances are described afterward.

Each MachXO3 contains a certain quantity of internal memory. The amount of memory depends on the device density of the MachXO3. Figure 19 shows the number of internal memory pages available for each MachXO3 device density. Each page represents 128 bits of data.

MachXO3 Slave SPI/I2C SRAM Configuration Flow

MachXO3 Slave SPI/I2C SRAM configuration requires a specific set of steps and timing. The flow chart in this section describes the command sequences and the timing required for successful SSPI/I2C SRAM configuration.

Figure 21. MachXO3 Slave SPI/I2C SRAM Configuration Flow



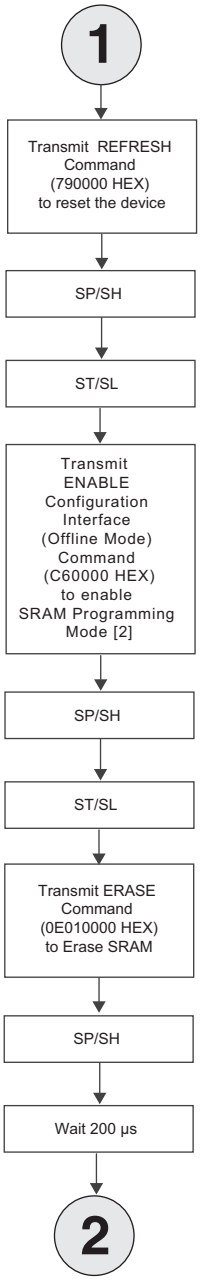
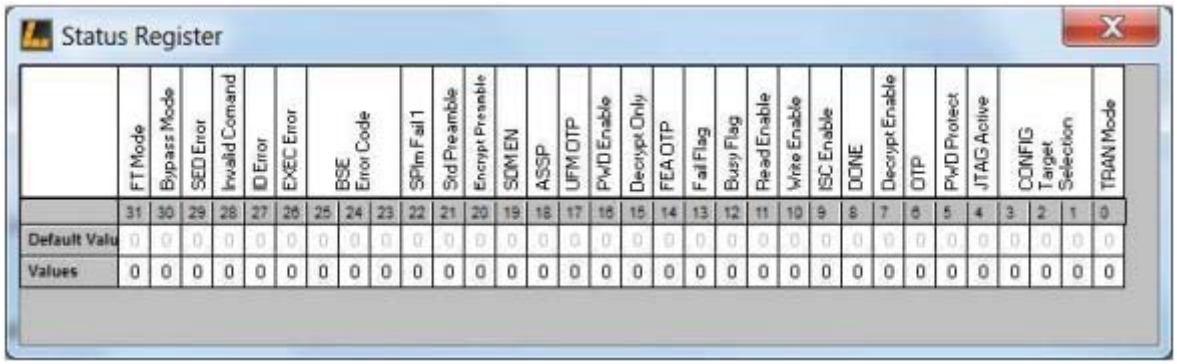
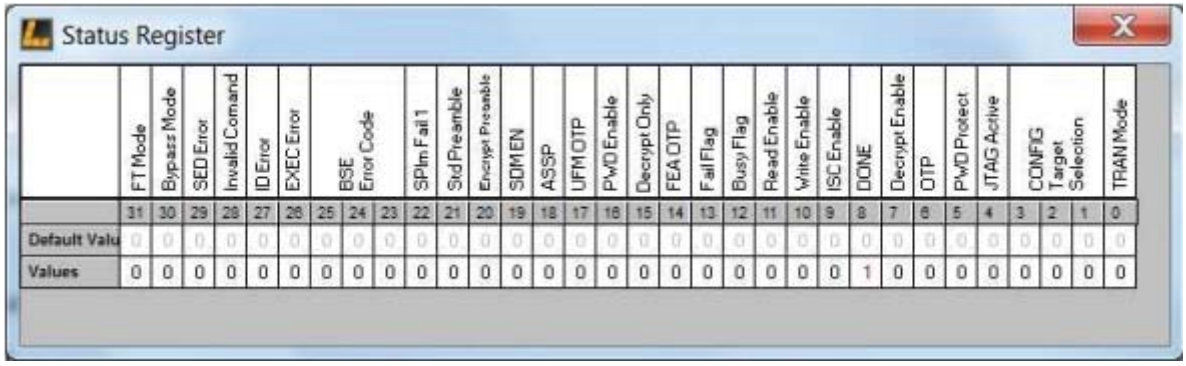

1
Transmit REFRESH Command (790000 HEX) to reset the device
SP/SH
ST/SL
Transmit ENABLE Configuration Interface (Offline Mode) Command (C60000 HEX) to enable SRAM Programming Mode [2]
SP/SH
ST/SL
Transmit ERASE Command (0E010000 HEX) to Erase SRAM
SP/SH
Wait 200 µs
2

Figure 22. Status Register Value After Erase

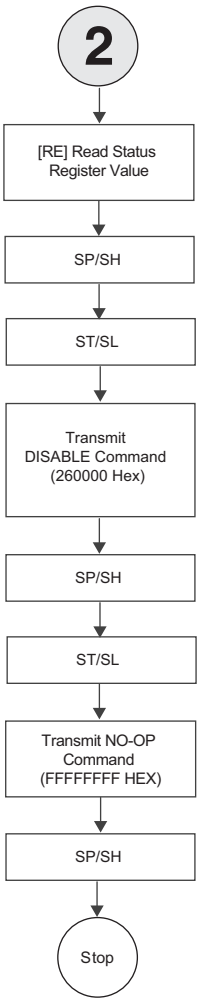


Expected value from SO: 0x00000000 with the MASK: 0x00003100
(bit 8-DONE = 0, bit 12-BUSY = 0, bit 13-FailFlag = 0)
Mask = 0 means don't care
Mask = 1 means care

Figure 23. Status Register Value After Program



Expected value from SO: 0x00000100 with the MASK: 0x00003100
(bit 8-DONE = 1, bit 12-BUSY = 0, bit 13-FailFlag = 0)
Mask = 0 means don't care
Mask = 1 means care


2
[RE] Read Status Register Value
SP/SH
ST/SL
Transmit DISABLE Command (260000 Hex)
SP/SH
ST/SL
Transmit NO-OP Command (FFFFFFFF HEX)
SP/SH
Stop

MachXO3 Programming Commands

Table 21. MachXO3 sysCONFIG Programming Commands

Command Name [SVF Synonym]	Command	Operands	Write Data	Read Data	Notes
Read Device ID [IDCODE_PUB]	0xE0	00 00 00	N/A	YY YY YY YY	YY characters represent the device-specific ID code.
Enable Configuration Interface (Transparent Mode) [ISC_ENABLE_X]	0x74	08 00 00[1]	N/A	N/A	Enable the Configuration Logic for device programming in transparent mode.[1]
Enable Configuration Interface (Offline Mode) [ISC_ENABLE]	0xC6	08 00 00[1]	N/A	N/A	Enable the Configuration Logic for device programming in Offline mode.[1]
Read Busy Flag [LSC_CHECK_BUSY]	0xF0	00 00 00	N/A	YY	Bit 1 0 7 Busy Ready
Read Status Register [LSC_READ_STATUS]	0x3C	00 00 00	N/A	YY YY YY YY	Bit 1 0 12 Busy Ready 13 Fail OK
Erase [ISC_ERASE]	0x0E	0Y 00 00	N/A	N/A	Y = Memory space to erase Y is a bitwise OR Bit 1=Enable 16 Erase SRAM 17 Erase Feature Row 18 Erase NVCM0/CFG 19 Erase NVCM1/UFM
Erase NVCM1/UFM [LSC_ERASE_TAG]	0xCB	00 00 00	N/A	N/A	Erase the NVCM1/UFM sector only.
Reset Configuration NVCM/CFG Address [LSC_INIT_ADDRESS]	0x46	00 00 00	N/A	N/A	Set Page Address pointer to the beginning of the NVCM0/Configuration Flash sector.
Set Address [LSC_WRITE_ADDRESS]	0xB4	00 00 00	M0 00 PP PP	N/A	Set the Page Address pointer to the NVCM/Flash page specified by the least significant 14 bits of the PP PP field. The 'M' field defines the NVCM/Flash space to access. Field 0x0 0x4 M NVCM0/CFG NVCM1/UFM
Program Page [LSC_PROG_INCR_NV]	0x70	00 00 01	YY * 16	N/A	Program one NVCM/Flash page. Can be used to program the NVCM0/CFG or NVCM1/UFM.
Reset NVCM1/UFM Address [LSC_INIT_ADDR_NVCM1/UFM]	0x47	00 00 00	N/A	N/A	Set the Page Address Pointer to the beginning of the NVCM1/UFM sector.
Program NVCM1/UFM Page [LSC_PROG_TAG]	0xC9	00 00 01	YY * 16	N/A	Program one NVCM1/UFM page.
Program USERCODE [ISC_PROGRAM_USERCODE]	0xC2	00 00 00	YY * 4	N/A	Program the USERCODE.
Read USERCODE [USERCODE]	0xC0	00 00 00	N/A	YY * 4	Retrieves the 32-bit USERCODE value.
Write Feature Row [LSC_PROG_FEATURE]	0xE4	00 00 00	YY * 8	N/A	Program the Feature Row bits.
Read Feature Row [LSC_READ_FEATURE]	0xE7	00 00 00	N/A	YY * 8	Retrieves the Feature Row bits.
Write FEABITS [LSC_PROG_FEABITS]	0xF8	00 00 00	YY * 2	N/A	Program the FEABITS.
Read FEABITS [LSC_READ_FEABITS]	0xFB	00 00 00	N/A	YY * 2	Retrieves the FEABITS.
Read NVCM/Flash [LSC_READ_INCR_NV]	0x73	M0 PP PP	N/A	See the Reading NVCM/Flash Pages section.	Retrieves PPPP count pages. Only the least significant 14 bits of PP PP are used. The 'M' field must be set based on the configuration port being used to read the NVCM/Flash. 0x0 I^2C 0x1 JTAG/SSPI

Table 21. MachXO3 sysCONFIG Programming Commands (Continued)

Command Name [SVF Synonym]	Command	Operands	Write Data	Read Data	Notes
Shift Flash Protect Key [LSC_SHIFT_PASSWORD]	0xBC	00 00 00	YY*8	N/A	Present the 64-bit Password. When enabled (PWD_enable = 1), the write data is compared to the Password contained into the Feature Row. If the values match, the device is unlocked for programming and configuration operations. The device remains unlocked until a Disable Configuration command is received, a Refresh command is issued, or a power cycle event occurs.

1. Transmit the command opcode and first two operand bytes when using the I^2C port. The final operand byte must not be transmitted.
2. SECURITY and SECURITY PLUS commands are mutually exclusive.

The I²C interface has additional overhead when reading NVCM/Flash pages. Reviewing Figure 26 shows how the data is presented during a multiple page read request. When the page count is three, and the Page Address Pointer is 0000, the I²C interface will return Page 0, 16 undefined bytes, Page 0, 4 dummy bytes, and Page 1. Reading the final four dummy bytes is optional.

References

- DS1047, MachXO3 Family Data Sheet

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
March 2017	2.1	Updated the MachXO3L/LF Features section. In the MachXO3L multi-time programmability feature, changed “two times” to “nine times”.
		Updated the Bitstream/PROM Sizes section. Revised Table 2, Maximum Configuration Bits. — Added 121 Ball Package to MachXO3L/LF-640E device. — Updated values.
		Updated the Feature Row section. — Changed “it can be reprogrammed up to eight times.” to “it can be programmed nine times.” — Changed “MachXO3L reserves eight times” to “MachXO3L reserves nine times”.
December 2016	2.0.	Updated WISHBONE Configuration Mode (MachXO3LF Only) section. Removed reference to Appendix C.
		Updated Reading NVCM/Flash Pages section. Added content on restriction to be observed when using the WISHBONE interface to read the configuration flash or UFM.
September 2016	1.9	Updated Dual Boot Configuration Mode section. Added paragraph on the use of Dual Boot Configuration Mode with MachXO3LF SED and SEC features.
April 2016	1.8	Updated Bitstream/PROM Sizes section. Added bitstream sizes for MachXO3L/LF-9400 to Table 2, Maximum Configuration Bits.
		Updated Feature Row section. Added password security features to Table 4, MachXO3L Feature Row Elements.
		Updated Master SPI Configuration Mode (MSPI) section. Removed “RC delay to PROGRAMN” workaround.
		Updated Dual Boot Configuration Mode section. Mentioned DUAL-BOOTGOLDEN configuration in introductory paragraph.
		Updated Password section.
		Updated Bitstream Generation Options section. Added DUALBOOT-GOLDEN feature.
		Updated Security Options section. Added BACKGROUND_RECONFIG feature.
		Updated NVCM/Flash Programming section. Updated Table 19, Number of Pages of NVCM/Flash Memory for the MachXO3 Family.
		Updated MachXO3 NVCM/Flash Programming Flow section. Added Password shift decision to Figure 20, MachXO3 NVCM/Flash Memory Programming Flow.
		Updated MachXO3 Programming Commands section. Added Password commands to Table 21, MachXO3 sysCONFIG Programming Commands.

Date	Version	Change Summary
		Updated Memory Space Accessibility section. In Table 5, MachXO3L/LF Programming and Configuration Ports, Internal interface information is added.
		Updated Dual Boot Configuration Mode section. Added MachXO3LF information.
		Added WISHBONE Configuration Mode (MachXO3LF Only) section.
		Updated Bitstream Generation Options section. Added CFG_EBRUFM (MachXO3LF) and CFGUFM (MachXO3LF) descriptions.
		Added MachXO3 Slave SPI SRAM Configuration Flow section.
		Updated I2C Configuration Mode section. Added new EFB instantiation requirement for I^2C configuration port access per Product Bulletin PB1412.
		Updated MachXO3 NVCM/Flash Programming Flow section. Revised Figure 21, MachXO3 Slave SPI SRAM Configuration Flow: — Added notes regarding EFB instantiation requirement for I^2C configuration port access.
		Updated MachXO3 Programming Commands section. Revised Table 21, MachXO3 sysCONFIG Programming Commands. Added Configure SRAM [LSC_BITSTREAM_BURST] command.
October 2014	1.4	Updated Reading NVCM Pages section. Added information on retrieval delay.
September 2014	1.3	Updated Feature Row section. — Added Figure 3, Feature Row Example. — Added Table 3, Feature Row Option and Diamond Spreadsheet View. — Updated Table 4, MachXO2 Feature Row Elements. Changed I^2C Slave Address feature to I^2C Programmable Primary Configuration Address and updated default mode state information.

Date	Version	Change Summary
July 2014	1.2	Product name/trademark adjustment.
		Updated MachXO3L Features and Definition of Terms sections. Removed background programming information.
		Updated Memory Space Accessibility section. Removed reference to Transparent mode.
		Updated Table 2, Maximum Configuration Bits. Added devices.
		Updated Table 3, MachXO3L Feature Row Elements. Revised feature to Config NVCM OTP.
		Updated Table 5, Default State of the sysCONFIG Pins. Revised PROGRAMN pin information.
		Updated Table 6, Default State in Diamond for Each Port. Revised SLAVE_SPI_PORT default state.
		Updated Master SPI Configuration Mode (MSPI) section. Added information on SPI Flash POR and MachXO3L POR conditions. Added Figure 8, RC Delay.
		Updated Slave SPI Mode (SSPI) section. Removed reference to transparent operations.
		Updated I^2C Configuration Mode section. Revised NVCM and Feature Row programming information.
		Updated JTAG Mode section. Removed reference to transparent NVCM programming.
		Added Software Selectable Options section.
		Added Advanced Configuration Information section.
		Updated Figure 16, JEDEC File Example. Revised NOTE DEVICE NAME to LCMXO3L-1300E-6CSFBGA256.
April 2014	01.1	Corrected typos.
February 2014	01.0	Initial release.