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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	20.48MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	9
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 32
Voltage - Supply (Vcc/Vdd)	3.5V ~ 18V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7032bstz-88

ADUC7032-8L* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

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DOCUMENTATION

Application Notes

- AN-946: Flash/EE Memory Programming via LIN—Protocol 6

Data Sheet

- ADuC7032-8L: Integrated Precision Battery Sensor for Automotive System Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

DESIGN RESOURCES

- ADUC7032-8L Material Declaration
- PCN-PDN Information
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REVISION HISTORY

11/10—Rev. 0 to Rev. A

Changed ±4.68 mV to ±9.375 mV, Table 32 42
Changes to Timers Section 69
Added Synchronization of Timers Across Asynchronous Clock Domains Section 70
Added Figure 32 and Figure 33; Renumbered Sequentially 70
Added Programming the Timers Section, Halting Timer2 Section, Starting Timer2 Section, and Example Code Section 71
Updated Outline Dimensions 117
Changes to Ordering Guide 117

8/07—Revision 0: Initial Version

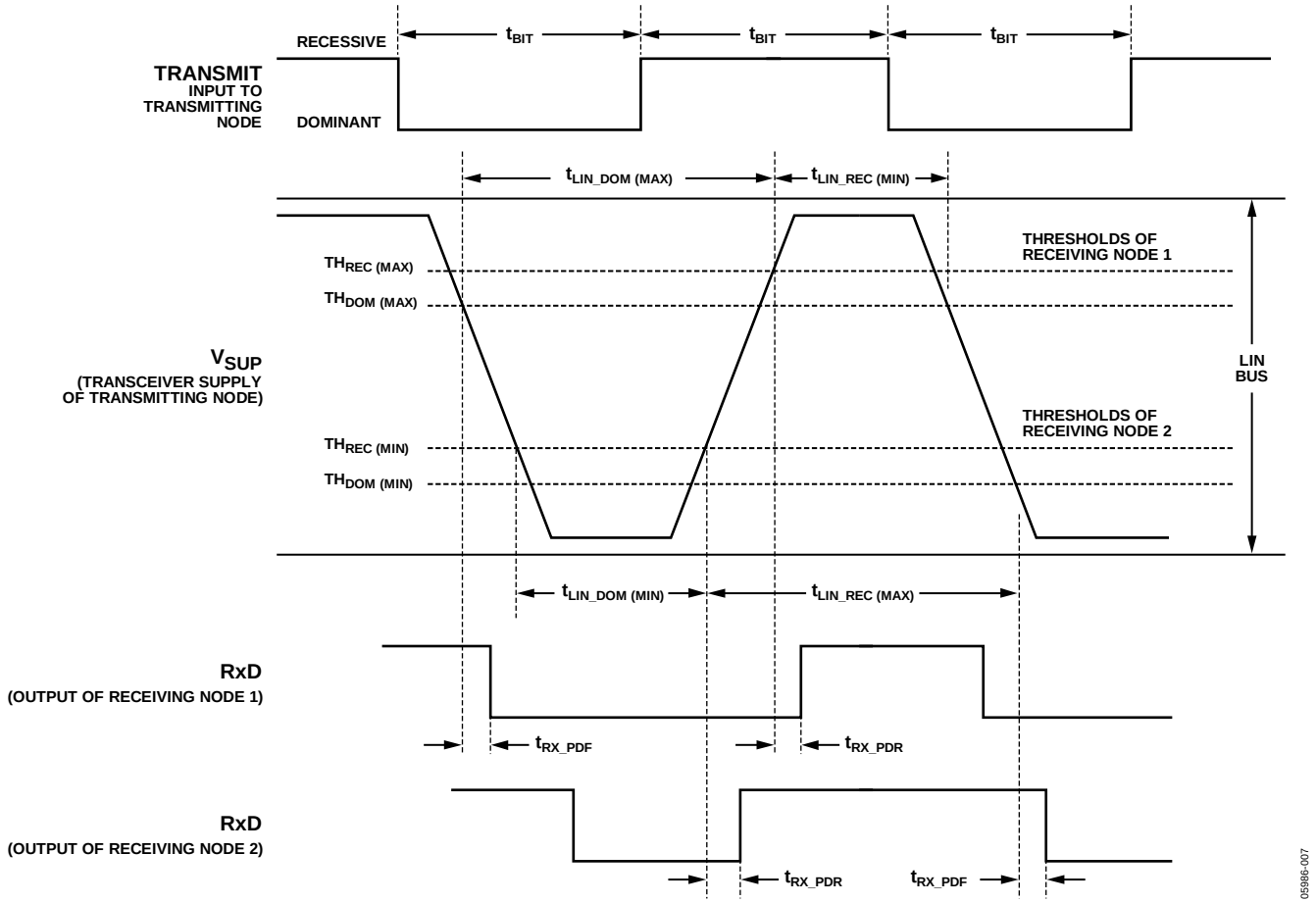

Figure 7. LIN 2.0 Timing Specifications

Pin No.	Mnemonic	Type[1]	Description
6	TCK	I	JTAG Test Clock. This clock input pin is one of the standard 5-pin JTAG debug ports on the part. It is an input pin only, and it has an internal, weak, pull-up resistor. When not in use, this pin remains unconnected.
7	TDI	I	JTAG Test Data Input. This data input pin is one of the standard 5-pin JTAG debug ports on the part. It is an input pin only, and it has an internal, weak, pull-up resistor. When not in use, this pin remains unconnected.
8, 34, 35	DGND	S	Ground Reference for On-Chip Digital Circuits.
9, 16, 17, 23, 25, 26, 32, 38, 39, 40, 43, 45	NC		No Connect. This pin is not connected internally but is reserved for possible future use. Therefore, this pin should not be connected externally. NC pins can be grounded, if required.
10	TDO	O	JTAG Test Data Output. This data output pin is one of the standard 5-pin JTAG debug ports on the part. It is an output pin only. At power-on, this output is disabled and pulled high via an internal, weak, pull-up resistor. When not in use, this pin remains unconnected.
11	NTRST	I	JTAG Test Reset. This reset input pin is one of the standard 5-pin JTAG debug ports on the part. It is an input pin only, and it has an internal, weak, pull-down resistor. When not in use, this pin remains unconnected. It is also monitored by the on-chip kernel to enable LIN boot load mode.
12	TMS	I	JTAG Test Mode Select. This mode select input pin is one of the standard 5-pin JTAG debug ports on the part. It is an input pin only, and it has an internal, weak, pull-up resistor. When not in use, this pin remains unconnected.
13	VBAT	I	Battery Voltage Input to Resistor Divider.
14	VREF	I	External Reference Input Terminal. If this input is not used, connect it directly to the AGND system ground.
15	GND_SW	S	Switch to Internal Analog Ground Reference. Negative input for external temperature channel and external reference. If this input is not used, connect it directly to the AGND system ground.
18	VTEMP	I	External Pin for NTC/PTC Temperature Measurement.
19	IIN+	I	Positive Differential Input for Current Channel.
20	IIN–	I	Negative Differential Input for Current Channel.
21, 22	AGND	S	Ground Reference for On-Chip Precision Analog Circuits.
24	REG_AVDD	S	Nominal 2.6 V Output from On-Chip Regulator.
27	GPIO_0/IRQ0/$\overline{SS}$	I/O	General-Purpose Digital I/O 0, External Interrupt Request 0, or SPI Interface. By default and after power-on reset, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, it remains unconnected. This multifunction pin can be configured in one of three states, namely General-Purpose Digital I/O 0. External Interrupt Request 0, active high. SPI interface, slave select input.
28	GPIO_1/SCLK	I/O	General-Purpose Digital I/O 1 or SPI Interface. By default and after power-on reset, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, it remains unconnected. This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 1. SPI interface, serial clock input.
29	GPIO_2/MIS0	I/O	General-Purpose Digital I/O 2 or SPI Interface. By default and after power-on reset, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, it remains unconnected.This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 2. SPI interface, master input/slave output pin.
30	GPIO_3/MOSI	I/O	General-Purpose Digital I/O 3 or SPI Interface. By default and after power-on reset, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, it remains unconnected. This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 3. SPI interface, master output/slave input pin.
31	GPIO_4/ECLK	I/O	General-Purpose Digital I/O 4 or Clock Output. By default and after power-on reset, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, it remains unconnected. This programmable digital I/O pin can also be configured to output a 2.56 MHz clock.
33	REG_DVDD	S	Nominal 2.6 V Output from the On-Chip Regulator.

RESET

There are four kinds of reset: external reset, power-on reset, watchdog reset, and software reset. The RSTSTA register indicates the source of the last reset and can be written by user code to initiate a software reset event. The bits in this register can be cleared to 0 by writing to the RSTCLR MMR at 0xFFFF0234.

The bit designations in RSTCLR mirror those of RSTSTA. These registers can be used during a reset exception service routine to identify the source of the reset. The implications of all four kinds of reset event are listed in Table 12.

Table 12. Device Reset Implications

Impact/Reset	Reset External Pins to Default State	Kernel Executed	Reset All External MMRs (Excluding RSTSTA)	Reset All High Voltage Indirect Registers	Peripherals Reset	RAM Valid[1]	RSTSTA (Status After Reset Event)
POR[1]	Yes	Yes	Yes	Yes	Yes	Yes/No[2]	RSTSTA[0] = 1
Watchdog Reset	Yes	Yes	Yes	Yes	Yes	Yes	RSTSTA[1] = 1
Software Reset	Yes	Yes	Yes	Yes	Yes	Yes	RSTSTA[2] = 1
External Reset Pin	Yes	Yes	Yes	Yes	Yes	Yes	RSTSTA[3] = 1

[1] RAM is valid except in the case of a reset following a LIN download.
[2] The impact of RAM is dependent on the contents of HVSTA[6] if LVF is enabled. When LVF is enabled using (HVCFG0[2]), RAM has not been corrupted by the POR reset mechanism if the LVF Status Bit HVSTA[6] = 1. See the Low Voltage Flag (LVF) section for more information.

RSTCLR Register

Name: RSTCLR
Address: 0xFFFF0234
Default Value: 0x00
Access: Write only
Function: This 8-bit write-only register clears the corresponding bit in RSTSTA.

RSTSTA Register

Name: RSTSTA
Address: 0xFFFF0230
Default Value: 0x01
Access: Read/write
Function: This 8-bit register indicates the source of the last reset event and can be written by user code to initiate a software reset.

Table 13. RSTCLR/RSTSTA MMR Bit Designations

Bit	Description
7 to 4	Not Used. These bits are not used and always read as 0.
3	External Reset. Set to 1 automatically when an external reset occurs. Cleared by setting the corresponding bit in RSTCLR.
2	Software Reset.[1] Set to 1 by user code to generate a software reset. Cleared by setting the corresponding bit in RSTCLR.
1	Watchdog Timeout. Set to 1 automatically when a watchdog timeout occurs. Cleared by setting the corresponding bit in RSTCLR.
0	Power-On Reset. Set automatically when a power-on reset occurs. Cleared by setting the corresponding bit in RSTCLR.

[1] If the software reset bit in RSTSTA is set, any write to RSTCLR that does not clear this bit generates a software reset.

FEE0MOD and FEE1MOD Registers

Name: FEE0MOD and FEE1MOD
Address: 0xFFFF0E04 and 0xFFFF0E84
Default Value (Both Registers): 0x00
Access: Read/write
Function: These registers are written by user code to configure the mode of operation of the Flash/EE memory controllers.

Table 16. FEE0MOD and FEE1MOD MMR Bit Designations

Bit	Description[1]
15 to 7	Not Used. These bits are reserved for future functionality and should be written as 0 by user code.
6 to 5	Flash/EE Security Lock Bits. These bits must be written as [6:5] = 10 to complete the Flash security protect sequence.
4	Flash/EE Controller Command Complete Interrupt Enable. Set to 1 by user code to enable the Flash/EE controller to generate an interrupt upon completion of a Flash/EE command. Cleared to disable the generation of a Flash/EE interrupt upon completion of a Flash/EE command.
3	Flash/EE Erase/Write Enable. Set by user code to enable the Flash/EE erase and write access via FEExCON. Cleared by user code to disable the Flash/EE erase and write access via FEExCON.
2	Reserved. Should be written as 0.
1	Flash/EE Controller Abort Enable. Set to 1 by user code to enable the Flash/EE controller abort functionality.
0	Reserved. Should be written as 0.

[1] x is 0 or 1 to designate Flash/EE Block 0 or Flash/EE Block 1.

FLASH/EE MEMORY SECURITY

The 94 kB of Flash/EE memory available to the user can be read-protected and write-protected using the FFE0HID and FEE1HID registers.

In Block 0, the FEE0HID MMR protects the 30 kB of Flash/EE memory. Bit 0 to Bit 28 of this register protect Page 0 to Page 57 from writing. Each bit protects two pages, that is, 1 kB. Bit 29 to Bit 30 protect Page 58 and Page 59, respectively; that is, each bit write-protects a single page of 512 bytes. The MSB of this register (Bit 31) protects Block 0 from being read through JTAG.

The FEE0PRO register mirrors the bit definitions of the FEE0HID MMR. The FEE0PRO MMR allows user code to lock the protection or security configuration of the Flash/EE memory so that the protection configuration is automatically loaded on subsequent power-on or reset events.

This flexibility allows the user to set and test protection settings temporarily using the FEE0HID MMR and subsequently lock the required protection configuration (using FEE0PRO) when shipping protection systems into the field.

In Block 1 (64 kB), the FEE1HID MMR protects the 64 kB of Flash/EE memory. Bit 0 to Bit 29 of this register protect Page 0 to Page 119 from writing. Each bit protects four pages, that is, 2 kB. Bit 30 protects Page 120 to Page 127; that is, Bit 30 write-protects eight pages of 512 bytes. The MSB of this register (Bit 31) protects Flash/EE Block 1 from being read through JTAG.

As with Block 0, the FEE1PRO register mirrors the bit definitions of the FEE1HID MMR. The FEE1PRO MMR allows user code to lock the protection or security configuration of the Flash/EE memory so that the protection configuration is automatically loaded on subsequent power-on or reset events.

FLASH/EE MEMORY RELIABILITY

The Flash/EE memory array on the part is fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as follows:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

In reliability qualification, every halfword (16-bits wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. As shown in Table 1, the Flash/EE memory endurance qualification of the parts is carried out in accordance with JEDEC Retention Lifetime Specification A117. The results allow the specification of a minimum endurance figure over supply and temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal JEDEC Retention Lifetime Specification A117 at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. Also, note that retention lifetime, based on an activation energy of 0.6 eV, derates with TJ, as shown in Figure 12.

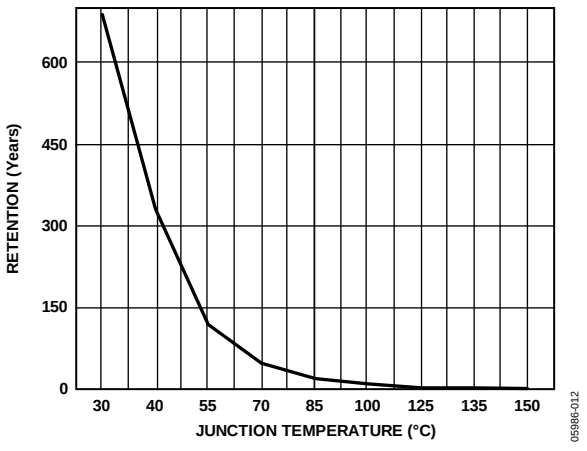

Figure 12. Flash/EE Memory Data Retention

CODE EXECUTION TIME FROM SRAM AND FLASH/EE

This section describes SRAM and Flash/EE memory access times during execution for applications where execution time is critical.

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle. However, if the instruction involves reading or writing data to memory, one or two extra cycles must be added. If the data is in SRAM, one extra cycle is needed. If the data is in Flash/EE, two extra cycles are needed to get the 32-bit data from Flash/EE.

A control flow instruction (for example, a branch instruction) takes one cycle to fetch and two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

In Thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

In ARM mode, with CD = 0, two cycles are needed to fetch the 32-bit instructions. With CD > 0, no extra cycles are required for the fetch because the Flash/EE memory continues to be clocked at full speed. In addition, some dead time is needed before accessing data for any value of CD bits.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline if CD = 0.

A data processing instruction involving only the core register does not require any extra clock cycles. Data transfer instructions are more complex and are summarized in Table 19.

Table 19. Typical Execution Cycles in ARM/Thumb Mode

Instruction	Fetch Cycle	Dead Time	Data Access
LD	2/1	1	2
LDH	2/1	1	1
LDM/POP	2/1	N	2 × N
STR	2/1	1	2 × 50 µs
STRH	2/1	1	50 µs
STM/PUSH	2/1	N	2 × N × 50 µs

With 1 < N ≤ 16, N is the number of registers to load or store in the multiple load/store instruction.

By default, Flash/EE code execution is suspended during any Flash/EE erase or write cycle. A page (512 bytes) erase cycle takes 20 ms, and a write (16 bits) word command takes 50 µs. However, the Flash/EE memory controller allows erase/write cycles to be aborted if the ARM core receives an enabled interrupt during the current Flash/EE erase/write cycle. The ARM7 can, therefore, immediately service the interrupt and then return to repeat the Flash/EE command. The abort operation typically takes 10 clock cycles. If the abort operation is not feasible, it is possible to run Flash/EE memory programming code and the relevant interrupt routines from SRAM, allowing the core to service the interrupt immediately.

Bit	Description
4	Current Channel ADC Comparator Threshold. Valid only if the current channel ADC comparator is enabled via the ADCCFG MMR. Set by hardware if the absolute value of the I-ADC conversion result exceeds the value written in the ADC0TH MMR. If the ADC threshold counter is used (ADC0TCL), this bit is set only when the specified number of I-ADC conversions equals the value in the ADC0THV MMR.
3	Current Channel ADC Overrange Bit. If the overrange detect function is enabled via the ADCCFG MMR, this bit is set by hardware if the I-ADC input is grossly (>30% approximately) overranged. This bit is updated every 125 µs. When set, this bit can only be cleared by software when ADCCFG[2] is cleared to disable the function or the ADC gain is changed via the ADC0CON MMR.
2	Temperature Conversion Result-Ready Bit. If the temperature channel ADC is enabled, this bit is set by hardware as soon as a valid temperature conversion result is written in the temperature data register (ADC2DAT MMR). Cleared by reading either ADC2DAT or ADC0DAT.
1	Voltage Conversion Result-Ready Bit. If the voltage channel ADC is enabled, this bit is set by hardware as soon as a valid voltage conversion result is written in the voltage data register (ADC1DAT MMR). Cleared by reading either ADC1DAT or ADC0DAT.
0	Current Conversion Result-Ready Bit. If the current channel ADC is enabled, this bit is set by hardware as soon as a valid current conversion result is written in the current data register (ADC0DAT MMR). Cleared by reading ADC0DAT.

ADC Interrupt Source Enable Register

Name: ADCMSKI
Address: 0xFFFF0504
Default Value: 0x00
Access: Read/write
Function: This register allows the ADC interrupt sources to be enabled individually. The bit positions in this register are the same as the lower eight bits in the ADCSTA MMR. If a bit is set by user code to 1, the respective interrupt is enabled. By default, all bits are set to 0, meaning that all ADC interrupt sources are disabled.

Current Channel ADC Data Register

Name: ADC0DAT
Address: 0xFFFF0520
Default Value: 0x0000
Access: Read only
Function: This current channel ADC data MMR holds the 16-bit conversion result from the I-ADC. The ADC does not update this MMR if the ADC conversion result-ready bit (ADCSTA[0]) is set. A read of this MMR by the MCU clears all asserted ready flags (ADCSTA[2:0]).

Voltage Channel Data Register

Name: ADC1DAT
Address: 0xFFFF0524
Default Value: 0x0000
Access: Read only
Function: This V-ADC data MMR holds the 16-bit conversion result from the V-ADC. The ADC does not update this MMR if the voltage conversion result-ready bit (ADCSTA[1]) is set. If I-ADC is not active, a read of this MMR by the MCU clears all asserted ready flags (ADCSTA[2:1]).

Temperature Channel ADC Data Register

Name: ADC2DAT
Address: 0xFFFF0528
Default Value: 0x0000
Access: Read only
Function: This T-ADC data MMR holds the 16-bit conversion result from the T-ADC. The ADC does not update this MMR if the temperature conversion result-ready bit (ADCSTA[2]) is set. A read of this MMR clears ADCSTA[2].

ADC FIFO Register

Name: ADCFIFO
Address: 0xFFFF052C
Default Value: 0x0000
Access: Read only
Function: This 32-bit, read-only register returns the value of the I-ADC and V-ADC conversion result held in the FIFO location currently pointed to by the FIFO read pointer. The low 16 bits [15:0] of this 32-bit word are the I-ADC result, and the high 16 bits [31:16] are the V-ADC result. The FIFO function is enabled via the ADCCFG[1] bit, and three flags available in the ADCSTA register allow user code to monitor and read the FIFO contents.

Current Channel ADC Offset Calibration Register

Name: ADC0OF
Address: 0xFFFF0530
Default Value: Part-specific, factory programmed
Access: Read/write
Function: This ADC offset MMR holds a 16-bit offset calibration coefficient for the I-ADC. The register is configured at power-on with a factory default value. However, this register is automatically overwritten if an offset calibration of the I-ADC is initiated by the user via bits in the ADCMDE MMR. User code can write to this calibration register only if the ADC is in idle mode. An ADC must be enabled and in idle mode before being written to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

Voltage Channel ADC Offset Calibration Register

Name: ADC1OF
Address: 0xFFFF0534
Default Value: Part-specific, factory programmed
Access: Read/write
Function: This V-ADC offset MMR holds a 16-bit offset calibration coefficient for the voltage channel. The register is configured at power-on with a factory default value. However, this register is automatically overwritten if an offset calibration of the voltage channel is initiated by the user via bits in the ADCMDE MMR. User code can write to this calibration register only if the ADC is in idle mode. An ADC must be enabled and in idle mode before being written to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

Temperature Channel ADC Offset Calibration Register

Name: ADC2OF
Address: 0xFFFF0538
Default Value: Part-specific, factory programmed
Access: Read/write
Function: This T-ADC offset MMR holds a 16-bit offset calibration coefficient for the temperature channel. The register is configured at power-on with a factory default value. However, this register is automatically overwritten if an offset calibration of the temperature channel is initiated by the user via bits in the ADCMDE MMR. User code can write to this calibration register only if the ADC is in idle mode. An ADC must be enabled and in idle mode before writing to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

For example, with the chop bit ADCFLT[15] set to 1, increasing the SF value (ADCFLT[6:0]) to 0x1F (31 decimal) and selecting an AF value (ADCFLT[13:8]) of 0x16 (22 decimal) results in an ADC throughput of 10 Hz. The frequency response in this case is shown in Figure 23.

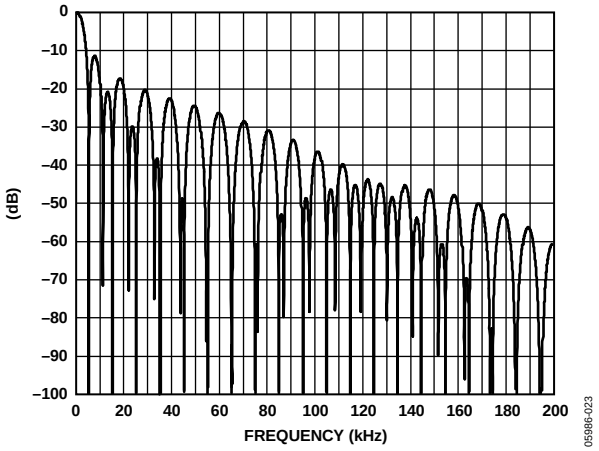

Figure 23. Typical Digital Filter Response at f_{ADC} = 10 Hz (ADCFLT = 0x961F)

Changing SF to 0x1D and setting AF to 0x3F, again with the chop bit enabled, configures the ADC into its minimum throughput rate in normal mode of 4 Hz. The digital filter frequency response with this configuration is shown in Figure 24.

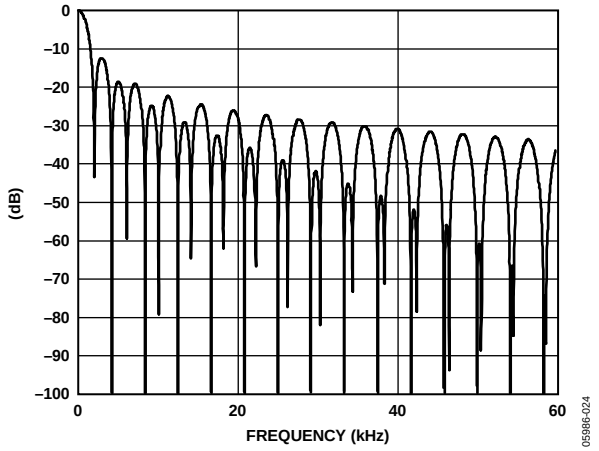

Figure 24. Typical Digital Filter Response at f_{ADC} = 4 Hz (ADCFLT = 0xBF1D)

In ADC low power mode, the ADC Σ-Δ modulator clock is no longer driven at 512 kHz but is driven directly from the on-chip low power (131 kHz) oscillator. Subsequently, for the same ADCFLT configurations in normal mode, all filter values should be scaled by a factor of approximately 4. This means that it is possible to configure the ADC for 1 Hz throughput in low power mode. The filter frequency response for this configuration is shown in Figure 25.

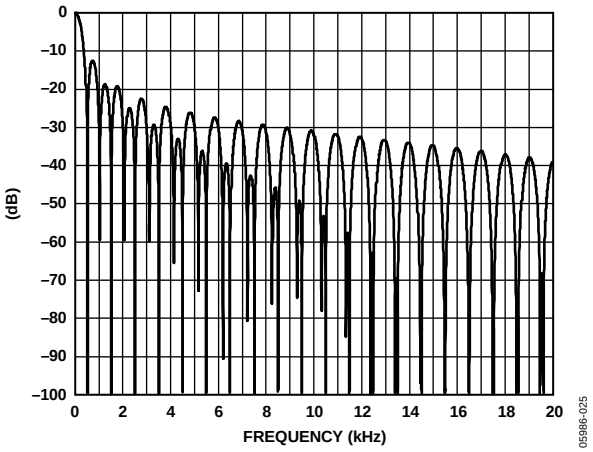

Figure 25. Typical Digital Filter Response at f_{ADC} = 1 Hz (ADCFLT = 0xBD1F)

In general, it is possible to program different values of SF and AF in the ADCFLT register and achieve the same ADC update rate. In practical terms, the trade-off with any value of ADCFLT is frequency response vs. ADC noise. For optimum filter response and ADC noise when using combinations of SF and AF, first choose an SF in the range of 16 to 40 (decimal) or 0x10 to 0x28. Then increase the AF value to achieve the required ADC throughput.

Table 44 shows some common ADCFLT configurations.

Table 44. Common ADCFLT Configurations

ADC Mode	SF	AF	Other Configuration	ADCFLT	f_{ADC}	t_{SETTLE}
Normal	0x1D	0x3F	Chop on	0xBF1D	4 Hz	0.5 sec
	0x1F	0x16	Chop on	0x961F	10 Hz	0.2 sec
	0x07	0x00	None	0x0007	1 kHz	3 ms
	0x07	0x00	Sinc3 modify	0x0087	1 kHz	3 ms
	0x03	0x00	Running average	0x4003	2 kHz	2 ms
	0x00	0x00	Running average	0x4000	8 kHz	0.5 ms
Low Power	0x10	0x03	Chop on	0x8310	20 Hz	100 ms
	0x10	0x09	Chop on	0x8910	10 Hz	200 ms
	0x1F	0x3D	Chop on	0xBD1F	1 Hz	2 sec

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 16 interrupt sources on the ADuC7032-8L that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals such as the ADC, UART, and so on. The ARM7TDMI CPU core recognizes interrupts as only one of two types: a normal interrupt request (IRQ) and a fast interrupt request (FIQ). All the interrupts can be masked separately.

The control and configuration of the interrupt system are managed through nine interrupt-related registers, four dedicated to IRQ and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ register represent the same interrupt source, as shown in Table 51.

IRQSTA/FIQSTA should be saved immediately upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

The interrupt generation route through the ARM7TDMI core is shown in Figure 29.

Consider the example of Timer0, which is configured to generate a timeout every 1 ms. After the first 1 ms timeout, FIQSIG/IRQSIG[2] is set and can be cleared only by writing to T0CLRI.

If Timer0 is not enabled in either IRQEN or FIQEN, FIQSTA/IRQSTA[2] is not set and an interrupt does not occur.

If Timer0 is enabled in either IRQEN or FIQEN, then FIQSTA/IRQSTA[2] is set and either an FIQ or an IRQ interrupt occurs.

Note that the IRQ and FIQ interrupt bit definitions in the CPSR control interrupt recognition by the ARM core only, not by the peripherals. For example, if Timer2 is configured to generate an IRQ via IRQEN, the IRQ interrupt bit is set (disabled) in the CPSR, and the ADuC7032-8L is powered down. When an interrupt occurs, the peripherals power up, but the ARM core remains powered down. This is equivalent to POWCON = 0x71. The ARM core can be powered up only by a reset event if this occurs.

Table 51. IRQ/FIQ MMRs Bit Designations

Bit	Description	Comments
0	All interrupts OR'ed (FIQ only).	
1	SWI is not used in IRQEN/CLR and FIQEN/CLR.	
2	Timer0.	See the Timer0—Lifetime Timer section.
3	Timer1.	See the Timer1 section.
4	Timer2 or Wake-Up Timer.	See the Timer2—Wake-Up Timer section.
5	Timer3 or Watchdog Timer.	See the Timer3—Watchdog Timer section.
6	Reserved. Should be written as 0.	
7	LIN Hardware.	See the LIN (Local Interconnect Network) Interface section
8	Flash/EE Interrupt.	See the Flash/EE Control Interface section.
9	PLL Lock.	See the ADUC7032-8L System Clocks section.
10	ADC.	See the 16-Bit, Sigma-Delta Analog-to-Digital Converters section.
11	UART.	See the UART Serial Interface section.
12	SPI Master.	See the Serial Peripheral Interface section.
13	XIRQ0 (GPIO IRQ 0).	See the General-Purpose I/O section.
14	XIRQ1 (GPIO IRQ 1).	See the General-Purpose I/O section.
15	Reserved. Should be written as 0.	
16	IRQ3. High voltage IRQ.	High voltage interrupt; see the High Voltage Peripheral Control Interface section
17	SPI Slave.	
18	XIRQ4 (GPIO IRQ 4).	See the General-Purpose I/O section.
19	XIRQ5 (GPIO IRQ 5).	See the General-Purpose I/O section.

Timer1 Capture Register

Name: T1CAP
Address: 0xFFFF0330
Default Value: 0x00000000
Access: Read/write
Function: This 32-bit register holds the 32-bit value captured by an enabled IRQ event.

Timer1 Control Register

Name: T1CON
Address: 0xFFFF0328
Default Value: 0x01000000
Access: Read/write
Function: This 32-bit MMR configures the mode of operation of Timer1.

Table 55. T1CON MMR Bit Designations

Bit	Description
31 to 24	Timer1 8-Bit Postscalar. By writing to these 8 bits, a value is loaded into the postscalar. Writing 0 to these bits is interpreted as a 1. By reading these 8 bits, the current value of the counter is loaded.
23	Timer1 Enable Postscalar. Set to enable Timer1 postscalar. If enabled, an interrupt is generated after T1CON[31:24] periods, as defined by T1LD. Cleared to disable Timer1 postscalar.
22 to 20	Reserved. This bit is reserved and should be written as 0 by user code.
19	Postscalar Compare Flag. Set if the number of Timer1 overflows is equal to the number written to the postscalar.
18	Timer1 Interrupt Source. Set to select interrupt generation from postscalar counter. Cleared to select interrupt generation direct from Timer1.
17	Event Select Bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16 to 12	Event Select Range, 0 to 31. The events are described in Table 53.
11 to 9	Clock Select. 000 = core clock (default). 001 = low power 32.768 kHz oscillator. 010 = GPIO_8. 011 = GPIO_5.
8	Count Up. Set by user for Timer1 to count up. Cleared by user for Timer1 to count down (default).
7	Timer1 Enable Bit. Set by user to enable Timer1. Cleared by user to disable Timer1 (default).
6	Timer1 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5 to 4	Format. 00 = binary (default). 01 = reserved. 10 = hours:minutes:seconds:hundredths—23 hours to 0 hour. 11 = hours:minutes:seconds:hundredths—255 hours to 0 hour.
3 to 0	Prescalar. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256. 1111 = source clock/32,768.

Timer2 Control Register

Name: T2CON
Address: 0xFFFF0348
Default Value: 0x0000
Access: Read/write
Function: This 32-bit MMR configures the mode of operation of Timer2.

Table 56. T2CON MMR Bit Designations

Bit	Description
31 to 11	Reserved.
10 to 9	Clock Source Select. 00 = core clock (default). 01 = low power 32.768 kHz oscillator. 10 = external 32.768 kHz watch crystal. 11 = precision 32.768 kHz oscillator.
8	Count Up. Set by user for Timer2 to count up. Cleared by user for Timer2 to count down (default).
7	Timer2 Enable Bit. Set by user to enable Timer2. Cleared by user to disable Timer2 (default).
6	Timer2 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default).
5 to 4	Format. 00 = binary (default). 01 = reserved. 10 = hours:minutes:seconds:hundredths—23 hours to 0 hour. 11 = hours:minutes:seconds:hundredths—255 hours to 0 hour.
3 to 0	Prescalar. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256 (should be used in conjunction with Timer2 Format 10 and Timer2 Format 11). 1111 = source clock/32,768.

GPIO Port0 Clear Register

Name: GP0CLR
Address: 0xFFFF0D28
Access: Write only
Function: This 32-bit MMR allows user code to individually bit address external GPIO pins to clear them low only. User code can do this via the GP0CLR MMR without needing to modify or maintain the status of any other GPIO pins, as user code needs to do when using GP0DAT.

Table 68. GP0CLR MMR Bit Designations

Bit	Description
31 to 21	Reserved. These bits are reserved and should be written as 0 by user code.
20	Port0.4 Clear Bit. Set to 1 by user code to clear the external GPIO_4 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_4 pin.
19	Port0.3 Clear Bit. Set to 1 by user code to clear the external GPIO_3 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_3 pin.
18	Port0.2 Clear Bit. Set to 1 by user code to clear the external GPIO_2 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_2 pin.
17	Port0.1 Clear Bit. Set to 1 by user code to clear the external GPIO_1 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_1 pin.
16	Port0.0 Clear Bit. Set to 1 by user code to clear the external GPIO_0 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_0 pin.
15 to 0	Reserved. These bits are reserved and should be written as 0 by user code.

GPIO Port1 Clear Register

Name: GP1CLR
Address: 0xFFFF0D38
Access: Write only
Function: This 32-bit MMR allows user code to individually bit address external GPIO pins to clear them low only. User code can do this via the GP1CLR MMR without needing to modify or maintain the status of any other GPIO pins, as user code needs to do when using GP1DAT.

Table 69. GP1CLR MMR Bit Designations

Bit	Description
31 to 18	Reserved. These bits are reserved and should be written as 0 by user code.
17	Port1.1 Clear Bit. Set to 1 by user code to clear the external GPIO_6 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_6 pin.
16	Port1.0 Clear Bit. Set to 1 by user code to clear the external GPIO_5 pin low. If user software clears this bit to 0, it has no effect on the external GPIO_5 pin.
15 to 0	Reserved. These bits are reserved and should be written as 0 by user code.

High Voltage Monitor Register

Name: HVMON
Address: Indirectly addressed via the HVCON high voltage interface
Default Value: 0x00
Access: Read only
Function: This 8-bit, read-only register reflects the current status of enabled high voltage related circuits and functions on the ADuC7032-8L. This register is not an MMR and does not appear in the MMR memory map. It is accessed via the HVCON registered interface, and data is read back from this register via HVDAT.

Table 77. HVMON Bit Designations

Bit	Description
7	WU Pin Diagnostic Readback. Once enabled via HVCFG1[4], this read-only bit reflects the state of the external WU (wake-up) pin.
6	Overtemperature. This bit is 0 if a thermal shutdown event has not occurred. This bit is 1 if a thermal shutdown event has occurred.
5	Reserved. This bit should not be used and is reserved for future use.
4	Buffer Enabled. This bit is 0 if the voltage channel ADC input buffer is disabled. This bit is 1 if the voltage channel ADC input buffer is enabled.
3	Low Voltage Flag Status Bit. (Valid only if enabled via HVCFG0[2].) This bit is 0 on power-up if REG_DVDD has dropped below 2.1 V. In this state, RAM contents can be deemed corrupt. This bit is 1 on power-up if REG_DVDD has not dropped below 2.1 V. In this state, RAM contents can be deemed valid. It is cleared only by re-enabling the low voltage flag in HVCFG0[2].
2	LIN Short-Circuit Status Flag. This bit is 0 if the LIN driver is operating normally. This bit is 1 if the LIN driver has experienced a short-circuit condition and is cleared automatically by writing to HVCFG1[3].
1	Reserved. This bit should not be used and is reserved for future use.
0	WU Short-Circuit Status Flag. This bit is 0 if the WU driver is operating normally. This bit is 1 if the WU driver has experienced a short-circuit condition.

HANDLING INTERRUPTS FROM THE HIGH VOLTAGE PERIPHERAL CONTROL INTERFACE

An interrupt controller is also integrated with the high voltage circuits. If enabled via IRQEN[16], one of five high voltage sources can assert the high voltage interrupt (IRQ3) signal and interrupt the MCU core.

While the MCU response to this interrupt event is, as normal, to vector to the IRQ or FIQ interrupt vector address, the high voltage interrupt controller simultaneously and automatically loads the current value of the high voltage status register (HVSTA) into the HVDAT register. During this time the busy bit, HVCON[0], is set to indicate the transfer is in progress and clears after 10 µs to indicate the HVSTA contents are available in HVDAT.

The interrupt handler can, therefore, poll the busy bit in HVCON until it deasserts and then read the HVDAT register.

At this time, HVDAT holds the value of the HVSTA register. The status flags can then be interrogated to determine the exact source of the high voltage interrupt and take appropriate action.

LOW VOLTAGE FLAG (LVF)

The ADuC7032-8L features a low voltage flag (LVF) that, when enabled, allows the user to monitor REG_DVDD. When enabled via HVCFG0[2], the low voltage flag can be monitored through HVMON[3]. If REG_DVDD drops below 2.1 V, HVMON[3] is cleared. If REG_DVDD drops below 2.1 V, the RAM contents are corrupted. Once the low voltage flag is enabled, it is reset only by REG_DVDD dropping below 2.1 V or the disabling of the LVF functionality using HVCFG0[2].

HIGH VOLTAGE DIAGNOSTICS

It is possible to diagnose fault conditions on the WU and LIN bus, as detailed in Table 78.

Table 78. High Voltage Diagnostics

High Voltage Pin	Fault Condition	Method	Result
LIN	Short between LIN and VBAT	Drive LIN low	LIN short-circuit interrupt is generated after 20 µs if more than 100 mA is drawn continuously.
	Short between LIN and GND	Drive LIN high	LIN readback low.
WU	Short between WU and VBAT	Drive WU low	Readback high.
	Short between WU and GND	Drive WU high	WU short-circuit interrupt is generated after 400 µs if more than 200 mA is sourced.
	Open circuit	Enable OC diagnostic resistor with WU disabled	HVMON[7] is cleared if load is connected; HVMON[7] is set if WU is open-circuited.

SPI Control Register

Name: SPICON
Address: 0xFFFF0A10
Default Value: 0x0000
Access: Read/write
Function: This 16-bit MMR configures the serial peripheral interface.

Table 89. SPICON MMR Bit Designations

Bit	Description
15 to 13	Reserved. Should be written as 0.
12	Continuous Transfer Enable. Set by user to enable continuous transfer. In master mode the transfer continues until no valid data is available in the SPITX register. $\overline{SS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until SPITX is empty. Cleared by user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, a new transfer is initiated after a stall period.
11	Loop Back Enable. Set by user to connect MISO to MOSI and test software. Cleared by user to normal mode.
10	Slave Output Enable. Set by user to enable slave output. Cleared by user to disable slave output.
9	Slave Select Input Enable. Set by user in master mode to enable the output.
8	SPIRX Overflow Overwrite Enable. Set by user. The valid data in the RX register is overwritten by the new serial byte received. Cleared by user. The new serial byte received is discarded.
7	SPITX Underflow Mode. Set by user to transmit the previous data. Cleared by user to transmit 0.
6	Transfer and Interrupt Mode (Master Mode). Set by user to initiate transfer with a write to the SPITX register. Interrupt occurs when SPITX is empty. Cleared by user to initiate transfer with a read of the SPIRX register. Interrupt occurs when SPIRX is full.
5	LSB First Transfer Enable Bit. Set by user. The LSB is transmitted first. Cleared by user. The MSB is transmitted first.
4	Reserved. Should be written as 0.
3	Serial Clock Polarity Mode Bit. Set by user. The serial clock idles high. Cleared by user. The serial clock idles low.
2	Serial Clock Phase Mode Bit. Set by user. The serial clock pulses at the beginning of each serial bit transfer. Cleared by user. The serial clock pulses at the end of each serial bit transfer.
1	Master Mode Enable Bit. Set by user to enable master mode. Cleared by user to enable slave mode.
0	SPI Enable Bit. Set by user to enable the SPI. Cleared to disable the SPI.

ADuC7032-8L EXAMPLE SCHEMATIC

This example schematic represents a basic functional circuit implementation. Additional components must be added to ensure the system meets any EMC and other overvoltage/overcurrent compliance requirements.

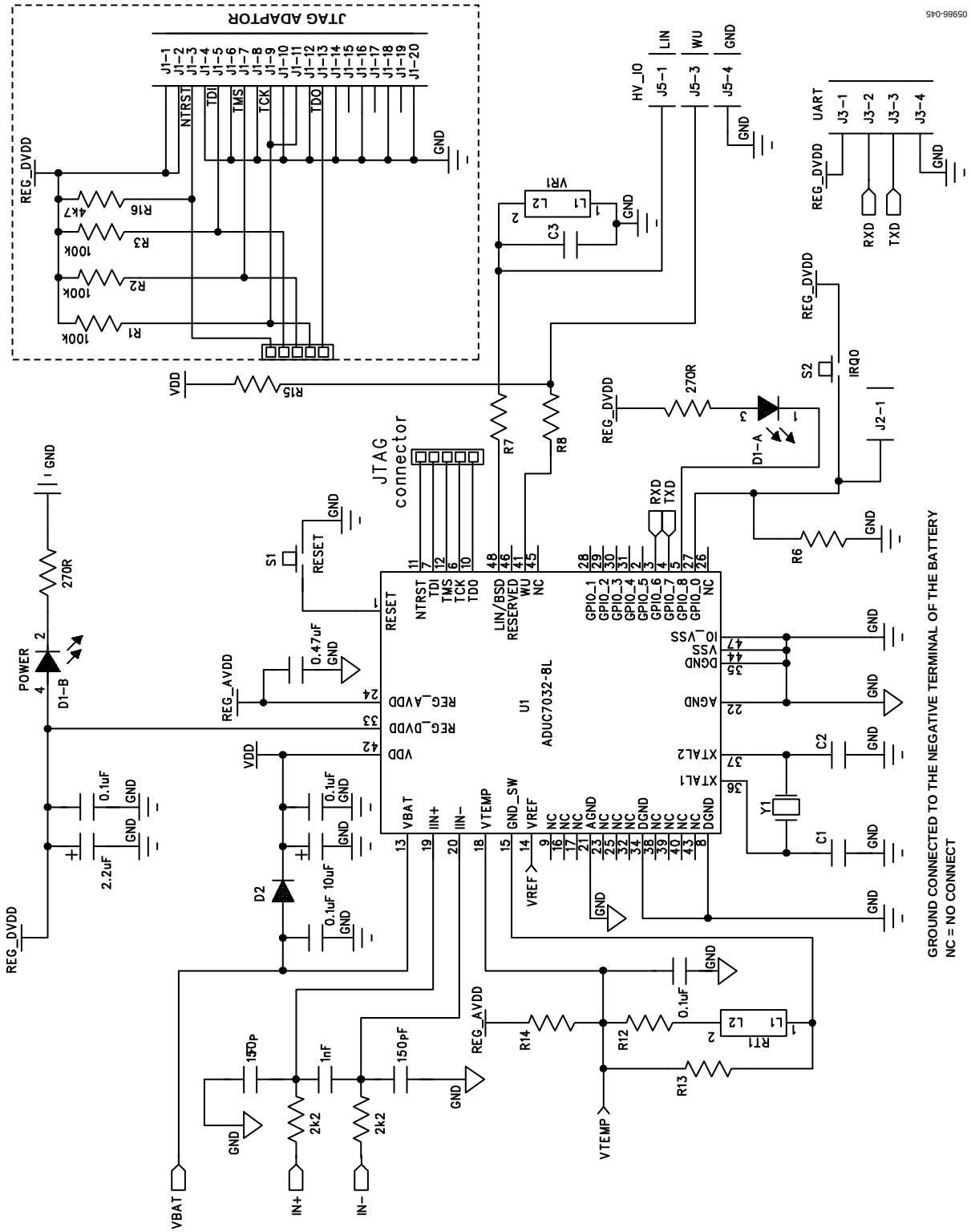

Figure 47. Basic Functional Circuit Implementation

NOTES

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