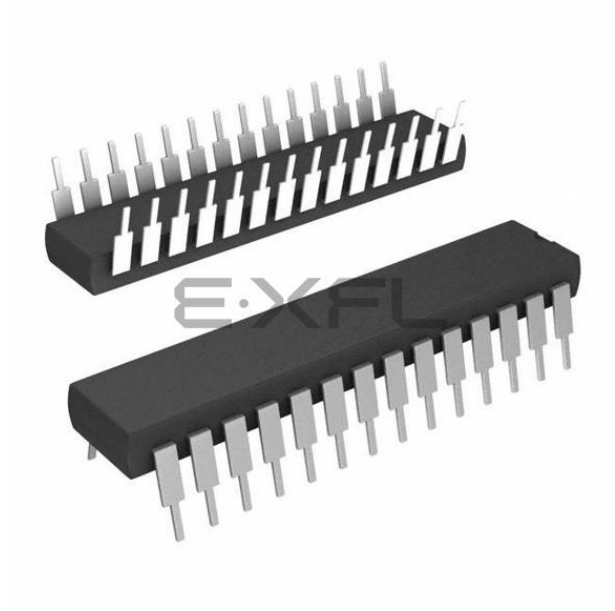


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f2510-e-sp |

**TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F2XXX/4XXX FAMILY**

| Pin Name | During Programming | | |
|---|---|---|---|
| | Pin Name | Pin Type | Pin Description |
| $\overline{MCLR}$/VPP/RE3 | VPP | P | Programming Enable |
| VDD(2) | VDD | P | Power Supply |
| VSS(2) | VSS | P | Ground |
| RB5 | PGM | I | Low-Voltage ICSP™ Input when LVP Configuration bit equals '1'(1) |
| RB6 | PGC | I | Serial Clock |
| RB7 | PGD | I/O | Serial Data |

**Legend:** I = Input, O = Output, P = Power
**Note 1:** See Figure 5-1 for more information.
**2:** All power supply (VDD) and ground (VSS) pins must be connected.

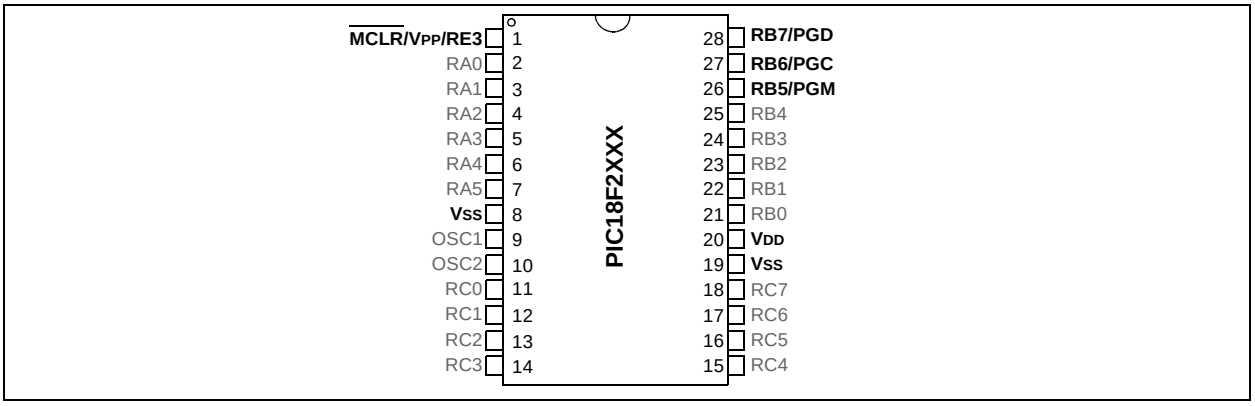
The following devices are included in 28-pin SPDIP, PDIP and SOIC parts:

- PIC18F2221
- PIC18F2321
- PIC18F2410
- PIC18F2420
- PIC18F2423
- PIC18F2450
- PIC18F2455
- PIC18F2458
- PIC18F2480
- PIC18F2510
- PIC18F2515
- PIC18F2520
- PIC18F2523
- PIC18F2525
- PIC18F2550
- PIC18F2553
- PIC18F2580
- PIC18F2585
- PIC18F2610
- PIC18F2620
- PIC18F2680
- PIC18F2682
- PIC18F2685

The following devices are included in 28-pin SSOP parts:

- PIC18F2221
- PIC18F2321

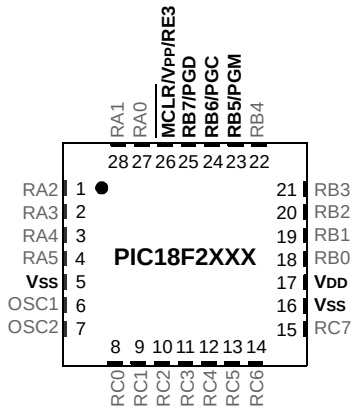
**FIGURE 2-1: 28-Pin SPDIP, PDIP, SOIC,SSOP**



The following devices are included in 28-pin QFN parts:

- PIC18F2221
- PIC18F2321
- PIC18F2410
- PIC18F2420
- PIC18F2423
- PIC18F2450
- PIC18F2480
- PIC18F2510
- PIC18F2520
- PIC18F2523
- PIC18F2580
- PIC18F2682
- PIC18F2685

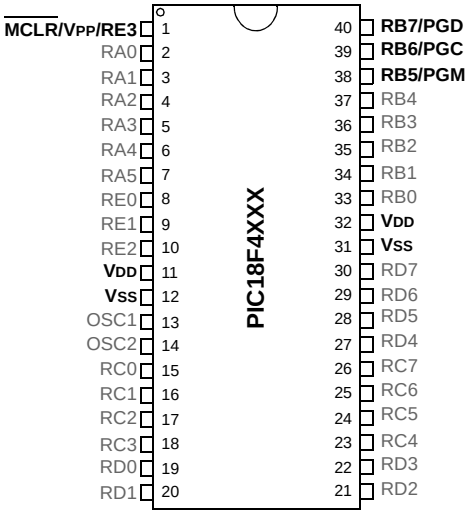
**FIGURE 2-2: 28-Pin QFN**




The following devices are included in 40-pin PDIP parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4515
- PIC18F4520
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

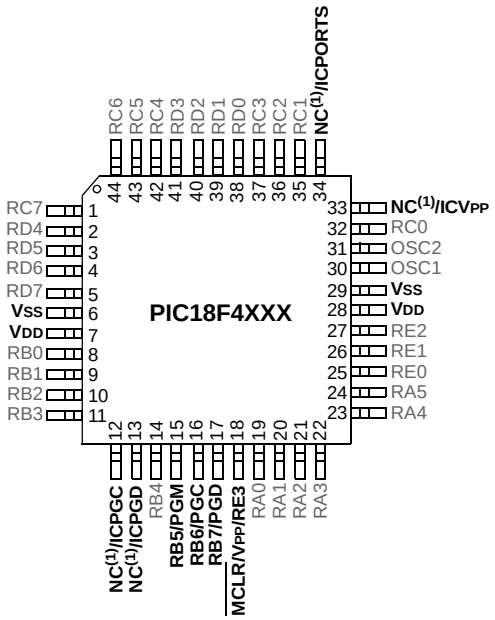
**FIGURE 2-3: 40-Pin PDIP**



The following devices are included in 44-pin TQFP parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4520
- PIC18F4515
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

**FIGURE 2-4: 44-PIN TQFP**

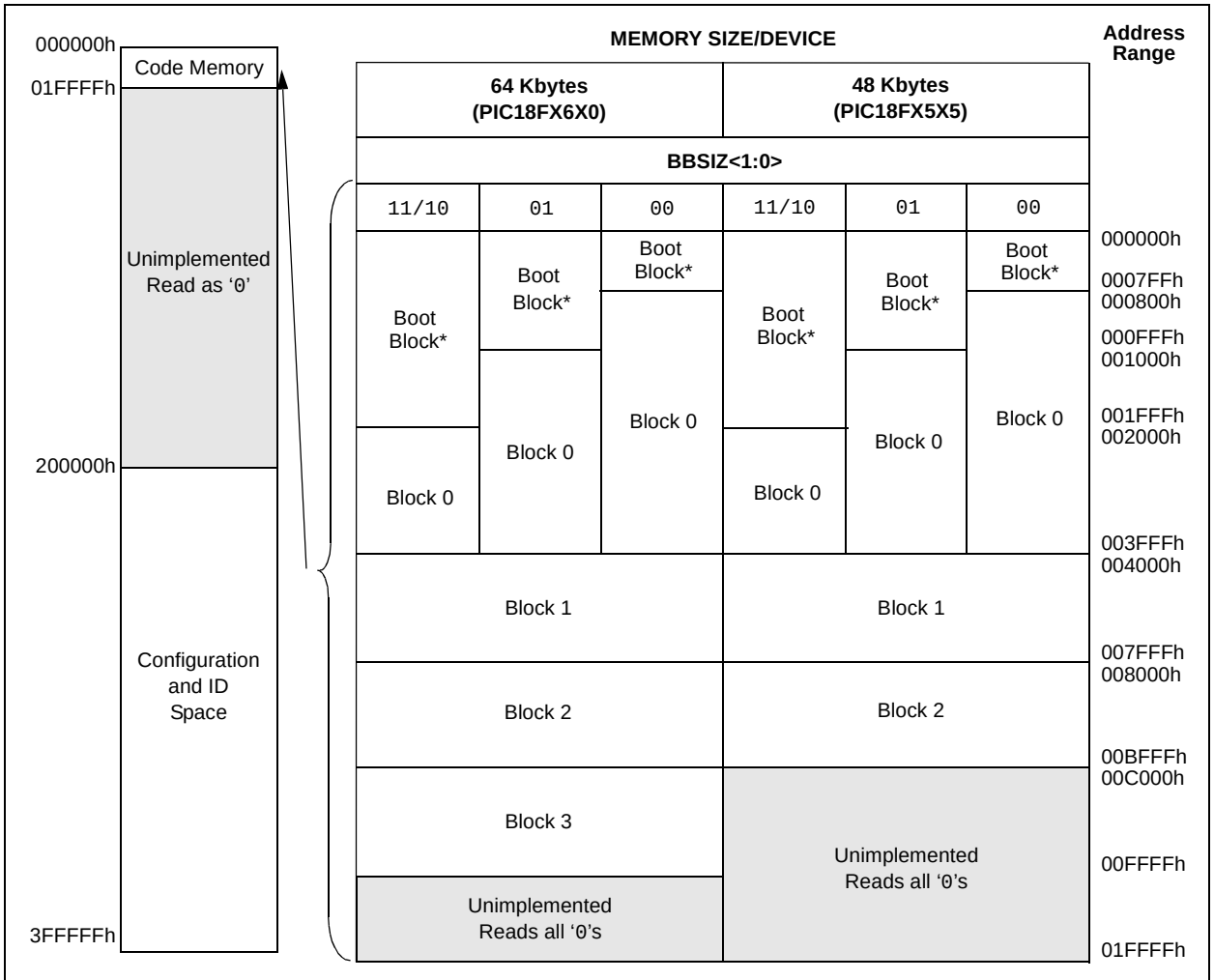



**Note 1:** These pins are NC (No Connect) for all devices listed above with the exception of the PIC18F4450, PIC18F4455, PIC18F4458 and the PIC18F4553 devices (see **Section 2.8 "Dedicated ICSP/ICD Port (44-Pin TQFP Only)"** for more information on programming these pins in these devices).

**TABLE 2-2: IMPLEMENTATION OF CODE MEMORY**

| Device | Code Memory Size (Bytes) |
|---|---|
| PIC18F2515 | 000000h-00BFFFh (48K) |
| PIC18F2525 | |
| PIC18F2585 | |
| PIC18F4515 | |
| PIC18F4525 | |
| PIC18F4585 | |
| PIC18F2610 | 000000h-00FFFFh (64K) |
| PIC18F2620 | |
| PIC18F2680 | |
| PIC18F4610 | |
| PIC18F4620 | |
| PIC18F4680 | |

**FIGURE 2-6: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX5X5/X6X0 DEVICES**




**Note:** Sizes of memory areas are not to scale.

* Boot Block size is determined by the BBSIZ<1:0> bits in the CONFIG4L register.

In addition to the code memory space, there are three blocks that are accessible to the user through Table Reads and Table Writes. Their locations in the memory map are shown in Figure 2-12.

Users may store identification information (ID) in eight ID registers. These ID registers are mapped in addresses, 200000h through 200007h. The ID locations read out normally, even after code protection is applied.

Locations, 300000h through 30000Dh, are reserved for the Configuration bits. These bits select various device options and are described in **Section 5.0 "Configuration Word"**. These Configuration bits read out normally, even after code protection.

Locations, 3FFFFEh and 3FFFFFh, are reserved for the Device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.0 "Configuration Word"**. These Device ID bits read out normally, even after code protection.

### 2.3.1 MEMORY ADDRESS POINTER

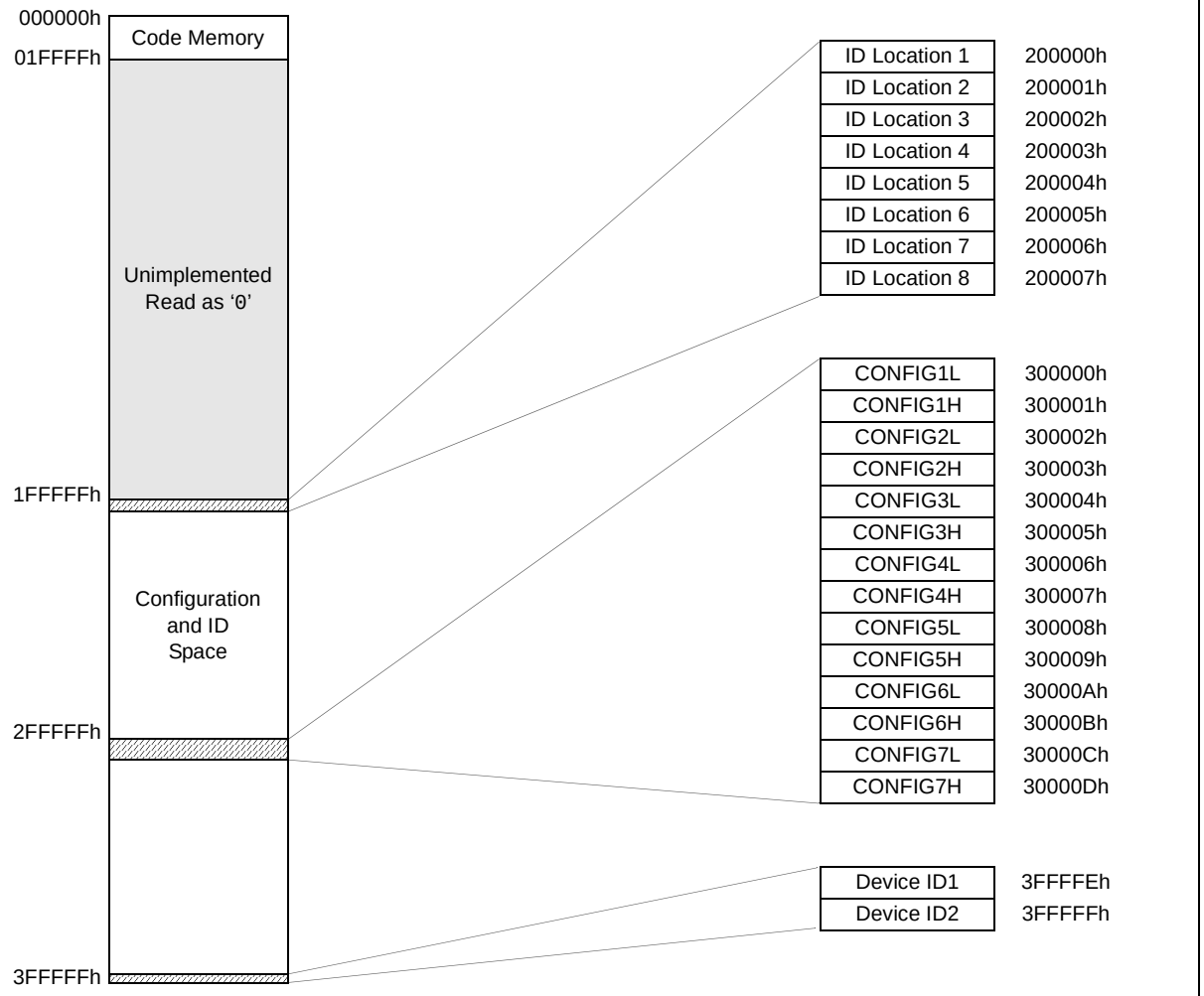
Memory in the address space, 0000000h to 3FFFFFh, is addressed via the Table Pointer register, which is comprised of three pointer registers:

- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

| TBLPTRU | TBLPTRH | TBLPTRL |
|---|---|---|
| Addr[21:16] | Addr[15:8] | Addr[7:0] |

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

**FIGURE 2-12: CONFIGURATION AND ID LOCATIONS FOR PIC18F2XXX/4XXX FAMILY DEVICES**




**Note:** Sizes of memory areas are not to scale.

## 2.6 Entering and Exiting Low-Voltage ICSP Program/Verify Mode

When the LVP Configuration bit is '1' (see **Section 5.3 "Single-Supply ICSP Programming"**), the Low-Voltage ICSP mode is enabled. As shown in Figure 2-16, Low-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low, placing a logic high on PGM and then raising MCLR/VPP/RE3 to VIH. In this mode, the RB5/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. Figure 2-17 shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

**FIGURE 2-16: ENTERING LOW-VOLTAGE PROGRAM/VERIFY MODE**

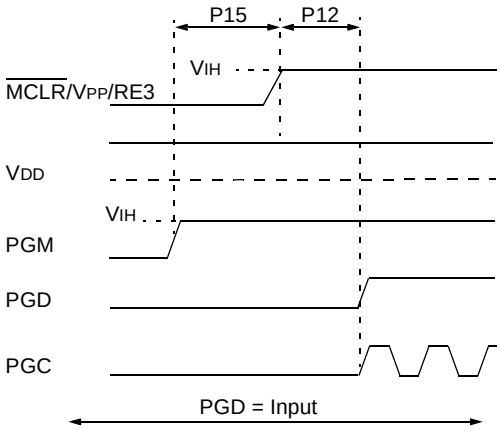
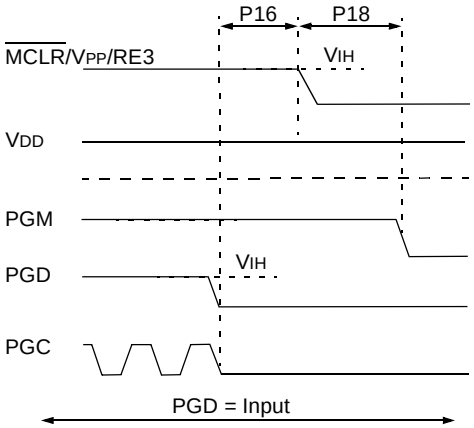



**FIGURE 2-17: EXITING LOW-VOLTAGE PROGRAM/VERIFY MODE**



### 3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device had been Bulk Erased prior to programming (see **Section 3.1.1 "High-Voltage ICSP Bulk Erase"**). It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of code memory (as described in **Section 4.2 "Verify Code Memory and ID Locations"**) and buffered. Modifications can be made on this buffer. Then, the block of code memory that was read out must be erased and rewritten with the modified data.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

**TABLE 3-6: MODIFYING CODE MEMORY**

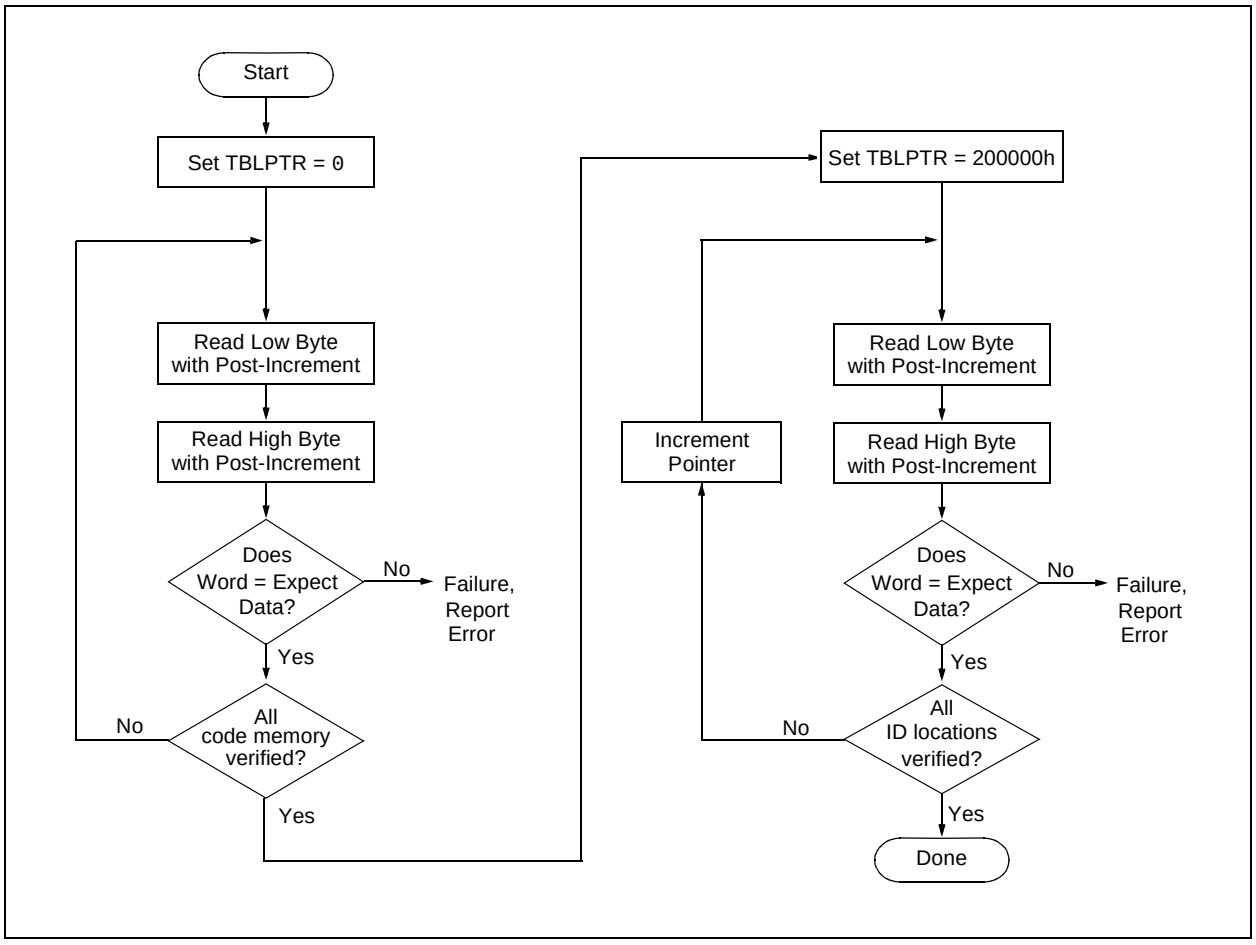
| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| Step 1: Direct access to code memory. | | |
| Step 2: Read and modify code memory (see **Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"**). | | |
| 0000<br>0000 | 8E A6<br>9C A6 | BSF EECON1, EEPGD<br>BCF EECON1, CFGS |
| Step 3: Set the Table Pointer for the block to be erased. | | |
| 0000<br>0000<br>0000<br>0000<br>0000<br>0000 | 0E <Addr[21:16]><br>6E F8<br>0E <Addr[8:15]><br>6E F7<br>0E <Addr[7:0]><br>6E F6 | MOVLW <Addr[21:16]><br>MOVWF TBLPTRU<br>MOVLW <Addr[8:15]><br>MOVWF TBLPTRH<br>MOVLW <Addr[7:0]><br>MOVWF TBLPTRL |
| Step 4: Enable memory writes and set up an erase. | | |
| 0000<br>0000 | 84 A6<br>88 A6 | BSF EECON1, WREN<br>BSF EECON1, FREE |
| Step 5: Initiate erase. | | |
| 0000<br>0000 | 82 A6<br>00 00 | BSF EECON1, WR<br>NOP - hold PGC high for time P9 and low for time P10. |
| Step 6: Load write buffer. The correct bytes will be selected based on the Table Pointer. | | |
| 0000<br>0000<br>0000<br>0000<br>0000<br>0000<br>1101<br>.<br>.<br>.<br>1111<br>0000 | 0E <Addr[21:16]><br>6E F8<br>0E <Addr[8:15]><br>6E F7<br>0E <Addr[7:0]><br>6E F6<br><MSB><LSB><br>.<br>.<br>.<br><MSB><LSB><br>00 00 | MOVLW <Addr[21:16]><br>MOVWF TBLPTRU<br>MOVLW <Addr[8:15]><br>MOVWF TBLPTRH<br>MOVLW <Addr[7:0]><br>MOVWF TBLPTRL<br>Write 2 bytes and post-increment address by 2.<br><br>Repeat as many times as necessary to fill the write buffer<br><br>Write 2 bytes and start programming.<br>NOP - hold PGC high for time P9 and low for time P10. |
| To continue modifying data, repeat Steps 2 through 6, where the Address Pointer is incremented by the appropriate number of bytes (see Table 3-4) at each iteration of the loop. The write cycle must be repeated enough times to completely rewrite the contents of the erase buffer. | | |
| Step 7: Disable writes. | | |
| 0000 | 94 A6 | BCF EECON1, WREN |

## 4.2 Verify Code Memory and ID Locations

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"** for implementation details of reading code memory.

The Table Pointer must be manually set to 200000h (base address of the ID locations) once the code memory has been verified. The post-increment feature of the Table Read 4-bit command may not be used to increment the Table Pointer beyond the code memory space. In a 64-Kbyte device, for example, a post-increment read of address, FFFFh, will wrap the Table Pointer back to 000000h, rather than point to the unimplemented address, 010000h.

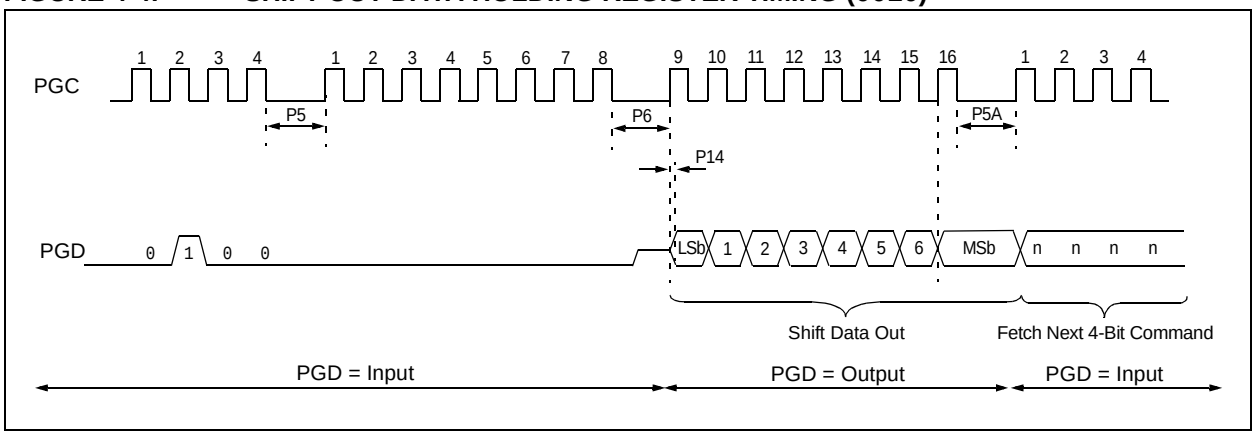
**FIGURE 4-2: VERIFY CODE MEMORY FLOW**




## 4.3 Verify Configuration Bits

A configuration address may be read and output on PGD via the 4-bit command, '1001'. Configuration data is read and written in a byte-wise fashion, so it is not necessary to merge two bytes into a word prior to a compare. The result may then be immediately compared to the appropriate configuration data in the programmer's memory for verification. Refer to **Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"** for implementation details of reading configuration data.

**FIGURE 4-4: SHIFT OUT DATA HOLDING REGISTER TIMING (0010)**




## 4.5 Verify Data EEPROM

A data EEPROM address may be read via a sequence of core instructions (4-bit command, '0000') and then output on PGD via the 4-bit command, '0010' (TABLAT register). The result may then be immediately compared to the appropriate data in the programmer's memory for verification. Refer to **Section 4.4 "Read Data EEPROM Memory"** for implementation details of reading data EEPROM.

## 4.6 Blank Check

The term Blank Check means to verify that the device has no programmed memory cells. All memories must be verified: code memory, data EEPROM, ID locations and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as '1'. Therefore, Blank Checking a device merely means to verify that all bytes read as FFh, except the Configuration bits. Unused (reserved) Configuration bits will read '0' (programmed). Refer to Figure 4-5 for blank configuration expect data for the various PIC18F2XXX/4XXX Family devices.

Given that Blank Checking is merely code and data EEPROM verification with FFh expect data, refer to **Section 4.4 "Read Data EEPROM Memory"** and **Section 4.2 "Verify Code Memory and ID Locations"** for implementation details.

**FIGURE 4-5: BLANK CHECK FLOW**

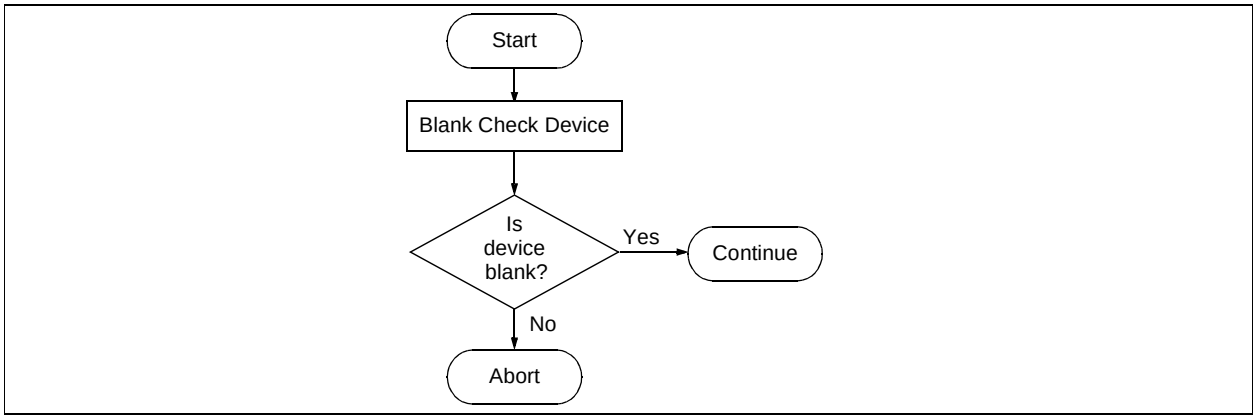


**TABLE 5-2: DEVICE ID VALUES**

| Device | Device ID Value | |
|---|---|---|
| | DEVID2 | DEVID1 |
| PIC18F2221 | 21h | 011x xxxx |
| PIC18F2321 | 21h | 001x xxxx |
| PIC18F2410 | 11h | 011x xxxx |
| PIC18F2420 | 11h | 010x xxxx(1) |
| PIC18F2423 | 11h | 010x xxxx(2) |
| PIC18F2450 | 24h | 001x xxxx |
| PIC18F2455 | 12h | 011x xxxx |
| PIC18F2458 | 2Ah | 011x xxxx |
| PIC18F2480 | 1Ah | 111x xxxx |
| PIC18F2510 | 11h | 001x xxxx |
| PIC18F2515 | 0Ch | 111x xxxx |
| PIC18F2520 | 11h | 000x xxxx(1) |
| PIC18F2523 | 11h | 000x xxxx(2) |
| PIC18F2525 | 0Ch | 110x xxxx |
| PIC18F2550 | 12h | 010x xxxx |
| PIC18F2553 | 2Ah | 010x xxxx |
| PIC18F2580 | 1Ah | 110x xxxx |
| PIC18F2585 | 0Eh | 111x xxxx |
| PIC18F2610 | 0Ch | 101x xxxx |
| PIC18F2620 | 0Ch | 100x xxxx |
| PIC18F2680 | 0Eh | 110x xxxx |
| PIC18F2682 | 27h | 000x xxxx |
| PIC18F2685 | 27h | 001x xxxx |
| PIC18F4221 | 21h | 010x xxxx |
| PIC18F4321 | 21h | 000x xxxx |
| PIC18F4410 | 10h | 111x xxxx |
| PIC18F4420 | 10h | 110x xxxx(1) |
| PIC18F4423 | 10h | 110x xxxx(2) |
| PIC18F4450 | 24h | 000x xxxx |
| PIC18F4455 | 12h | 001x xxxx |
| PIC18F4458 | 2Ah | 001x xxxx |
| PIC18F4480 | 1Ah | 101x xxxx |
| PIC18F4510 | 10h | 101x xxxx |
| PIC18F4515 | 0Ch | 011x xxxx |
| PIC18F4520 | 10h | 100x xxxx(1) |
| PIC18F4523 | 10h | 100x xxxx(2) |
| PIC18F4525 | 0Ch | 010x xxxx |
| PIC18F4550 | 12h | 000x xxxx |
| PIC18F4553 | 2Ah | 000x xxxx |
| PIC18F4580 | 1Ah | 100x xxxx |

**Legend:** The ‘x’s in DEVID1 contain the device revision code.

**Note 1:** DEVID1 bit 4 is used to determine the device type (REV4 = 0).

**2:** DEVID1 bit 4 is used to determine the device type (REV4 = 1).

**TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| PLLDIV<2:0> | CONFIG1L | Oscillator Selection bits<br>**(PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only)**<br>Divider must be selected to provide a 4 MHz input into the 96 MHz PLL:<br>111 = Oscillator divided by 12 (48 MHz input)<br>110 = Oscillator divided by 10 (40 MHz input)<br>101 = Oscillator divided by 6 (24 MHz input)<br>100 = Oscillator divided by 5 (20 MHz input)<br>011 = Oscillator divided by 4 (16 MHz input)<br>010 = Oscillator divided by 3 (12 MHz input)<br>001 = Oscillator divided by 2 (8 MHz input)<br>000 = No divide – oscillator used directly (4 MHz input) |
| VREGEN | CONFIG2L | USB Voltage Regulator Enable bit<br>**(PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only)**<br>1 = USB voltage regulator is enabled<br>0 = USB voltage regulator is disabled |
| BORV<1:0> | CONFIG2L | Brown-out Reset Voltage bits<br>11 = $V_{BOR}$ is set to 2.0V<br>10 = $V_{BOR}$ is set to 2.7V<br>01 = $V_{BOR}$ is set to 4.2V<br>00 = $V_{BOR}$ is set to 4.5V |
| BOREN<1:0> | CONFIG2L | Brown-out Reset Enable bits<br>11 = Brown-out Reset is enabled in hardware only (SBOREN is disabled)<br>10 = Brown-out Reset is enabled in hardware only and disabled in Sleep mode SBOREN is disabled)<br>01 = Brown-out Reset is enabled and controlled by software (SBOREN is enabled)<br>00 = Brown-out Reset is disabled in hardware and software |
| PWRTEN | CONFIG2L | Power-up Timer Enable bit<br>1 = PWRT is disabled<br>0 = PWRT is enabled |
| WDPS<3:0> | CONFIG2H | Watchdog Timer Postscaler Select bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>1101 = 1:8,192<br>1100 = 1:4,096<br>1011 = 1:2,048<br>1010 = 1:1,024<br>1001 = 1:512<br>1000 = 1:256<br>0111 = 1:128<br>0110 = 1:64<br>0101 = 1:32<br>0100 = 1:16<br>0011 = 1:8<br>0010 = 1:4<br>0001 = 1:2<br>0000 = 1:1 |

**Note 1:** The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

**2:** Not available in PIC18FXX8X and PIC18F2450/4450 devices.

**TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| BBSIZ<1:0>(1) | CONFIG4L | Boot Block Size Select bits **(PIC18F2321/4321 devices only)**<br>11 = 1K word (2 Kbytes) Boot Block<br>10 = 1K word (2 Kbytes) Boot Block<br>01 = 512 words (1 Kbyte) Boot Block<br>00 = 256 words (512 bytes) Boot Block<br>Boot Block Size Select bits **(PIC18F2221/4221 devices only)**<br>11 = 512 words (1 Kbyte) Boot Block<br>10 = 512 words (1 Kbyte) Boot Block<br>01 = 512 words (1 Kbyte) Boot Block<br>00 = 256 words (512 bytes) Boot Block |
| BBSIZ(1) | CONFIG4L | Boot Block Size Select bits<br>**(PIC18F2480/2580/4480/4580 and PIC18F2450/4450 devices only)**<br>1 = 2K words (4 Kbytes) Boot Block<br>0 = 1K word (2 Kbytes) Boot Block |
| LVP | CONFIG4L | Low-Voltage Programming Enable bit<br>1 = Low-Voltage Programming is enabled, RB5 is the PGM pin<br>0 = Low-Voltage Programming is disabled, RB5 is an I/O pin |
| STVREN | CONFIG4L | Stack Overflow/Underflow Reset Enable bit<br>1 = Reset on stack overflow/underflow is enabled<br>0 = Reset on stack overflow/underflow is disabled |
| CP5 | CONFIG5L | Code Protection bit (Block 5 code memory area)<br>**(PIC18F2685 and PIC18F4685 devices only)**<br>1 = Block 5 is not code-protected<br>0 = Block 5 is code-protected |
| CP4 | CONFIG5L | Code Protection bit (Block 4 code memory area)<br>**(PIC18F2682/2685 and PIC18F4682/4685 devices only)**<br>1 = Block 4 is not code-protected<br>0 = Block 4 is code-protected |
| CP3 | CONFIG5L | Code Protection bit (Block 3 code memory area)<br>1 = Block 3 is not code-protected<br>0 = Block 3 is code-protected |
| CP2 | CONFIG5L | Code Protection bit (Block 2 code memory area)<br>1 = Block 2 is not code-protected<br>0 = Block 2 is code-protected |
| CP1 | CONFIG5L | Code Protection bit (Block 1 code memory area)<br>1 = Block 1 is not code-protected<br>0 = Block 1 is code-protected |
| CP0 | CONFIG5L | Code Protection bit (Block 0 code memory area)<br>1 = Block 0 is not code-protected<br>0 = Block 0 is code-protected |
| CPD | CONFIG5H | Code Protection bit (Data EEPROM)<br>1 = Data EEPROM is not code-protected<br>0 = Data EEPROM is code-protected |
| CPB | CONFIG5H | Code Protection bit (Boot Block memory area)<br>1 = Boot Block is not code-protected<br>0 = Boot Block is code-protected |

**Note 1:** The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

**2:** Not available in PIC18FXX8X and PIC18F2450/4450 devices.

**TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| EBTR0 | CONFIG7L | Table Read Protection bit (Block 0 code memory area)<br>1 = Block 0 is not protected from Table Reads executed in other blocks<br>0 = Block 0 is protected from Table Reads executed in other blocks |
| EBTRB | CONFIG7H | Table Read Protection bit (Boot Block memory area)<br>1 = Boot Block is not protected from Table Reads executed in other blocks<br>0 = Boot Block is protected from Table Reads executed in other blocks |
| DEV<10:3> | DEVID2 | Device ID bits<br>These bits are used with the DEV<2:0> bits in the DEVID1 register to identify part number. |
| DEV<2:0> | DEVID1 | Device ID bits<br>These bits are used with the DEV<10:3> bits in the DEVID2 register to identify part number. |
| REV<4:0> | DEVID1 | Revision ID bits<br>These bits are used to indicate the revision of the device. The REV4 bit is sometimes used to fully specify the device type. |

**Note 1:** The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

**2:** Not available in PIC18FXX8X and PIC18F2450/4450 devices.

## 5.3 Single-Supply ICSP Programming

The LVP bit in Configuration register, CONFIG4L, enables Single-Supply (Low-Voltage) ICSP Programming. The LVP bit defaults to a '1' (enabled) from the factory.

If Single-Supply Programming mode is not used, the LVP bit can be programmed to a '0' and RB5/PGM becomes a digital I/O pin. However, the LVP bit may only be programmed by entering the High-Voltage ICSP mode, where MCLR/VPP/RE3 is raised to VIHH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

**Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR/VPP/RE3 pin.

**2:** While in Low-Voltage ICSP mode, the RB5 pin can no longer be used as a general purpose I/O.

## 5.4 Embedding Configuration Word Information in the HEX File

To allow portability of code, a PIC18F2XXX/4XXX Family programmer is required to read the Configuration Word locations from the hex file. If Configuration Word information is not present in the hex file, then a simple warning message should be issued. Similarly, while saving a hex file, all Configuration Word information must be included. An option to not include the Configuration Word information may be provided. When embedding Configuration Word information in the hex file, it should start at address, 300000h.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

## 5.5 Embedding Data EEPROM Information In the HEX File

To allow portability of code, a PIC18F2XXX/4XXX Family programmer is required to read the data EEPROM information from the hex file. If data EEPROM information is not present, a simple warning message should be issued. Similarly, when saving a hex file, all data EEPROM information must be included. An option to not include the data EEPROM information may be provided. When embedding data EEPROM information in the hex file, it should start at address, F00000h.

Microchip Technology Inc. believes that this feature is important for the benefit of the end customer.

## 5.6 Checksum Computation

The checksum is calculated by summing the following:

- The contents of all code memory locations
- The Configuration Words, appropriately masked
- ID locations (if any block is code-protected)

The Least Significant 16 bits of this sum is the checksum. The contents of the data EEPROM are not used.

### 5.6.1 PROGRAM MEMORY

When program memory contents are summed, each 16-bit word is added to the checksum. The contents of program memory, from 000000h to the end of the last program memory block, are used for this calculation. Overflows from bit 15 may be ignored.

### 5.6.2 CONFIGURATION WORDS

For checksum calculations, unimplemented bits in Configuration Words should be ignored as such bits always read back as '1's. Each 8-bit Configuration Word is ANDed with a corresponding mask to prevent unused bits from affecting checksum calculations.

The mask contains a '0' in unimplemented bit positions, or a '1' where a choice can be made. When ANDed with the value read out of a Configuration Word, only implemented bits remain. A list of suitable masks is provided in Table 5-5.

**TABLE 5-4: DEVICE BLOCK LOCATIONS AND SIZES (CONTINUED)**

| Device | Memory Size (Bytes) | Pins | Ending Address | | | | | | | Size (Bytes) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Boot Block | Block 0 | Block 1 | Block 2 | Block 3 | Block 4 | Block 5 | Boot Block | Block 0 | Remaining Blocks | Device Total |
| PIC18F4455 | 24K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | — | — | — | 2048 | 6144 | 16384 | 24576 |
| PIC18F4458 | 24K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | — | — | — | 2048 | 6144 | 16384 | 24576 |
| PIC18F4480 | 16K | 40 | 0007FF | 001FFF | 003FFF | — | — | — | — | 2048 | 6144 | 8192 | 16384 |
| | | | 000FFF | | | | | | | 4096 | 4096 | | |
| PIC18F4510 | 32K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | 007FFF | — | — | 2048 | 6144 | 24576 | 32768 |
| PIC18F4515 | 48K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | — | — | — | 2048 | 14336 | 32768 | 49152 |
| PIC18F4520 | 32K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | 007FFF | — | — | 2048 | 14336 | 16384 | 32768 |
| PIC18F4523 | 32K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | 007FFF | — | — | 2048 | 14336 | 16384 | 32768 |
| PIC18F4525 | 48K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | — | — | — | 2048 | 14336 | 32768 | 49152 |
| PIC18F4550 | 32K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | 007FFF | — | — | 2048 | 6144 | 24576 | 32768 |
| PIC18F4553 | 32K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | 007FFF | — | — | 2048 | 6144 | 24576 | 32768 |
| PIC18F4580 | 32K | 40 | 0007FF | 001FFF | 003FFF | 005FFF | 007FFF | — | — | 2048 | 6144 | 24576 | 32768 |
| | | | 000FFF | | | | | | | 4096 | 4096 | | |
| PIC18F4585 | 48K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | — | — | — | 2048 | 14336 | 32768 | 49152 |
| | | | 000FFF | | | | | | | 4096 | 12288 | | |
| | | | 001FFF | | | | | | | 8192 | 8192 | | |
| PIC18F4610 | 64K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | 00FFFF | — | — | 2048 | 14336 | 49152 | 65536 |
| PIC18F4620 | 64K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | 00FFFF | — | — | 2048 | 14336 | 49152 | 65536 |
| PIC18F4680 | 64K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | 00FFFF | — | — | 2048 | 14336 | 49152 | 65536 |
| | | | 000FFF | | | | | | | 4096 | 12288 | | |
| | | | 001FFF | | | | | | | 8192 | 8192 | | |
| PIC18F4682 | 80K | 40 | 0007FF | 003FFF | 007FFF | 00BFFF | 00FFFF | 013FFF | — | 2048 | 14336 | 65536 | 81920 |
| | | | 000FFF | | | | | | | 4096 | 12288 | | |
| | | | 001FFF | | | | | | | 8192 | 8192 | | |
| PIC18F4685 | 96K | 44 | 0007FF | 003FFF | 007FFF | 00BFFF | 00FFFF | 013FFF | 017FFF | 2048 | 14336 | 81920 | 98304 |
| | | | 000FFF | | | | | | | 4096 | 12288 | | |
| | | | 001FFF | | | | | | | 8192 | 8192 | | |

**Legend:** — = unimplemented.

**TABLE 5-5: CONFIGURATION WORD MASKS FOR COMPUTING CHECKSUMS (CONTINUED)**

| Device | Configuration Word (CONFIGxx) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1L | 1H | 2L | 2H | 3L | 3H | 4L | 4H | 5L | 5H | 6L | 6H | 7L | 7H |
| | Address (30000xh) | | | | | | | | | | | | | |
| | 0h | 1h | 2h | 3h | 4h | 5h | 6h | 7h | 8h | 9h | Ah | Bh | Ch | Dh |
| PIC18F4620 | 00 | CF | 1F | 1F | 00 | 87 | C5 | 00 | 0F | C0 | 0F | E0 | 0F | 40 |
| PIC18F4680 | 00 | CF | 1F | 1F | 00 | 86 | C5 | 00 | 0F | C0 | 0F | E0 | 0F | 40 |
| PIC18F4682 | 00 | CF | 1F | 1F | 00 | 86 | C5 | 00 | 3F | C0 | 3F | E0 | 3F | 40 |
| PIC18F4685 | 00 | CF | 1F | 1F | 00 | 86 | C5 | 00 | 3F | C0 | 3F | E0 | 3F | 40 |

**Legend:** Shaded cells are unimplemented.

## 6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

**Standard Operating Conditions**
Operating Temperature: 25°C is recommended

| Param No. | Sym | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| D110 | VIHH | High-Voltage Programming Voltage on MCLR/VPP/RE3 | VDD + 4.0 | 12.5 | V | **(Note 2)** |
| D110A | VIHL | Low-Voltage Programming Voltage on MCLR/VPP/RE3 | 2.00 | 5.50 | V | **(Note 2)** |
| D111 | VDD | Supply Voltage During Programming | 2.00 | 5.50 | V | Externally timed, Row Erases and all writes |
| | | | 3.0 | 5.50 | V | Self-timed, Bulk Erases only **(Note 3)** |
| D112 | IPP | Programming Current on MCLR/VPP/RE3 | — | 300 | μA | **(Note 2)** |
| D113 | IDDP | Supply Current During Programming | — | 10 | mA | |
| D031 | VIL | Input Low Voltage | VSS | 0.2 VDD | V | |
| D041 | VIH | Input High Voltage | 0.8 VDD | VDD | V | |
| D080 | VOL | Output Low Voltage | — | 0.6 | V | IOL = 8.5 mA @ 4.5V |
| D090 | VOH | Output High Voltage | VDD – 0.7 | — | V | IOH = -3.0 mA @ 4.5V |
| D012 | CIO | Capacitive Loading on I/O pin (PGD) | — | 50 | pF | To meet AC specifications |
| | | | | | | |
| P1 | TR | MCLR/VPP/RE3 Rise Time to Enter Program/Verify mode | — | 1.0 | μs | **(Notes 1, 2)** |
| P2 | TPGC | Serial Clock (PGC) Period | 100 | — | ns | VDD = 5.0V |
| | | | 1 | — | μs | VDD = 2.0V |
| P2A | TPGCL | Serial Clock (PGC) Low Time | 40 | — | ns | VDD = 5.0V |
| | | | 400 | — | ns | VDD = 2.0V |
| P2B | TPGCH | Serial Clock (PGC) High Time | 40 | — | ns | VDD = 5.0V |
| | | | 400 | — | ns | VDD = 2.0V |
| P3 | TSET1 | Input Data Setup Time to Serial Clock ↓ | 15 | — | ns | |
| P4 | THLD1 | Input Data Hold Time from PGC ↓ | 15 | — | ns | |
| P5 | TDLY1 | Delay Between 4-Bit Command and Command Operand | 40 | — | ns | |
| P5A | TDLY1A | Delay Between 4-Bit Command Operand and Next 4-Bit Command | 40 | — | ns | |
| P6 | TDLY2 | Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word | 20 | — | ns | |
| P9 | TDLY5 | PGC High Time (minimum programming time) | 1 | — | ms | Externally timed |
| P10 | TDLY6 | PGC Low Time After Programming (high-voltage discharge time) | 100 | — | μs | |
| P11 | TDLY7 | Delay to Allow Self-Timed Data Write or Bulk Erase to Occur | 5 | — | ms | |

**Note 1:** Do not allow excess time when transitioning MCLR between VIL and VIHH. This can cause spurious program executions to occur. The maximum transition time is:
1 TCY + TPWRT (if enabled) + 1024 TOSC (for LP, HS, HS/PLL and XT modes only) +
2 ms (for HS/PLL mode only) + 1.5 μs (for EC mode only)
where TCY is the instruction cycle time, TPWRT is the Power-up Timer period and TOSC is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.

**2:** When ICPRT = 1, this specification also applies to ICVPP.

**3:** At 0°C-50°C.

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



**Trademarks**



ISBN: 978-1-63277-856-7

**QUALITY MANAGEMENT SYSTEM**
**CERTIFIED BY DNV**
**═ ISO/TS 16949 ═**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

# Worldwide Sales and Service

## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

**Austin, TX**
Tel: 512-257-3370

**Boston**
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

**Chicago**
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

**Cleveland**
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

**Dallas**
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

**Detroit**
Novi, MI
Tel: 248-848-4000

**Houston, TX**
Tel: 281-894-5983

**Indianapolis**
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

**Los Angeles**
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

**New York, NY**
Tel: 631-435-6000

**San Jose, CA**
Tel: 408-735-9110

**Canada - Toronto**
Tel: 905-673-0699
Fax: 905-673-6509

## ASIA/PACIFIC

**Asia Pacific Office**
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

**Hong Kong**
Tel: 852-2943-5100
Fax: 852-2401-3431

**Australia - Sydney**
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

**China - Beijing**
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

**China - Chengdu**
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

**China - Chongqing**
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

**China - Dongguan**
Tel: 86-769-8702-9880

**China - Hangzhou**
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

**China - Hong Kong SAR**
Tel: 852-2943-5100
Fax: 852-2401-3431

**China - Nanjing**
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

**China - Qingdao**
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

**China - Shanghai**
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

**China - Shenyang**
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

**China - Shenzhen**
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

**China - Wuhan**
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

**China - Xian**
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

## ASIA/PACIFIC

**China - Xiamen**
Tel: 86-592-2388138
Fax: 86-592-2388130

**China - Zhuhai**
Tel: 86-756-3210040
Fax: 86-756-3210049

**India - Bangalore**
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

**India - New Delhi**
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

**India - Pune**
Tel: 91-20-3019-1500

**Japan - Osaka**
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

**Japan - Tokyo**
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

**Korea - Daegu**
Tel: 82-53-744-4301
Fax: 82-53-744-4302

**Korea - Seoul**
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

**Malaysia - Kuala Lumpur**
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

**Malaysia - Penang**
Tel: 60-4-227-8870
Fax: 60-4-227-4068

**Philippines - Manila**
Tel: 63-2-634-9065
Fax: 63-2-634-9069

**Singapore**
Tel: 65-6334-8870
Fax: 65-6334-8850

**Taiwan - Hsin Chu**
Tel: 886-3-5778-366
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**
Tel: 886-7-213-7828

**Taiwan - Taipei**
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

**Thailand - Bangkok**
Tel: 66-2-694-1351
Fax: 66-2-694-1350

## EUROPE

**Austria - Wels**
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

**Denmark - Copenhagen**
Tel: 45-4450-2828
Fax: 45-4485-2829

**France - Paris**
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

**Germany - Dusseldorf**
Tel: 49-2129-3766400

**Germany - Karlsruhe**
Tel: 49-721-625370

**Germany - Munich**
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

**Italy - Milan**
Tel: 39-0331-742611
Fax: 39-0331-466781

**Italy - Venice**
Tel: 39-049-7625286

**Netherlands - Drunen**
Tel: 31-416-690399
Fax: 31-416-690340

**Poland - Warsaw**
Tel: 48-22-3325737

**Spain - Madrid**
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

**Sweden - Stockholm**
Tel: 46-8-5090-4654

**UK - Wokingham**
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15