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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

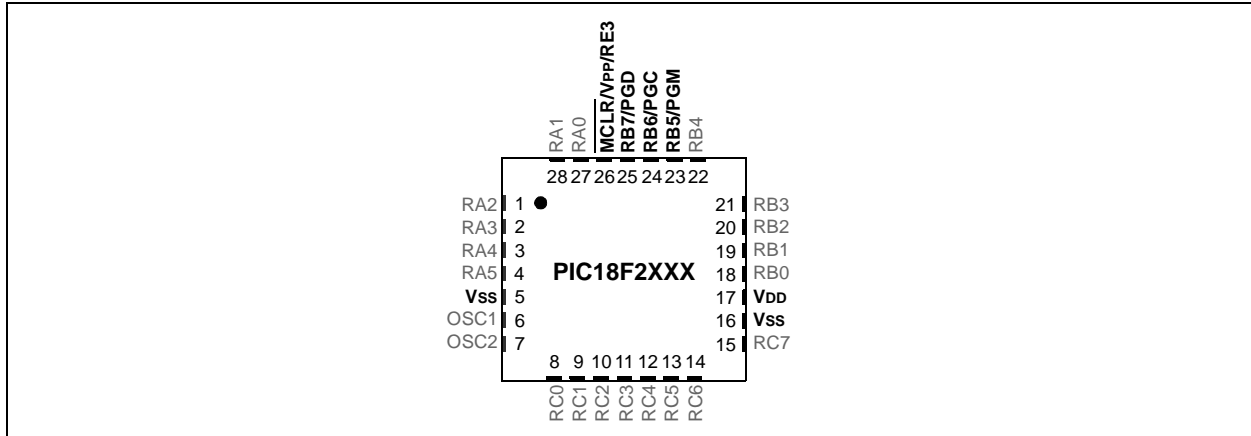
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2515-i-sp

PIC18F2XXX/4XXX FAMILY

The following devices are included in 28-pin QFN parts:

- | | | | |
|--------------|--------------|--------------|--------------|
| • PIC18F2221 | • PIC18F2423 | • PIC18F2510 | • PIC18F2580 |
| • PIC18F2321 | • PIC18F2450 | • PIC18F2520 | • PIC18F2682 |
| • PIC18F2410 | • PIC18F2480 | • PIC18F2523 | • PIC18F2685 |
| • PIC18F2420 | • | • | • |

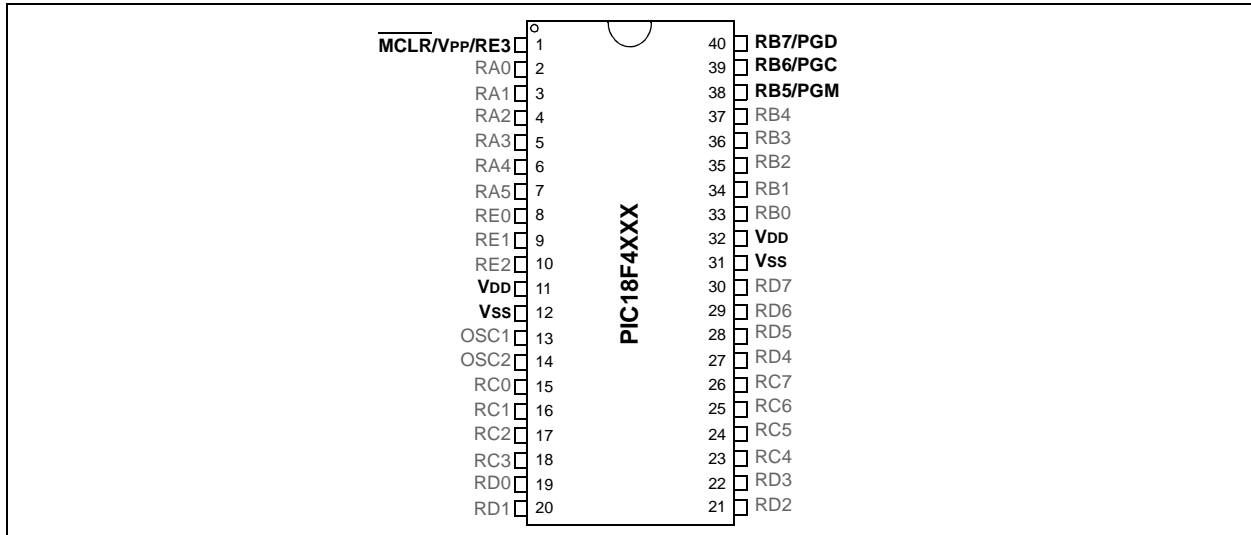
FIGURE 2-2: 28-Pin QFN



The following devices are included in 40-pin PDIP parts:

- | | | | |
|--------------|--------------|--------------|--------------|
| • PIC18F4221 | • PIC18F4455 | • PIC18F4523 | • PIC18F4610 |
| • PIC18F4321 | • PIC18F4458 | • PIC18F4525 | • PIC18F4620 |
| • PIC18F4410 | • PIC18F4480 | • PIC18F4550 | • PIC18F4680 |
| • PIC18F4420 | • PIC18F4510 | • PIC18F4553 | • PIC18F4682 |
| • PIC18F4423 | • PIC18F4515 | • PIC18F4580 | • PIC18F4685 |
| • PIC18F4450 | • PIC18F4520 | • PIC18F4585 | • |

FIGURE 2-3: 40-Pin PDIP

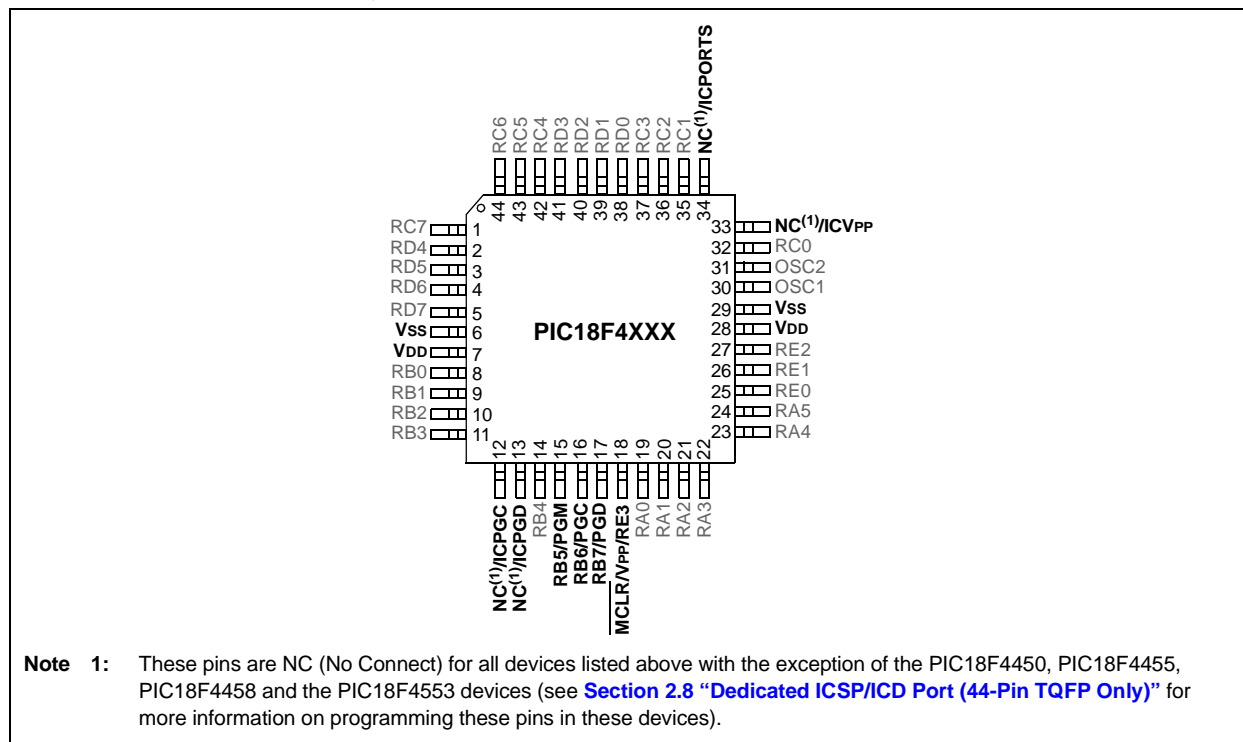


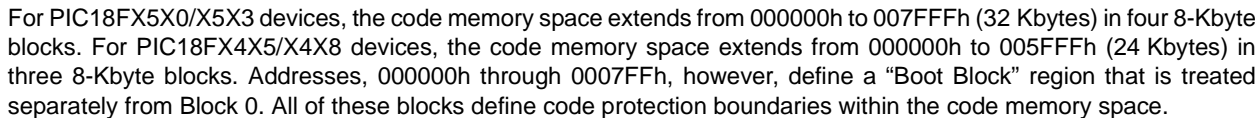
PIC18F2XXX/4XXX FAMILY

The following devices are included in 44-pin TQFP parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4520
- PIC18F4515
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

FIGURE 2-4: 44-PIN TQFP





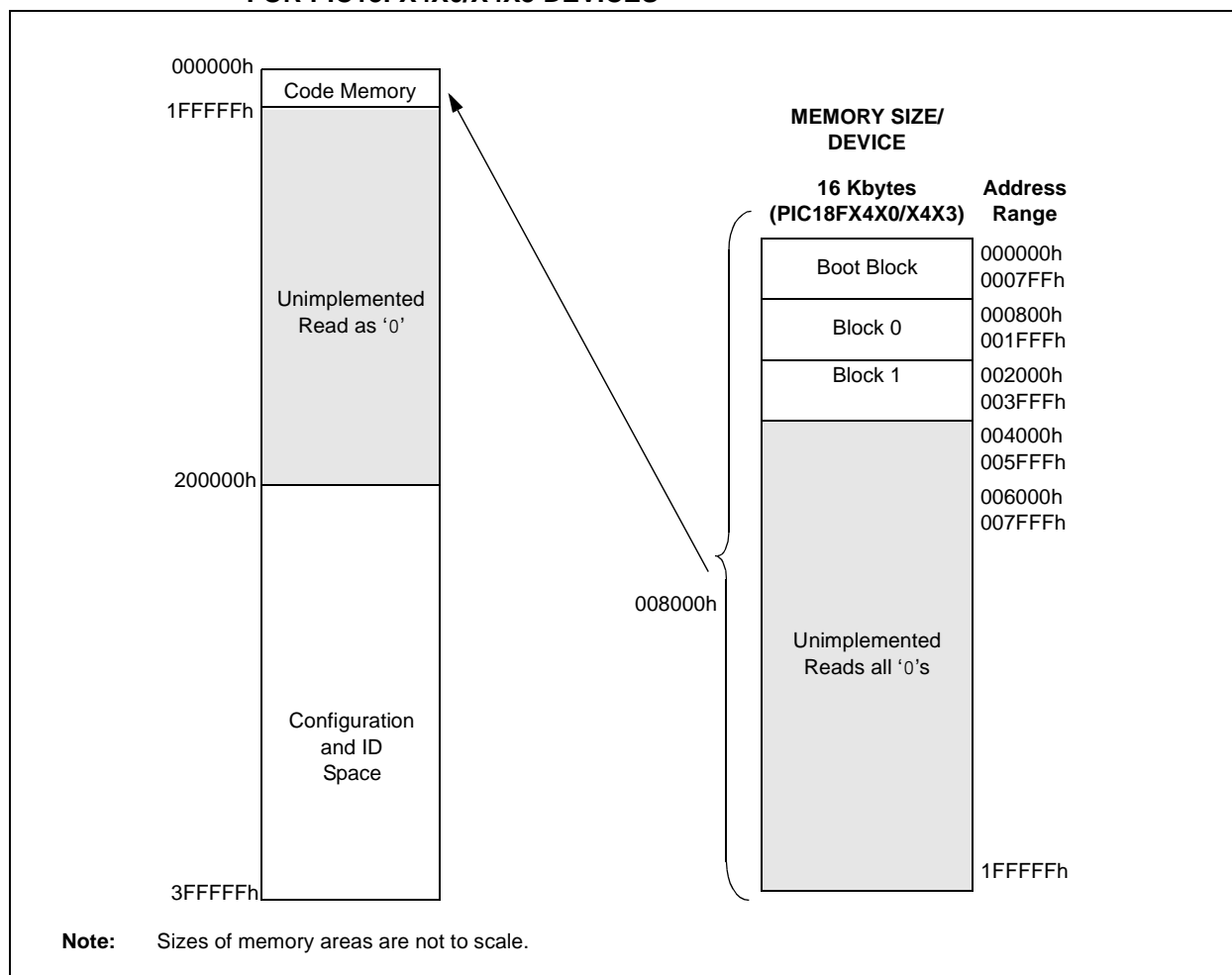
DS30009622M-page 8

PIC18F2XXX/4XXX FAMILY

TABLE 2-5: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2410	000000h-003FFFh (16K)
PIC18F2420	
PIC18F2423	
PIC18F2450	
PIC18F4410	
PIC18F4420	
PIC18F4450	

FIGURE 2-9: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX4X0/X4X3 DEVICES



For PIC18F2480/4480 devices, the code memory space extends from 0000h to 03FFFh (16 Kbytes) in one 16-Kbyte block. For PIC18F2580/4580 devices, the code memory space extends from 0000h to 07FFFh (32 Kbytes) in two 16-Kbyte blocks. Addresses, 0000h through 07FFFh, however, define a "Boot Block" region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

The size of the Boot Block in PIC18F2480/2580/4480/4580 devices can be configured as 1 or 2K words (see [Figure 2-10](#)). This is done through the BBSIZ<0> bit in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

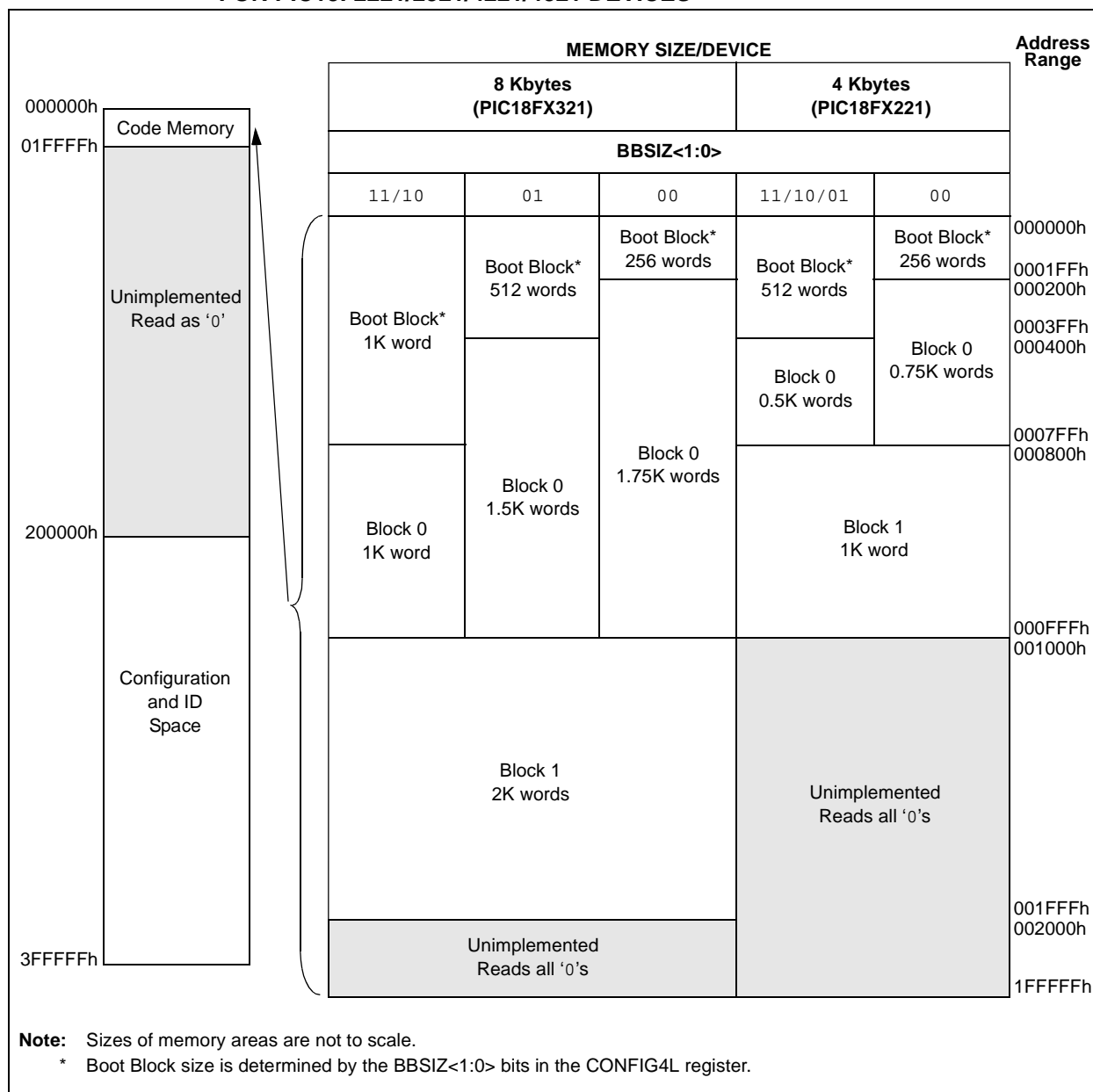
PIC18F2XXX/4XXX FAMILY

The size of the Boot Block in PIC18F2221/2321/4221/4321 devices can be configured as 256, 512 or 1024 words (see [Figure 2-11](#)). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L (see [Figure 2-11](#)). It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

TABLE 2-7: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2221	000000h-000FFFh (4K)
PIC18F4221	
PIC18F2321	000000h-001FFFh (8K)
PIC18F4321	

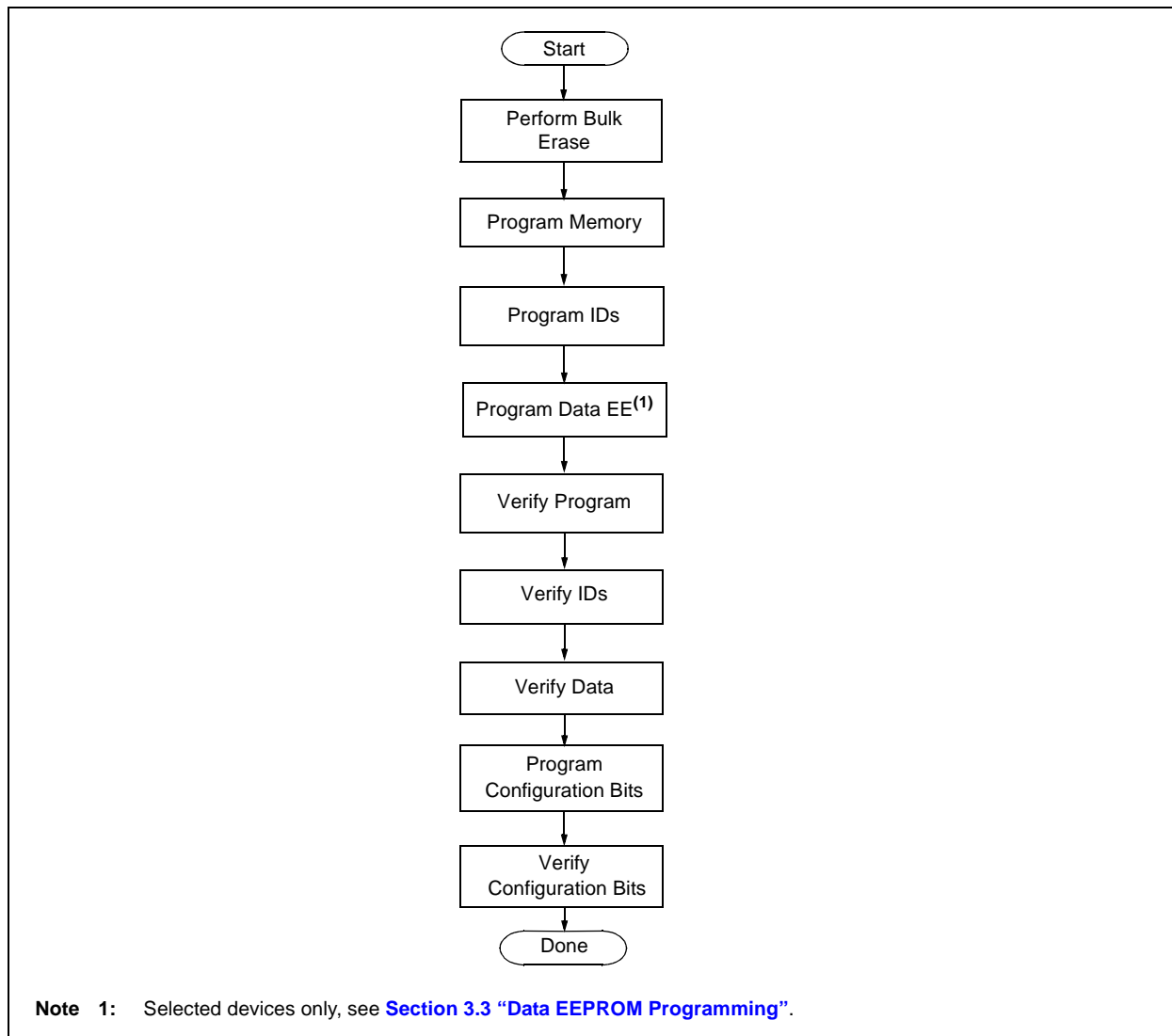
FIGURE 2-11: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2221/2321/4221/4321 DEVICES



2.4 High-Level Overview of the Programming Process

Figure 2-13 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory, ID locations and data EEPROM are programmed (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)). These memories are then verified to ensure that programming was successful. If no errors are detected, the Configuration bits are then programmed and verified.

FIGURE 2-13: HIGH-LEVEL PROGRAMMING FLOW



2.6 Entering and Exiting Low-Voltage ICSP Program/Verify Mode

When the LVP Configuration bit is '1' (see [Section 5.3 “Single-Supply ICSP Programming”](#)), the Low-Voltage ICSP mode is enabled. As shown in [Figure 2-16](#), Low-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low, placing a logic high on PGM and then raising $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$ to V_{IH} . In this mode, the RB5/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. [Figure 2-17](#) shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-16: ENTERING LOW-VOLTAGE PROGRAM/VERIFY MODE

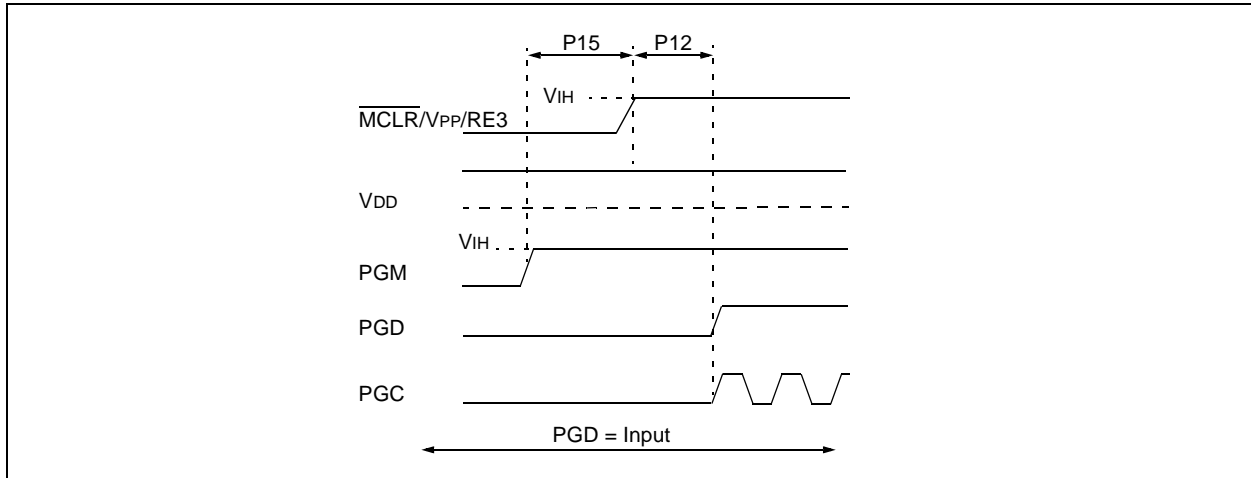
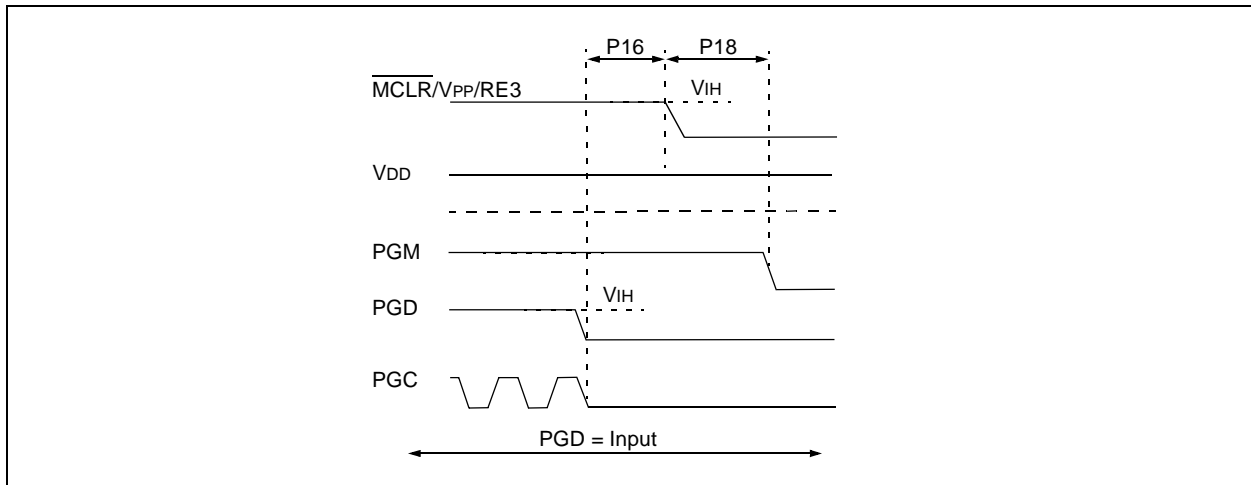


FIGURE 2-17: EXITING LOW-VOLTAGE PROGRAM/VERIFY MODE

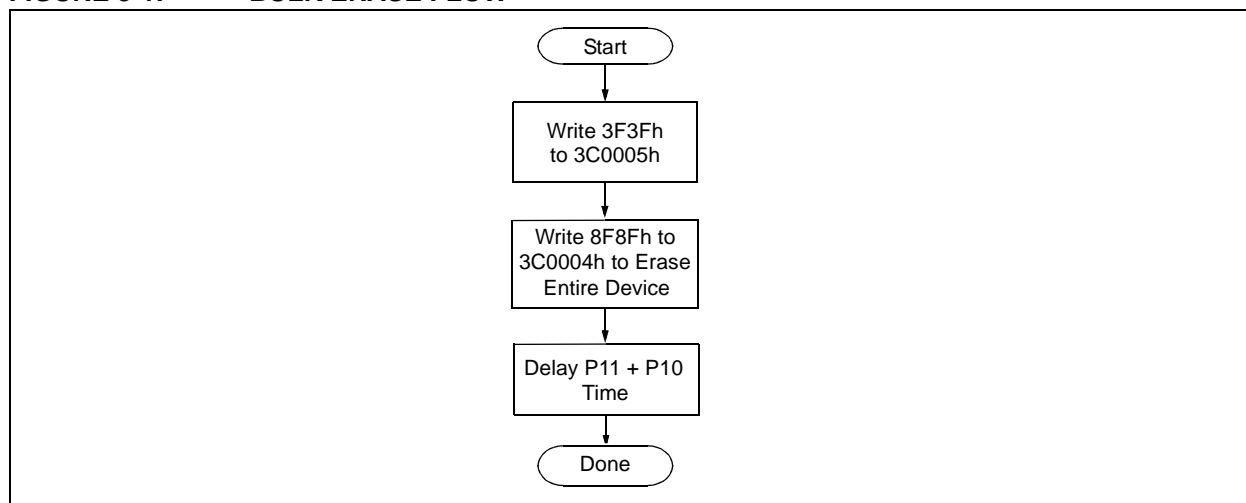


PIC18F2XXX/4XXX FAMILY

TABLE 3-2: BULK ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	3F 3F	Write 3F3Fh to 3C0005h
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	8F 8F	Write 8F8Fh TO 3C0004h to erase entire device. NOP Hold PGD low until erase completes.
0000	00 00	
0000	00 00	

FIGURE 3-1: BULK ERASE FLOW



PIC18F2XXX/4XXX FAMILY

3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device had been Bulk Erased prior to programming (see [Section 3.1.1 “High-Voltage ICSP Bulk Erase”](#)). It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of code memory (as described in [Section 4.2 “Verify Code Memory and ID Locations”](#)) and buffered. Modifications can be made on this buffer. Then, the block of code memory that was read out must be erased and rewritten with the modified data.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

TABLE 3-6: MODIFYING CODE MEMORY

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory.		
Step 2: Read and modify code memory (see Section 4.1 “Read Code Memory, ID Locations and Configuration Bits”).		
0000 0000	8E A6 9C A6	BSF EECON1, EEPGD BCF EECON1, CFGS
Step 3: Set the Table Pointer for the block to be erased.		
0000 0000 0000 0000 0000 0000	0E <Addr[21:16]> 6E F8 0E <Addr[8:15]> 6E F7 0E <Addr[7:0]> 6E F6	MOVLW <Addr[21:16]> MOVWF TBLPTRU MOVLW <Addr[8:15]> MOVWF TBLPTRH MOVLW <Addr[7:0]> MOVWF TBLPTRL
Step 4: Enable memory writes and set up an erase.		
0000 0000	84 A6 88 A6	BSF EECON1, WREN BSF EECON1, FREE
Step 5: Initiate erase.		
0000 0000	82 A6 00 00	BSF EECON1, WR NOP - hold PGC high for time P9 and low for time P10.
Step 6: Load write buffer. The correct bytes will be selected based on the Table Pointer.		
0000 0000 0000 0000 0000 0000 1101 . . . 1111 0000	0E <Addr[21:16]> 6E F8 0E <Addr[8:15]> 6E F7 0E <Addr[7:0]> 6E F6 <MSB><LSB> . . . <MSB><LSB> 00 00	MOVLW <Addr[21:16]> MOVWF TBLPTRU MOVLW <Addr[8:15]> MOVWF TBLPTRH MOVLW <Addr[7:0]> MOVWF TBLPTRL Write 2 bytes and post-increment address by 2. Repeat as many times as necessary to fill the write buffer Write 2 bytes and start programming. NOP - hold PGC high for time P9 and low for time P10.
To continue modifying data, repeat Steps 2 through 6, where the Address Pointer is incremented by the appropriate number of bytes (see Table 3-4) at each iteration of the loop. The write cycle must be repeated enough times to completely rewrite the contents of the erase buffer.		
Step 7: Disable writes.		
0000	94 A6	BCF EECON1, WREN

PIC18F2XXX/4XXX FAMILY

3.3 Data EEPROM Programming

Note: Data EEPROM programming is not available on the following devices:	
PIC18F2410	PIC18F4410
PIC18F2450	PIC18F4450
PIC18F2510	PIC18F4510
PIC18F2515	PIC18F4515
PIC18F2610	PIC18F4610

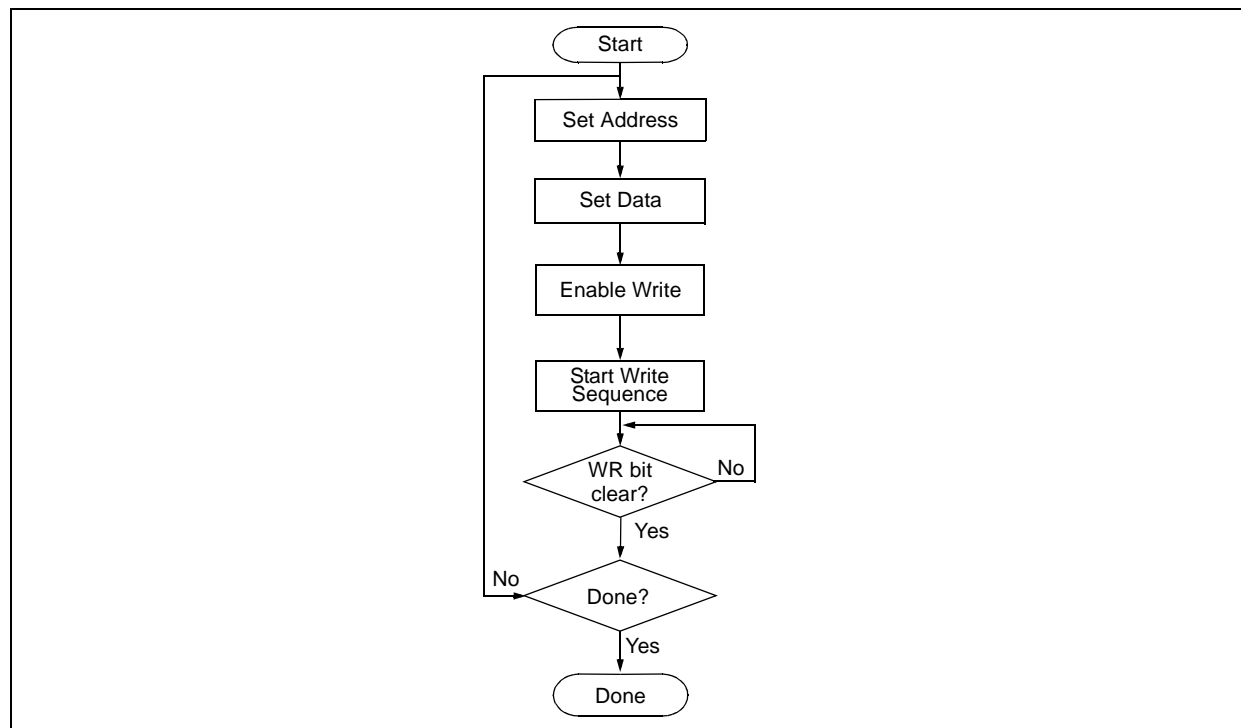
Data EEPROM is accessed one byte at a time via an Address Pointer (register pair: EEADRH:EEADR) and a data latch (EEDATA). Data EEPROM is written by loading EEADRH:EEADR with the desired memory location, EEDATA, with the data to be written and initiating a memory write by appropriately configuring the EECON1 register. A byte write automatically erases the location and writes the new data (erase-before-write).

When using the EECON1 register to perform a data EEPROM write, both the EEPGD and CFGS bits must be cleared (EECON1<7:6> = 00). The WREN bit must be set (EECON1<2> = 1) to enable writes of any sort and this must be done prior to initiating a write sequence. The write sequence is initiated by setting the WR bit (EECON1<1> = 1).

The write begins on the falling edge of the 4th PGC after the WR bit is set. It ends when the WR bit is cleared by hardware.

After the programming sequence terminates, PGC must still be held low for the time specified by Parameter P10 to allow high-voltage discharge of the memory array.

FIGURE 3-6: PROGRAM DATA FLOW



PIC18F2XXX/4XXX FAMILY

TABLE 3-7: PROGRAMMING DATA MEMORY

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to data EEPROM.		
0000	9E A6	BCF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Set the data EEPROM Address Pointer.		
0000	0E <Addr>	MOVLW <Addr>
0000	6E A9	MOVWF EEADR
0000	0E <AddrH>	MOVLW <AddrH>
0000	6E AA	MOVWF EEADRH
Step 3: Load the data to be written.		
0000	0E <Data>	MOVLW <Data>
0000	6E A8	MOVWF EEDATA
Step 4: Enable memory writes.		
0000	84 A6	BSF EECON1, WREN
Step 5: Initiate write.		
0000	82 A6	BSF EECON1, WR
Step 6: Poll WR bit, repeat until the bit is clear.		
0000	50 A6	MOVF EECON1, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0010	<MSB><LSB>	Shift out data ⁽¹⁾
Step 7: Hold PGC low for time P10.		
Step 8: Disable writes.		
0000	94 A6	BCF EECON1, WREN
Repeat Steps 2 through 8 to write more data.		

Note 1: See [Figure 4-4](#) for details on shift out data timing.

PIC18F2XXX/4XXX FAMILY

4.0 READING THE DEVICE

4.1 Read Code Memory, ID Locations and Configuration Bits

Code memory is accessed, one byte at a time, via the 4-bit command, '1001' (Table Read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

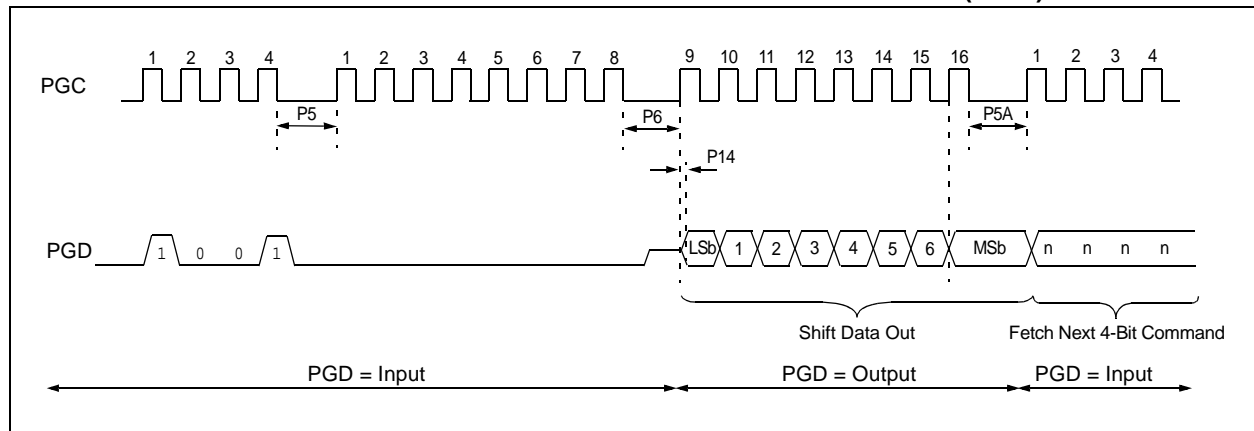
The 4-bit command is shifted in, LSb first. The read is executed during the next eight clocks, then shifted out on PGD during the last eight clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see [Figure 4-1](#)). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFFh address space, so it also applies to the reading of the ID and Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

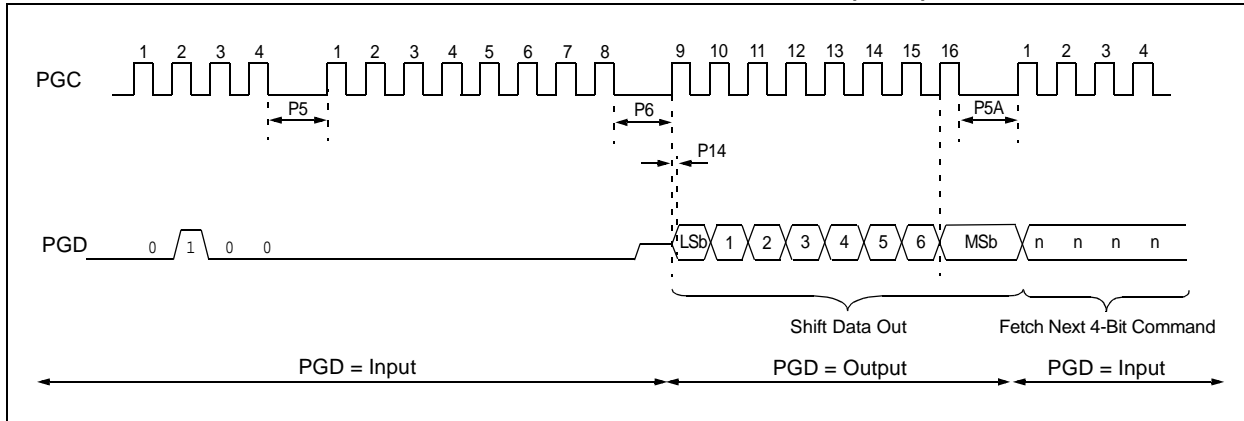
4-Bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

FIGURE 4-1: TABLE READ POST-INCREMENT INSTRUCTION TIMING (1001)



PIC18F2XXX/4XXX FAMILY

FIGURE 4-4: SHIFT OUT DATA HOLDING REGISTER TIMING (0010)



4.5 Verify Data EEPROM

A data EEPROM address may be read via a sequence of core instructions (4-bit command, '0000') and then output on PGD via the 4-bit command, '0010' (TABLAT register). The result may then be immediately compared to the appropriate data in the programmer's memory for verification. Refer to [Section 4.4 "Read Data EEPROM Memory"](#) for implementation details of reading data EEPROM.

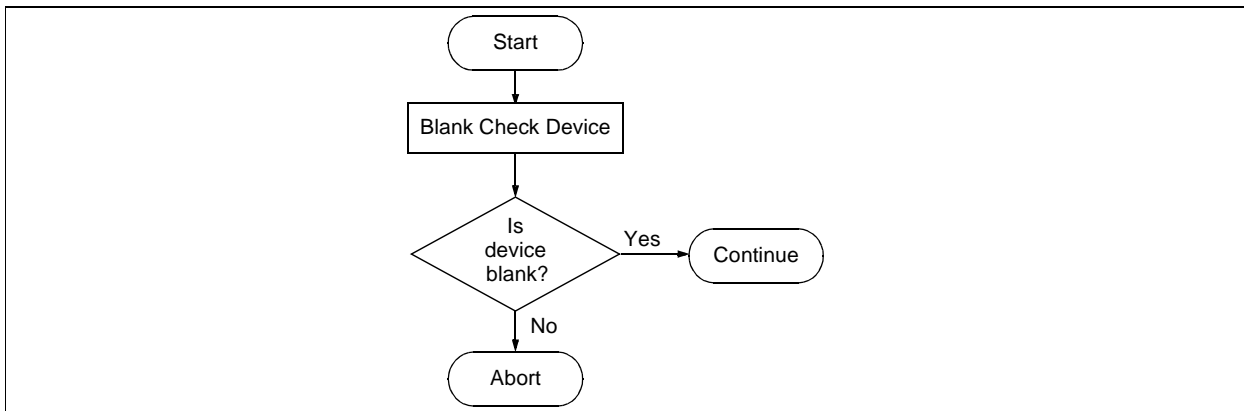
4.6 Blank Check

The term Blank Check means to verify that the device has no programmed memory cells. All memories must be verified: code memory, data EEPROM, ID locations and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as '1'. Therefore, Blank Checking a device merely means to verify that all bytes read as FFh, except the Configuration bits. Unused (reserved) Configuration bits will read '0' (programmed). Refer to [Figure 4-5](#) for blank configuration expect data for the various PIC18F2XXX/4XXX Family devices.

Given that Blank Checking is merely code and data EEPROM verification with FFh expect data, refer to [Section 4.4 "Read Data EEPROM Memory"](#) and [Section 4.2 "Verify Code Memory and ID Locations"](#) for implementation details.

FIGURE 4-5: BLANK CHECK FLOW



5.0 CONFIGURATION WORD

The PIC18F2XXX/4XXX Family devices have several Configuration Words. These bits can be set or cleared to select various device configurations. All other memory areas should be programmed and verified prior to setting the Configuration Words. These bits may be read out normally, even after read or code protection. See [Table 5-1](#) for a list of Configuration bits and Device IDs, and [Table 5-3](#) for the Configuration bit descriptions.

5.1 ID Locations

A user may store identification information (ID) in eight ID locations, mapped in 200000h:200007h. It is recommended that the Most Significant nibble of each ID be Fh. In doing so, if the user code inadvertently tries to execute from the ID space, the ID data will execute as a NOP.

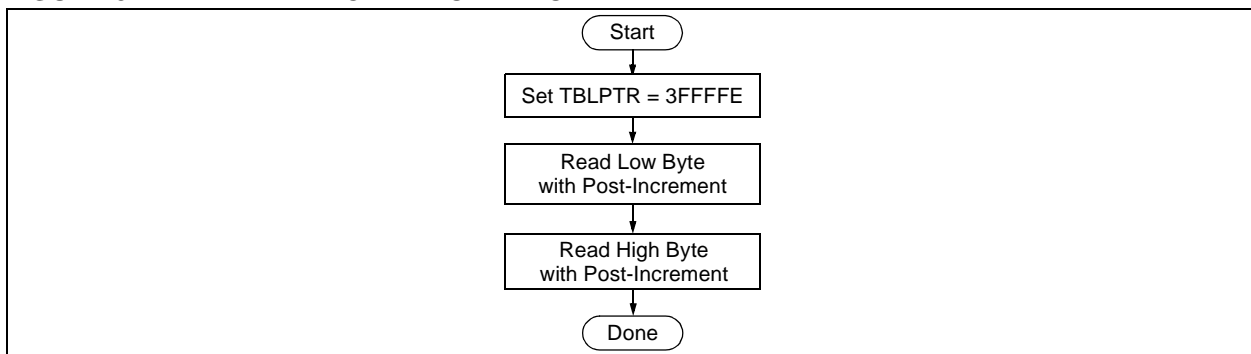
5.2 Device ID Word

The Device ID Word for the PIC18F2XXX/4XXX Family devices is located at 3FFFFEh:3FFFFFh. These bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code or read protection.

In some cases, devices may share the same DEVID values. In such cases, the Most Significant bit of the device revision, REV4 (DEVID1<4>), will need to be examined to completely determine the device being accessed.

See [Table 5-2](#) for a complete list of Device ID values.

FIGURE 5-1: READ DEVICE ID WORD FLOW



PIC18F2XXX/4XXX FAMILY

TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
IESO	CONFIG1H	Internal External Switchover bit 1 = Internal External Switchover mode is enabled 0 = Internal External Switchover mode is disabled
FCMEN	CONFIG1H	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor is enabled 0 = Fail-Safe Clock Monitor is disabled
FOSC<3:0>	CONFIG1H	Oscillator Selection bits 11xx = External RC oscillator, CLKO function on RA6 101x = External RC oscillator, CLKO function on RA6 1001 = Internal RC oscillator, CLKO function on RA6, port function on RA7 1000 = Internal RC oscillator, port function on RA6, port function on RA7 0111 = External RC oscillator, port function on RA6 0110 = HS oscillator, PLL is enabled (Clock Frequency = 4 x FOSC1) 0101 = EC oscillator, port function on RA6 0100 = EC oscillator, CLKO function on RA6 0011 = External RC oscillator, CLKO function on RA6 0010 = HS oscillator 0001 = XT oscillator 0000 = LP oscillator
FOSC<3:0>	CONFIG1H	Oscillator Selection bits (PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only) 111x = HS oscillator, PLL is enabled, HS is used by USB 110x = HS oscillator, HS is used by USB 1011 = Internal oscillator, HS is used by USB 1010 = Internal oscillator, XT is used by USB 1001 = Internal oscillator, CLKO function on RA6, EC is used by USB 1000 = Internal oscillator, port function on RA6, EC is used by USB 0111 = EC oscillator, PLL is enabled, CLKO function on RA6, EC is used by USB 0110 = EC oscillator, PLL is enabled, port function on RA6, EC is used by USB 0101 = EC oscillator, CLKO function on RA6, EC is used by USB 0100 = EC oscillator, port function on RA6, EC is used by USB 001x = XT oscillator, PLL is enabled, XT is used by USB 000x = XT oscillator, XT is used by USB
USBDIV	CONFIG1L	USB Clock Selection bit (PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only) Selects the clock source for full-speed USB operation: 1 = USB clock source comes from the 96 MHz PLL divided by 2 0 = USB clock source comes directly from the OSC1/OSC2 oscillator block; no divide
CPUDIV<1:0>	CONFIG1L	CPU System Clock Selection bits (PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only) 11 = CPU system clock divided by 4 10 = CPU system clock divided by 3 01 = CPU system clock divided by 2 00 = No CPU system clock divide

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

PIC18F2XXX/4XXX FAMILY

TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
EBTR0	CONFIG7L	Table Read Protection bit (Block 0 code memory area) 1 = Block 0 is not protected from Table Reads executed in other blocks 0 = Block 0 is protected from Table Reads executed in other blocks
EBTRB	CONFIG7H	Table Read Protection bit (Boot Block memory area) 1 = Boot Block is not protected from Table Reads executed in other blocks 0 = Boot Block is protected from Table Reads executed in other blocks
DEV<10:3>	DEVID2	Device ID bits These bits are used with the DEV<2:0> bits in the DEVID1 register to identify part number.
DEV<2:0>	DEVID1	Device ID bits These bits are used with the DEV<10:3> bits in the DEVID2 register to identify part number.
REV<4:0>	DEVID1	Revision ID bits These bits are used to indicate the revision of the device. The REV4 bit is sometimes used to fully specify the device type.

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

PIC18F2XXX/4XXX FAMILY

5.6.3 ID LOCATIONS

Normally, the contents of these locations are defined by the user, but MPLAB® IDE provides the option of writing the device's unprotected 16-bit checksum in the 16 Most Significant bits of the ID locations (see MPLAB IDE Configure/ID Memory" menu). The lower 16 bits are not used and remain clear. This is the sum of all program memory contents and Configuration Words (appropriately masked) before any code protection is enabled.

If the user elects to define the contents of the ID locations, nothing about protected blocks can be known. If the user uses the preprotected checksum, provided by MPLAB IDE, an indirect characteristic of the programmed code is provided.

5.6.4 CODE PROTECTION

Blocks that are code-protected read back as all '0's and have no effect on checksum calculations. If any block is code-protected, then the contents of the ID locations are included in the checksum calculation.

All Configuration Words and the ID locations can always be read out normally, even when the device is fully code-protected. Checking the code protection settings in Configuration Words can direct which, if any, of the program memory blocks can be read, and if the ID locations should be used for checksum calculations.

PIC18F2XXX/4XXX FAMILY

TABLE 5-4: DEVICE BLOCK LOCATIONS AND SIZES

Device	Memory Size (Bytes)	Pins	Ending Address							Size (Bytes)			
			Boot Block	Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Boot Block	Block 0	Remaining Blocks	Device Total
PIC18F2221	4K	28	0001FF	0007FF	000FFF	—	—	—	—	512	1536	2048	4096
			0003FF							1024	1024		
PIC18F2321	8K	28	0001FF	000FFF	001FFF	—	—	—	—	512	3584	4096	8192
			0003FF							1024	3072		
			0007FF							2048	2048		
PIC18F2410	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F2420	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F2423	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F2450	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		
PIC18F2455	24K	28	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F2458	24K	28	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F2480	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		
PIC18F2510	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F2515	48K	28	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F2520	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F2523	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F2525	48K	28	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F2550	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F2553	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F2580	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
			000FFF							4096	4096		
PIC18F2585	48K	28	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F2610	64K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F2620	64K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F2680	64K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F2682	80K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	—	2048	14336	65536	81920
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F2685	96K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	017FFF	2048	14336	81920	98304
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4221	4K	40	0001FF	0007FF	000FFF	—	—	—	—	512	1536	2048	4096
			0003FF							1024	1024		
PIC18F4321	8K	40	0001FF	000FFF	001FFF	—	—	—	—	512	3584	4096	8192
			0003FF							1024	3072		
			0007FF							2048	2048		
PIC18F4410	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F4420	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F4423	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F4450	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		

Legend: — = unimplemented.

PIC18F2XXX/4XXX FAMILY

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions						
Operating Temperature: 25°C is recommended						
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
P11A	TDRWT	Data Write Polling Time	4	—	ms	
P12	THLD2	Input Data Hold Time from $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \uparrow$	2	—	μs	
P13	TSET2	$\text{VDD} \uparrow$ Setup Time to $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \uparrow$	100	—	ns	(Note 2)
P14	TVALID	Data Out Valid from PGC \uparrow	10	—	ns	
P15	TSET3	PGM \uparrow Setup Time to $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \uparrow$	2	—	μs	(Note 2)
P16	TDLY8	Delay Between Last PGC \downarrow and $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \downarrow$	0	—	s	
P17	THLD3	$\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \downarrow$ to $\text{VDD} \downarrow$	—	100	ns	
P18	THLD4	$\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \downarrow$ to PGM \downarrow	0	—	s	

- Note 1:** Do not allow excess time when transitioning $\overline{\text{MCLR}}$ between VIL and VIHH . This can cause spurious program executions to occur. The maximum transition time is:
1 $\text{T}_{\text{CY}} + \text{T}_{\text{PWRT}}$ (if enabled) + 1024 T_{OSC} (for LP, HS, HS/PLL and XT modes only) +
2 ms (for HS/PLL mode only) + 1.5 μs (for EC mode only)
where T_{CY} is the instruction cycle time, T_{PWRT} is the Power-up Timer period and T_{OSC} is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.
- 2:** When $\text{ICPRT} = 1$, this specification also applies to ICVPP .
- 3:** At 0°C-50°C.