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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

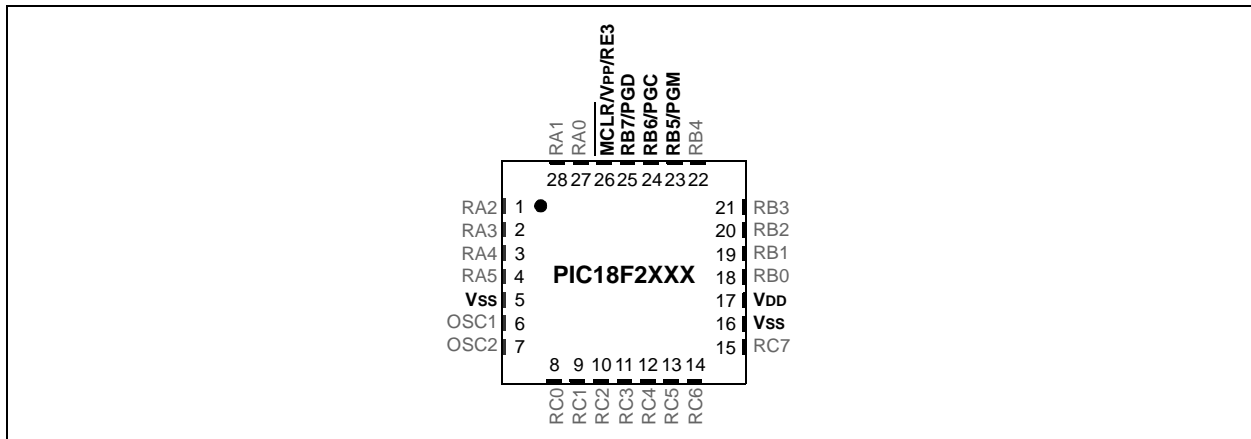
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4515t-i-ml

PIC18F2XXX/4XXX FAMILY

The following devices are included in 28-pin QFN parts:

- | | | | |
|--------------|--------------|--------------|--------------|
| • PIC18F2221 | • PIC18F2423 | • PIC18F2510 | • PIC18F2580 |
| • PIC18F2321 | • PIC18F2450 | • PIC18F2520 | • PIC18F2682 |
| • PIC18F2410 | • PIC18F2480 | • PIC18F2523 | • PIC18F2685 |
| • PIC18F2420 | • | • | • |

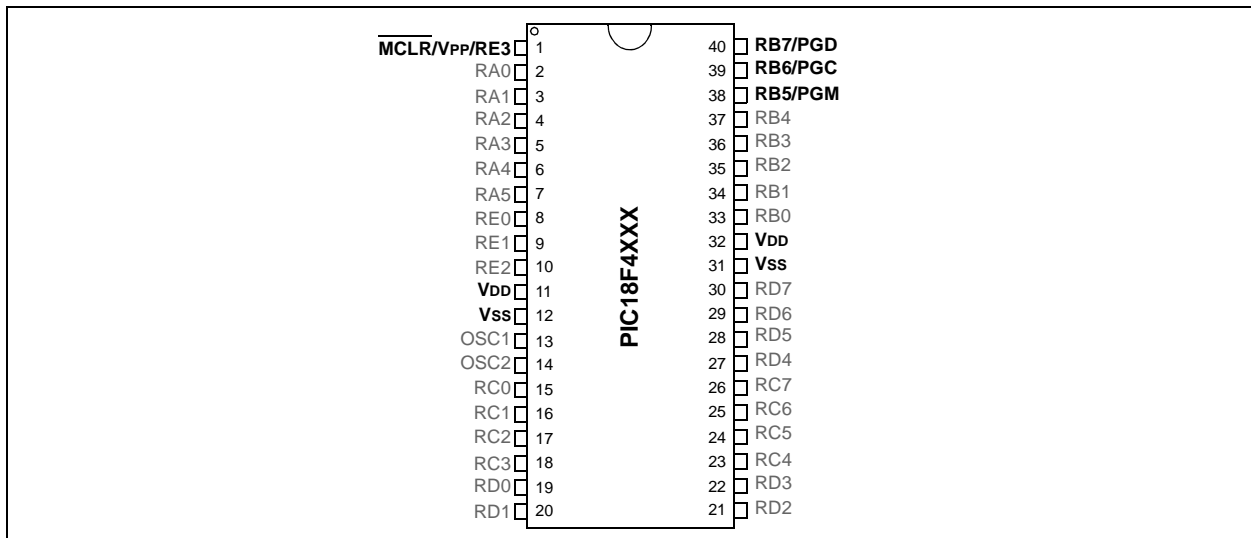
FIGURE 2-2: 28-Pin QFN



The following devices are included in 40-pin PDIP parts:

- | | | | |
|--------------|--------------|--------------|--------------|
| • PIC18F4221 | • PIC18F4455 | • PIC18F4523 | • PIC18F4610 |
| • PIC18F4321 | • PIC18F4458 | • PIC18F4525 | • PIC18F4620 |
| • PIC18F4410 | • PIC18F4480 | • PIC18F4550 | • PIC18F4680 |
| • PIC18F4420 | • PIC18F4510 | • PIC18F4553 | • PIC18F4682 |
| • PIC18F4423 | • PIC18F4515 | • PIC18F4580 | • PIC18F4685 |
| • PIC18F4450 | • PIC18F4520 | • PIC18F4585 | • |

FIGURE 2-3: 40-Pin PDIP

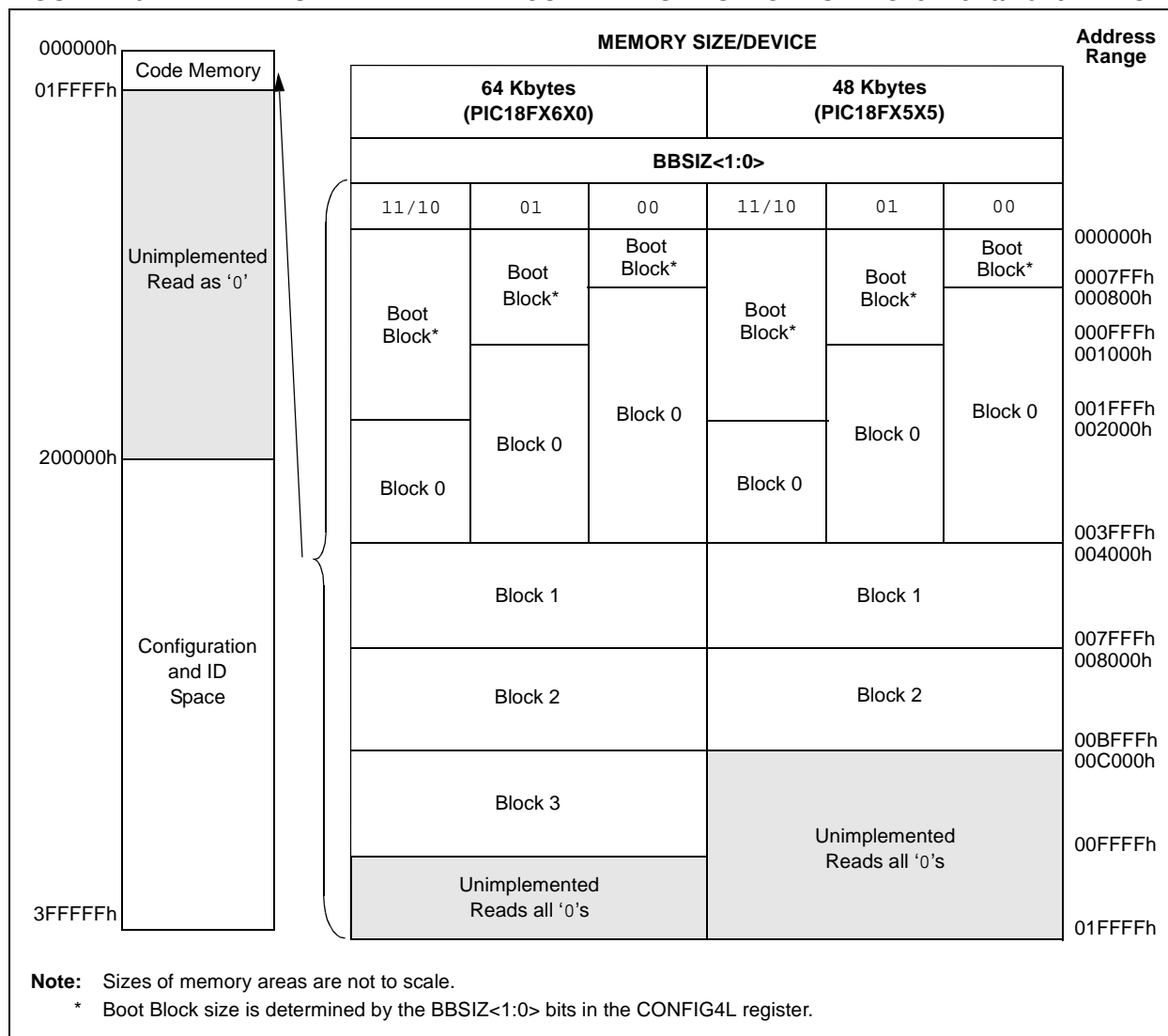


PIC18F2XXX/4XXX FAMILY

TABLE 2-2: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2515	000000h-00BFFFh (48K)
PIC18F2525	
PIC18F2585	
PIC18F4515	
PIC18F4525	
PIC18F4585	
PIC18F2610	000000h-00FFFFh (64K)
PIC18F2620	
PIC18F2680	
PIC18F4610	
PIC18F4620	
PIC18F4680	

FIGURE 2-6: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX5X5/X6X0 DEVICES

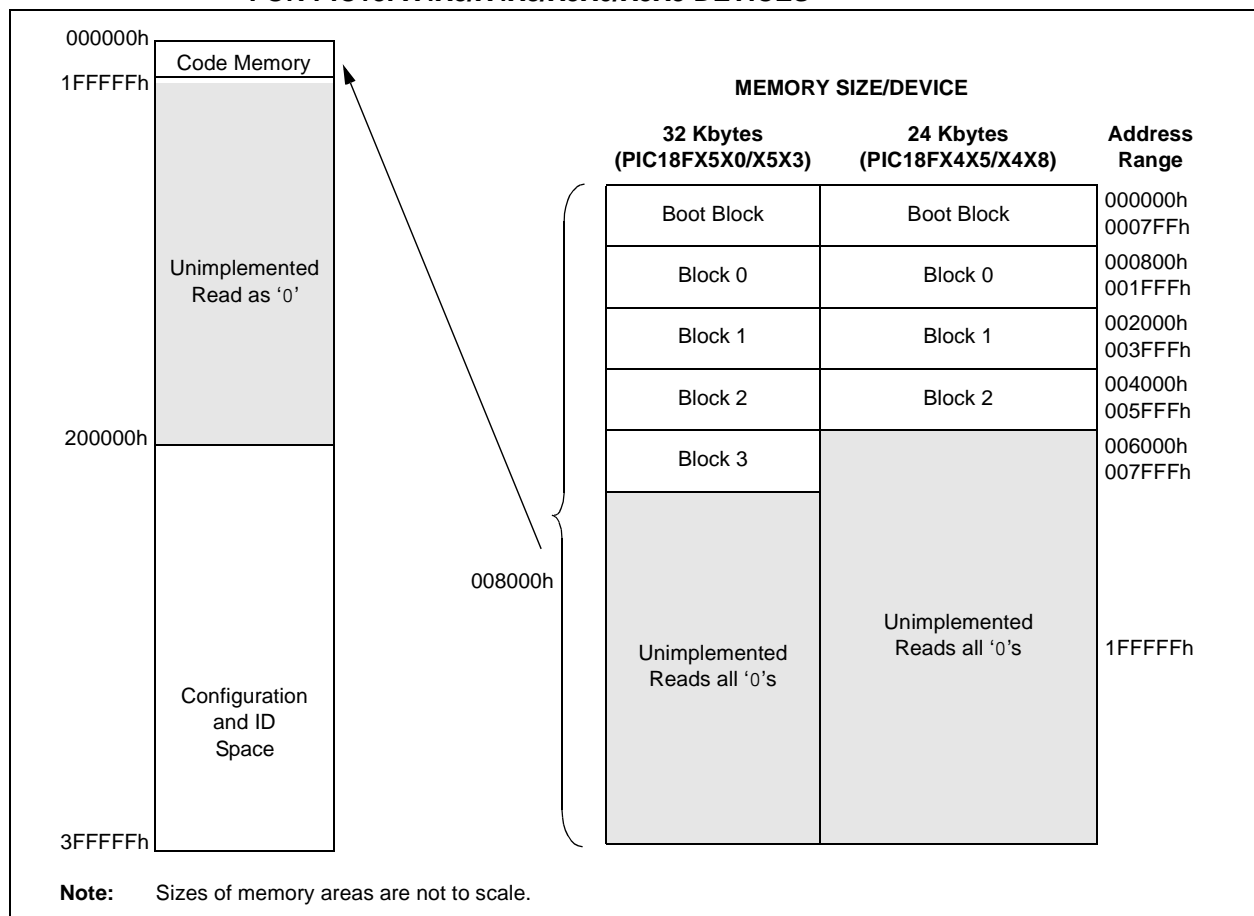


PIC18F2XXX/4XXX FAMILY

TABLE 2-4: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2455	000000h-005FFFh (24K)
PIC18F2458	
PIC18F4455	
PIC18F4458	
PIC18F2510	000000h-007FFFh (32K)
PIC18F2520	
PIC18F2523	
PIC18F2550	
PIC18F2553	
PIC18F4510	
PIC18F4520	
PIC18F4523	
PIC18F4550	
PIC18F4553	

FIGURE 2-8: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX4X5/X4X8/X5X0/X5X3 DEVICES



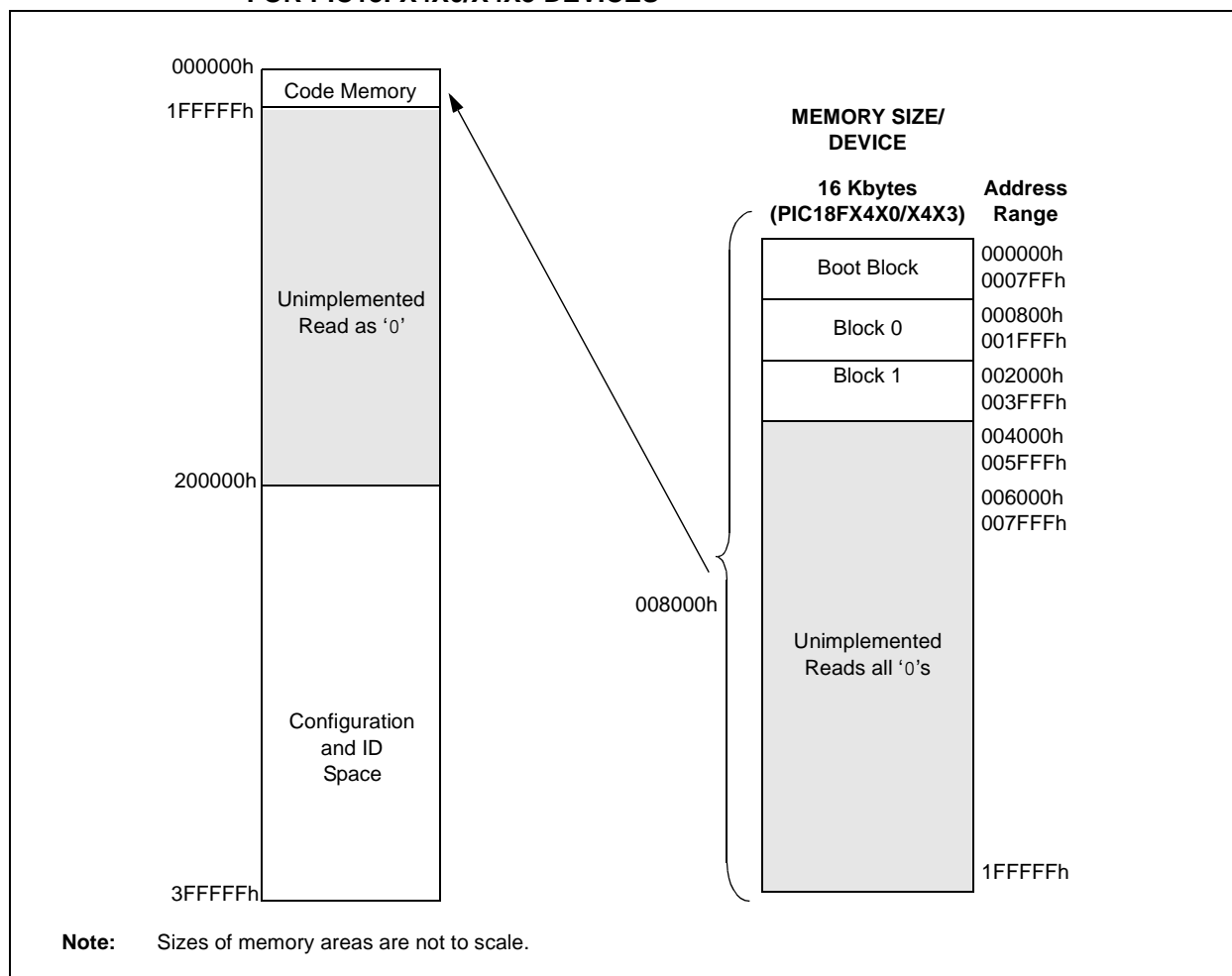
For PIC18FX4X0/X4X3 devices, the code memory space extends from 000000h to 003FFFh (16 Kbytes) in two 8-Kbyte blocks. Addresses, 000000h through 0003FFFh, however, define a "Boot Block" region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

PIC18F2XXX/4XXX FAMILY

TABLE 2-5: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2410	000000h-003FFFh (16K)
PIC18F2420	
PIC18F2423	
PIC18F2450	
PIC18F4410	
PIC18F4420	
PIC18F4450	

FIGURE 2-9: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX4X0/X4X3 DEVICES



For PIC18F2480/4480 devices, the code memory space extends from 0000h to 03FFFh (16 Kbytes) in one 16-Kbyte block. For PIC18F2580/4580 devices, the code memory space extends from 0000h to 07FFFh (32 Kbytes) in two 16-Kbyte blocks. Addresses, 0000h through 07FFFh, however, define a "Boot Block" region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

The size of the Boot Block in PIC18F2480/2580/4480/4580 devices can be configured as 1 or 2K words (see [Figure 2-10](#)). This is done through the BBSIZ<0> bit in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

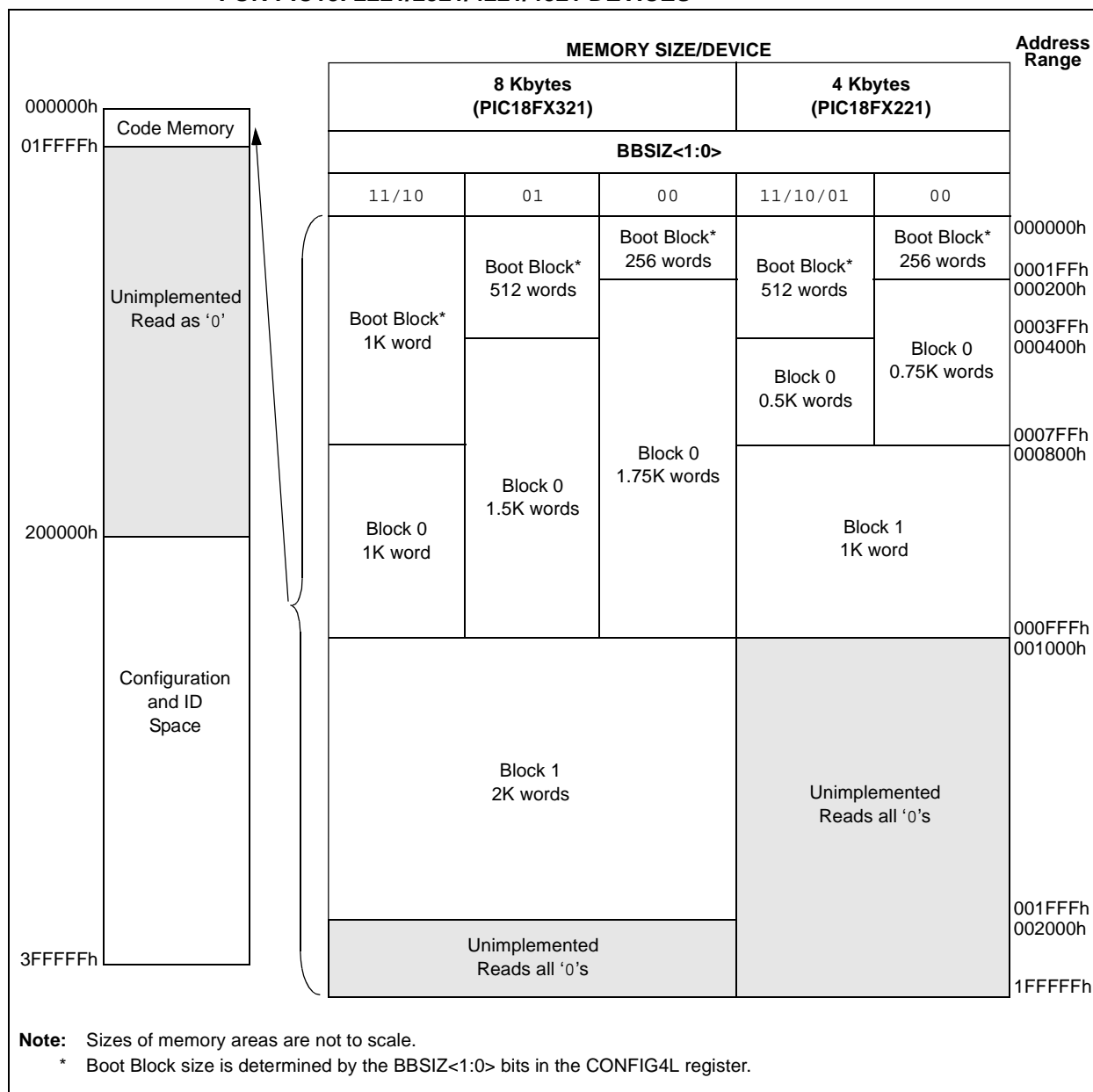
PIC18F2XXX/4XXX FAMILY

The size of the Boot Block in PIC18F2221/2321/4221/4321 devices can be configured as 256, 512 or 1024 words (see [Figure 2-11](#)). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L (see [Figure 2-11](#)). It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

TABLE 2-7: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F2221	000000h-000FFFh (4K)
PIC18F4221	
PIC18F2321	000000h-001FFFh (8K)
PIC18F4321	

FIGURE 2-11: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2221/2321/4221/4321 DEVICES



As shown in [Figure 2-14](#), the High-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low and then raising MCLR/VPP/RE3 to VIHh (high voltage). Once in this mode, the code memory, data EEPROM (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)), ID locations and Configuration bits can be accessed and programmed in serial fashion. [Figure 2-15](#) shows the exit sequence.

Timing diagram showing the relationship between D110, MCLR/VPP/RE3, VDD, PGD, and PGC. The diagram illustrates the sequence of events during a programming operation, including the rise of VDD, the assertion of MCLR/VPP/RE3 to VPP, and the subsequent PGD signal driven by PGC. The PGC signal has a period P1 and pulse widths P12 and P13. A horizontal dashed line indicates the D110 data level.

The diagram illustrates the timing sequence for the MCLR/VPP/RE3 pin during a self-programming operation. The signals shown are:

- MCLR/VPP/RE3**: The master clear/vpp/reprogram pin. It is pulled up to VDD and driven low during programming.
- D110**: The data bus. It is high during programming.
- VDD**: The supply voltage. It is high during programming and drops to a low level after the operation.
- PGD**: The program data output. It is high during programming and drops to a low level after the operation.
- PGC**: The program clock. It is a square wave signal that is high during programming and drops to a low level after the operation.

Key timing parameters are indicated by arrows:

- P16**: Program time (from the start of the programming operation to the end of the programming operation).
- P17**: Program time (from the start of the programming operation to the end of the programming operation).
- P1**: Program time (from the start of the programming operation to the end of the programming operation).

The PGD signal is labeled as **PGD = Input**.

PIC18F2XXX/4XXX FAMILY

2.7 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC and are Least Significant bit (LSb) first.

2.7.1 4-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in [Table 2-8](#).

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or 8 bits of input data and 8 bits of output data.

Throughout this specification, commands and data are presented as illustrated in [Table 2-9](#). The 4-bit command is shown Most Significant bit (MSb) first. The command operand, or "Data Payload", is shown as <MSB><LSB>. [Figure 2-18](#) demonstrates how to serially present a 20-bit command/operand to the device.

2.7.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

TABLE 2-8: COMMANDS FOR PROGRAMMING

Description	4-Bit Command
Core Instruction (Shift in 16-bit instruction)	0000
Shift Out TABLAT Register	0010
Table Read	1000
Table Read, Post-Increment	1001
Table Read, Post-Decrement	1010
Table Read, Pre-Increment	1011
Table Write	1100
Table Write, Post-Increment by 2	1101
Table Write, Start Programming, Post-Increment by 2	1110
Table Write, Start Programming	1111

TABLE 2-9: SAMPLE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
1101	3C 40	Table Write, post-increment by 2

PIC18F2XXX/4XXX FAMILY

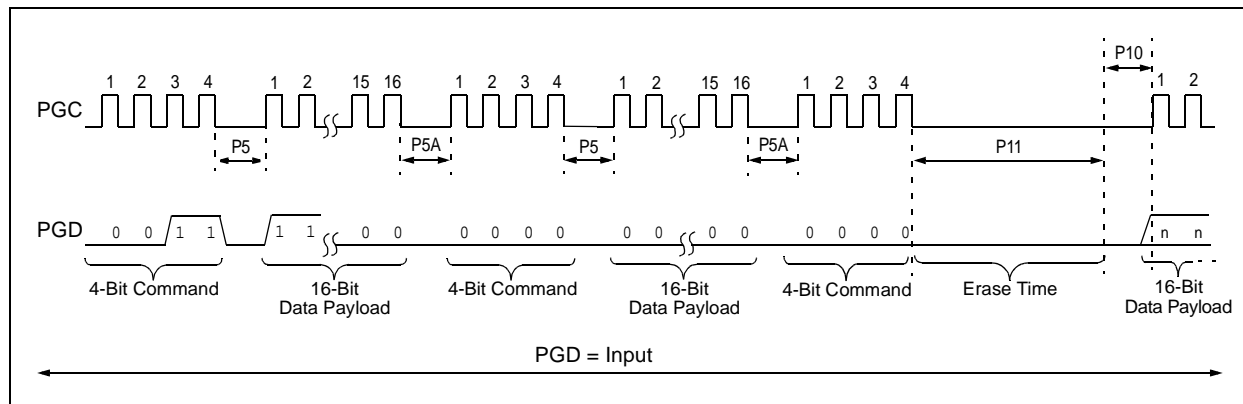
3.1.2 LOW-VOLTAGE ICSP BULK ERASE

When using low-voltage ICSP, the part must be supplied by the voltage specified in Parameter D111 if a Bulk Erase is to be executed. All other Bulk Erase details, as described above, apply.

If it is determined that a program memory erase must be performed at a supply voltage below the Bulk Erase limit, refer to the erase methodology described in [Section 3.1.3 “ICSP Row Erase”](#) and [Section 3.2.1 “Modifying Code Memory”](#).

If it is determined that a data EEPROM erase (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)) must be performed at a supply voltage below the Bulk Erase limit, follow the methodology described in [Section 3.3 “Data EEPROM Programming”](#) and write ‘1’s to the array.

FIGURE 3-2: BULK ERASE TIMING



3.1.3 ICSP ROW ERASE

Regardless of whether high or low-voltage ICSP is used, it is possible to erase one row (64 bytes of data), provided the block is not code or write-protected. Rows are located at static boundaries, beginning at program memory address, 000000h, extending to the internal program memory limit (see [Section 2.3 “Memory Maps”](#)).

The Row Erase duration is externally timed and is controlled by PGC. After the WR bit in EECON1 is set, a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by Parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to Row Erase a PIC18F2XXX/4XXX Family device is shown in [Table 3-3](#). The flowchart, shown in [Figure 3-3](#), depicts the logic necessary to completely erase a PIC18F2XXX/4XXX Family device. The timing diagram that details the Start Programming command and Parameters P9 and P10 is shown in [Figure 3-5](#).

Note: The TBLPTR register can point to any byte within the row intended for erase.

PIC18F2XXX/4XXX FAMILY

TABLE 3-5: WRITE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Load write buffer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 3: Repeat for all but the last two bytes.		
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
Step 4: Load write buffer for last two bytes.		
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
To continue writing data, repeat Steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop.		

PIC18F2XXX/4XXX FAMILY

FIGURE 3-4: PROGRAM CODE MEMORY FLOW

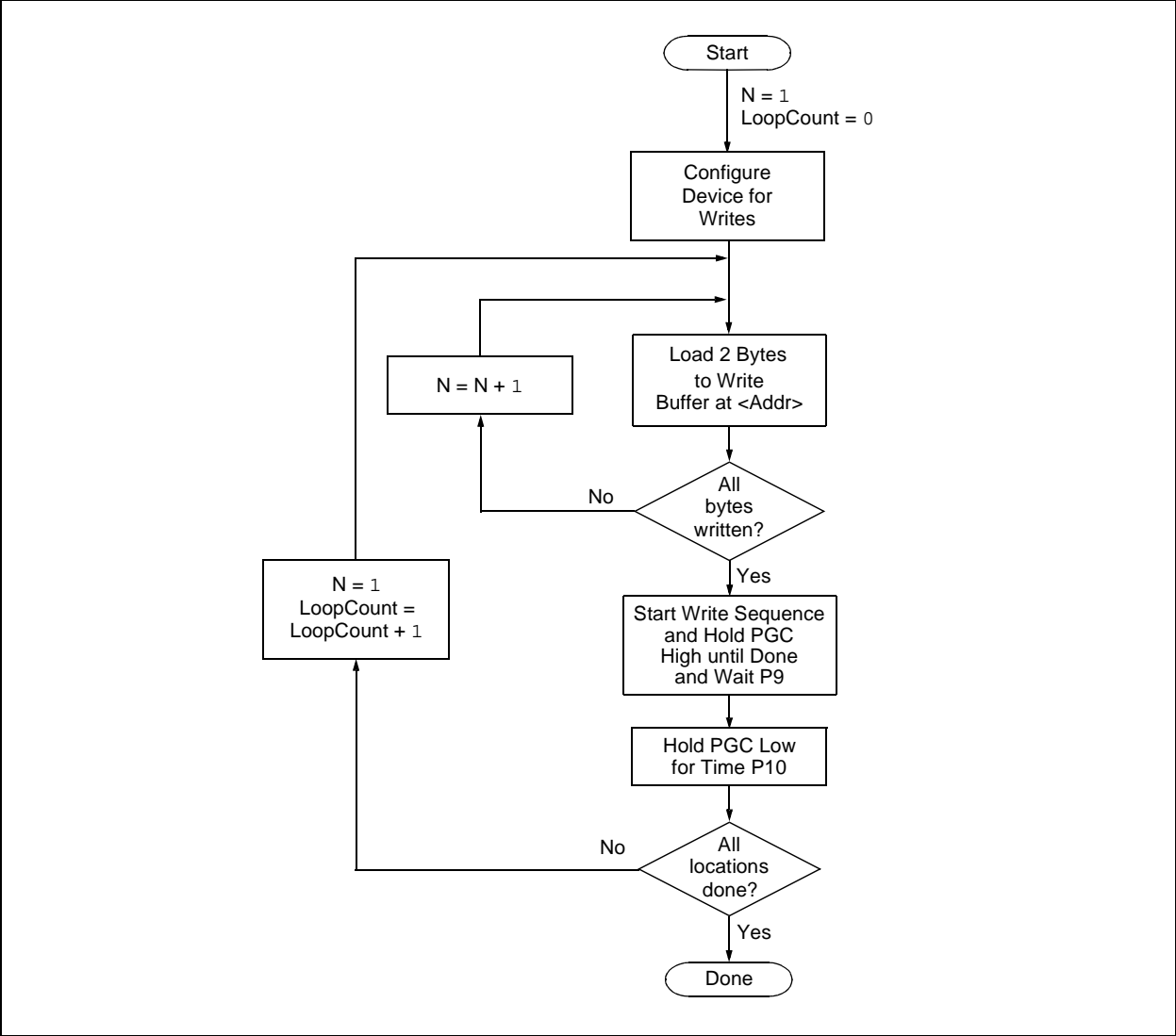
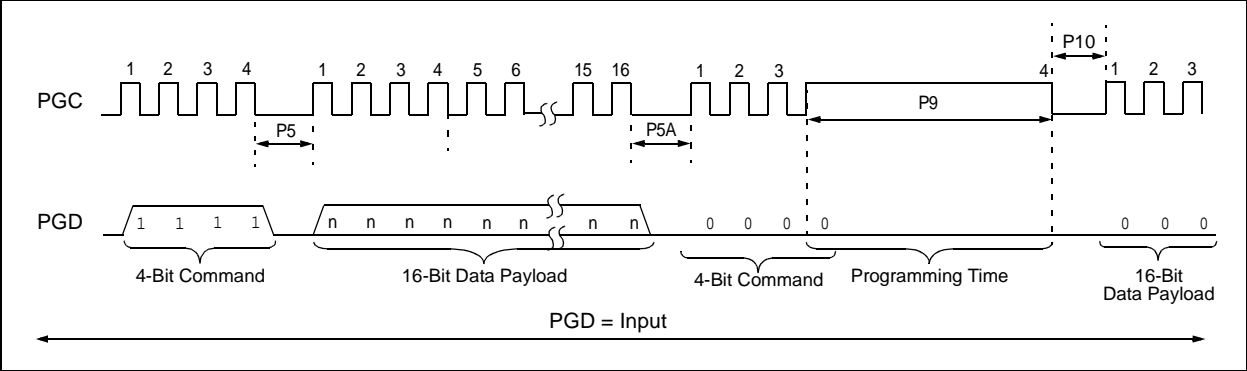


FIGURE 3-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



PIC18F2XXX/4XXX FAMILY

3.4 ID Location Programming

The ID locations are programmed much like the code memory. The ID registers are mapped in addresses, 200000h through 200007h. These locations read out normally even after code protection.

Note: The user only needs to fill the first 8 bytes of the write buffer in order to write the ID locations.

Table 3-8 demonstrates the code sequence required to write the ID locations.

In order to modify the ID locations, refer to the methodology described in [Section 3.2.1 “Modifying Code Memory”](#). As with code memory, the ID locations must be erased before being modified.

TABLE 3-8: WRITE ID SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Load write buffer with 8 bytes and write.		
0000	0E 20	MOVLW 20h
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 00	MOVLW 00h
0000	6E F6	MOVWF TBLPTRL
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.

3.5 Boot Block Programming

The code sequence detailed in [Table 3-5](#) should be used, except that the address used in “Step 2” will be in the range of 000000h to 0007FFh.

3.6 Configuration Bits Programming

Unlike code memory, the Configuration bits are programmed a byte at a time. The Table Write, Begin Programming 4-bit command ('1111') is used, but only eight bits of the following 16-bit payload will be written. The LSB of the payload will be written to even addresses and the MSB will be written to odd addresses. The code sequence to program two consecutive configuration locations is shown in [Table 3-9](#).

Note: The address must be explicitly written for each byte programmed. The addresses can not be incremented in this mode.

4.0 READING THE DEVICE

4.1 Read Code Memory, ID Locations and Configuration Bits

Code memory is accessed, one byte at a time, via the 4-bit command, '1001' (Table Read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

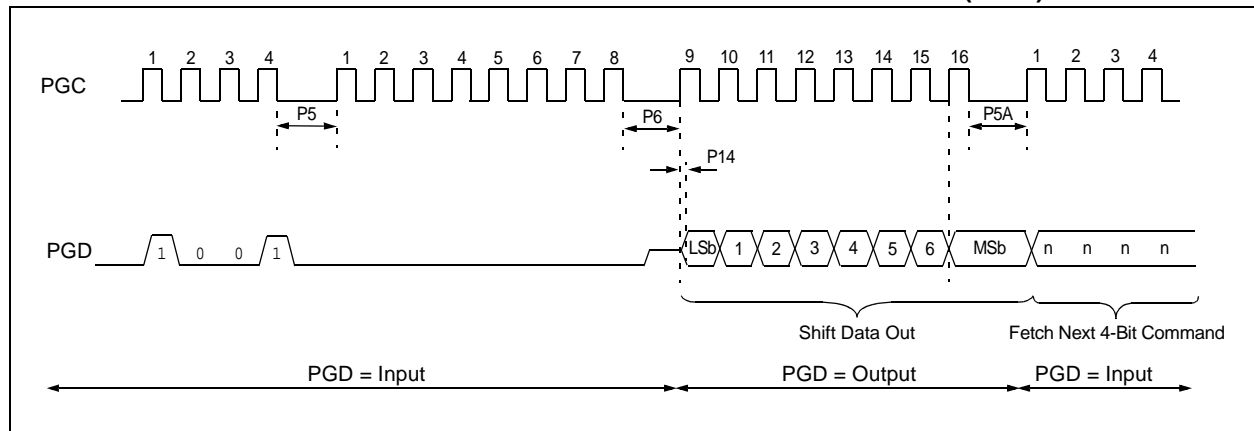
The 4-bit command is shifted in, LSb first. The read is executed during the next eight clocks, then shifted out on PGD during the last eight clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see [Figure 4-1](#)). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFFh address space, so it also applies to the reading of the ID and Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

FIGURE 4-1: TABLE READ POST-INCREMENT INSTRUCTION TIMING (1001)



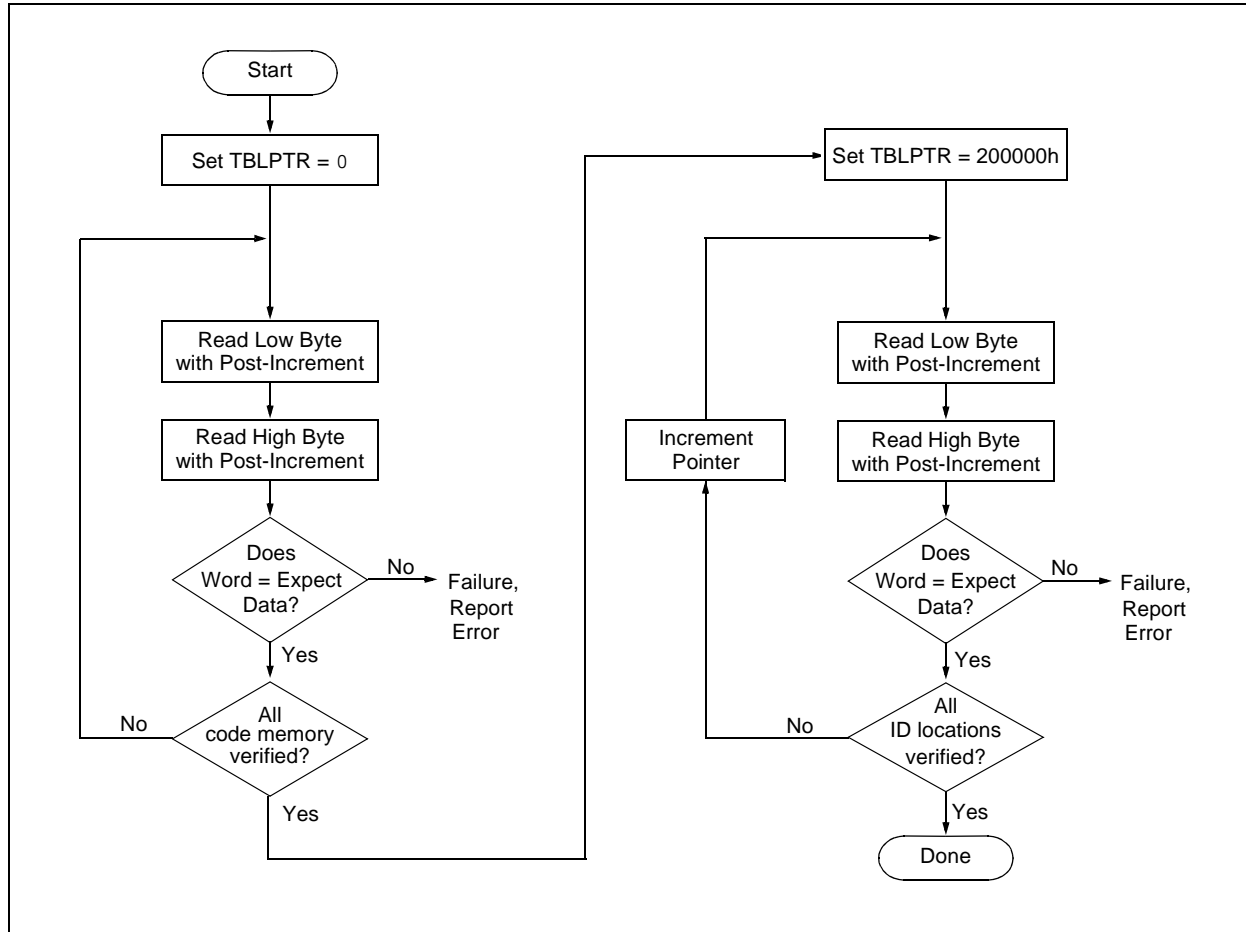
PIC18F2XXX/4XXX FAMILY

4.2 Verify Code Memory and ID Locations

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to [Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"](#) for implementation details of reading code memory.

The Table Pointer must be manually set to 200000h (base address of the ID locations) once the code memory has been verified. The post-increment feature of the Table Read 4-bit command may not be used to increment the Table Pointer beyond the code memory space. In a 64-Kbyte device, for example, a post-increment read of address, FFFFh, will wrap the Table Pointer back to 000000h, rather than point to the unimplemented address, 010000h.

FIGURE 4-2: VERIFY CODE MEMORY FLOW



4.3 Verify Configuration Bits

A configuration address may be read and output on PGD via the 4-bit command, '1001'. Configuration data is read and written in a byte-wise fashion, so it is not necessary to merge two bytes into a word prior to a compare. The result may then be immediately compared to the appropriate configuration data in the programmer's memory for verification. Refer to [Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"](#) for implementation details of reading configuration data.

The diagram illustrates the timing relationship between the PGC (Pulse Generator Clock) and PGD (Programmable Generator Data) signals. The PGC signal is a periodic clock with specific periods labeled P5, P6, and P5A. The PGD signal is a data bus that is input during P5, output during P6, and input again during P5A. The output data is shown as a sequence of bits: LSb, 1, 2, 3, 4, 5, 6, MSb, followed by four 'n' bits. The diagram is divided into three sections: PGD = Input, PGD = Output, and PGD = Input.

A data EEPROM address may be read via a sequence of core instructions (4-bit command, '0000') and then output on PGD via the 4-bit command, '0010' (TABLAT register). The result may then be immediately compared to the appropriate data in the programmer's memory for verification. Refer to [Section 4.4 "Read Data EEPROM Memory"](#) for implementation details of reading data EEPROM.

The term Blank Check means to verify that the device has no programmed memory cells. All memories must be verified: code memory, data EEPROM, ID locations and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

Given that Blank Checking is merely code and data EEPROM verification with FFh expect data, refer to [Section 4.4 “Read Data EEPROM Memory”](#) and [Section 4.2 “Verify Code Memory and ID Locations”](#) for implementation details.

```
graph TD; Start([Start]) --> BlankCheck[Blank Check Device]; BlankCheck --> IsBlank{Is device blank?}; IsBlank -- Yes --> Continue([Continue]); IsBlank -- No --> Abort([Abort]);
```

PIC18F2XXX/4XXX FAMILY

TABLE 5-2: DEVICE ID VALUES (CONTINUED)

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F4585	0Eh	101x xxxx
PIC18F4610	0Ch	001x xxxx
PIC18F4620	0Ch	000x xxxx
PIC18F4680	0Eh	100x xxxx
PIC18F4682	27h	010x xxxx
PIC18F4685	27h	011x xxxx

Legend: The 'x's in DEVID1 contain the device revision code.

Note 1: DEVID1 bit 4 is used to determine the device type (REV4 = 0).

2: DEVID1 bit 4 is used to determine the device type (REV4 = 1).

PIC18F2XXX/4XXX FAMILY

TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
PLLDIV<2:0>	CONFIG1L	Oscillator Selection bits (PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only) Divider must be selected to provide a 4 MHz input into the 96 MHz PLL: 111 = Oscillator divided by 12 (48 MHz input) 110 = Oscillator divided by 10 (40 MHz input) 101 = Oscillator divided by 6 (24 MHz input) 100 = Oscillator divided by 5 (20 MHz input) 011 = Oscillator divided by 4 (16 MHz input) 010 = Oscillator divided by 3 (12 MHz input) 001 = Oscillator divided by 2 (8 MHz input) 000 = No divide – oscillator used directly (4 MHz input)
VREGEN	CONFIG2L	USB Voltage Regulator Enable bit (PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only) 1 = USB voltage regulator is enabled 0 = USB voltage regulator is disabled
BORV<1:0>	CONFIG2L	Brown-out Reset Voltage bits 11 = VBOR is set to 2.0V 10 = VBOR is set to 2.7V 01 = VBOR is set to 4.2V 00 = VBOR is set to 4.5V
BOREN<1:0>	CONFIG2L	Brown-out Reset Enable bits 11 = Brown-out Reset is enabled in hardware only (SBOREN is disabled) 10 = Brown-out Reset is enabled in hardware only and disabled in Sleep mode (SBOREN is disabled) 01 = Brown-out Reset is enabled and controlled by software (SBOREN is enabled) 00 = Brown-out Reset is disabled in hardware and software
PWRTEN	CONFIG2L	Power-up Timer Enable bit 1 = PWRT is disabled 0 = PWRT is enabled
WDPS<3:0>	CONFIG2H	Watchdog Timer Postscaler Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

PIC18F2XXX/4XXX FAMILY

TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
WDTEN	CONFIG2H	Watchdog Timer Enable bit 1 = WDT is enabled 0 = WDT is disabled (control is placed on the SWDTEN bit)
MCLRE	CONFIG3H	MCLR Pin Enable bit 1 = MCLR pin is enabled, RE3 input pin is disabled 0 = RE3 input pin is enabled, MCLR pin is disabled
LPT1OSC	CONFIG3H	Low-Power Timer1 Oscillator Enable bit 1 = Timer1 is configured for low-power operation 0 = Timer1 is configured for high-power operation
PBADEN	CONFIG3H	PORTB A/D Enable bit 1 = PORTB A/D<4:0> pins are configured as analog input channels on Reset 0 = PORTB A/D<4:0> pins are configured as digital I/O on Reset
PBADEN	CONFIG3H	PORTB A/D Enable bit (PIC18FXX8X devices only) 1 = PORTB A/D<4:0> and PORTB A/D<1:0> pins are configured as analog input channels on Reset 0 = PORTB A/D<4:0> pins are configured as digital I/O on Reset
CCP2MX	CONFIG3H	CCP2 MUX bit 1 = CCP2 input/output is multiplexed with RC1 ⁽²⁾ 0 = CCP2 input/output is multiplexed with RB3
DEBUG	CONFIG4L	Background Debugger Enable bit 1 = Background debugger is disabled, RB6 and RB7 are configured as general purpose I/O pins 0 = Background debugger is enabled, RB6 and RB7 are dedicated to In-Circuit Debug
XINST	CONFIG4L	Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode are enabled 0 = Instruction set extension and Indexed Addressing mode are disabled (Legacy mode)
ICPRT	CONFIG4L	Dedicated In-Circuit (ICD/ICSP™) Port Enable bit (PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only) 1 = ICPORT is enabled 0 = ICPORT is disabled
BBSIZ<1:0> ⁽¹⁾	CONFIG4L	Boot Block Size Select bits (PIC18F2585/2680/4585/4680 devices only) 11 = 4K words (8 Kbytes) Boot Block 10 = 4K words (8 Kbytes) Boot Block 01 = 2K words (4 Kbytes) Boot Block 00 = 1K word (2 Kbytes) Boot Block
BBSIZ<2:1> ⁽¹⁾	CONFIG4L	Boot Block Size Select bits (PIC18F2682/2685/4582/4685 devices only) 11 = 4K words (8 Kbytes) Boot Block 10 = 4K words (8 Kbytes) Boot Block 01 = 2K words (4 Kbytes) Boot Block 00 = 1K word (2 Kbytes) Boot Block

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

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TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
WRT5	CONFIG6L	Write Protection bit (Block 5 code memory area) (PIC18F2685 and PIC18F4685 devices only) 1 = Block 5 is not write-protected 0 = Block 5 is write-protected
WRT4	CONFIG6L	Write Protection bit (Block 4 code memory area) (PIC18F2682/2685 and PIC18F4682/4685 devices only) 1 = Block 4 is not write-protected 0 = Block 4 is write-protected
WRT3	CONFIG6L	Write Protection bit (Block 3 code memory area) 1 = Block 3 is not write-protected 0 = Block 3 is write-protected
WRT2	CONFIG6L	Write Protection bit (Block 2 code memory area) 1 = Block 2 is not write-protected 0 = Block 2 is write-protected
WRT1	CONFIG6L	Write Protection bit (Block 1 code memory area) 1 = Block 1 is not write-protected 0 = Block 1 is write-protected
WRT0	CONFIG6L	Write Protection bit (Block 0 code memory area) 1 = Block 0 is not write-protected 0 = Block 0 is write-protected
WRTD	CONFIG6H	Write Protection bit (Data EEPROM) 1 = Data EEPROM is not write-protected 0 = Data EEPROM is write-protected
WRTB	CONFIG6H	Write Protection bit (Boot Block memory area) 1 = Boot Block is not write-protected 0 = Boot Block is write-protected
WRTC	CONFIG6H	Write Protection bit (Configuration registers) 1 = Configuration registers are not write-protected 0 = Configuration registers are write-protected
EBTR5	CONFIG7L	Table Read Protection bit (Block 5 code memory area) (PIC18F2685 and PIC18F4685 devices only) 1 = Block 5 is not protected from Table Reads executed in other blocks 0 = Block 5 is protected from Table Reads executed in other blocks
EBTR4	CONFIG7L	Table Read Protection bit (Block 4 code memory area) (PIC18F2682/2685 and PIC18F4682/4685 devices only) 1 = Block 4 is not protected from Table Reads executed in other blocks 0 = Block 4 is protected from Table Reads executed in other blocks
EBTR3	CONFIG7L	Table Read Protection bit (Block 3 code memory area) 1 = Block 3 is not protected from Table Reads executed in other blocks 0 = Block 3 is protected from Table Reads executed in other blocks
EBTR2	CONFIG7L	Table Read Protection bit (Block 2 code memory area) 1 = Block 2 is not protected from Table Reads executed in other blocks 0 = Block 2 is protected from Table Reads executed in other blocks
EBTR1	CONFIG7L	Table Read Protection bit (Block 1 code memory area) 1 = Block 1 is not protected from Table Reads executed in other blocks 0 = Block 1 is protected from Table Reads executed in other blocks

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

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TABLE 5-4: DEVICE BLOCK LOCATIONS AND SIZES

Device	Memory Size (Bytes)	Pins	Ending Address							Size (Bytes)			
			Boot Block	Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Boot Block	Block 0	Remaining Blocks	Device Total
PIC18F2221	4K	28	0001FF	0007FF	000FFF	—	—	—	—	512	1536	2048	4096
			0003FF							1024	1024		
PIC18F2321	8K	28	0001FF	000FFF	001FFF	—	—	—	—	512	3584	4096	8192
			0003FF							1024	3072		
			0007FF							2048	2048		
PIC18F2410	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F2420	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F2423	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F2450	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		
PIC18F2455	24K	28	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F2458	24K	28	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F2480	16K	28	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		
PIC18F2510	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F2515	48K	28	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F2520	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F2523	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F2525	48K	28	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F2550	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F2553	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F2580	32K	28	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
			000FFF							4096	4096		
PIC18F2585	48K	28	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F2610	64K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F2620	64K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F2680	64K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F2682	80K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	—	2048	14336	65536	81920
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F2685	96K	28	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	017FFF	2048	14336	81920	98304
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4221	4K	40	0001FF	0007FF	000FFF	—	—	—	—	512	1536	2048	4096
			0003FF							1024	1024		
PIC18F4321	8K	40	0001FF	000FFF	001FFF	—	—	—	—	512	3584	4096	8192
			0003FF							1024	3072		
			0007FF							2048	2048		
PIC18F4410	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F4420	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F4423	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
PIC18F4450	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		

Legend: — = unimplemented.

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6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions						
Operating Temperature: 25°C is recommended						
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
P11A	TDRWT	Data Write Polling Time	4	—	ms	
P12	THLD2	Input Data Hold Time from $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \uparrow$	2	—	μs	
P13	TSET2	$\text{VDD} \uparrow$ Setup Time to $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \uparrow$	100	—	ns	(Note 2)
P14	TVALID	Data Out Valid from PGC \uparrow	10	—	ns	
P15	TSET3	PGM \uparrow Setup Time to $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \uparrow$	2	—	μs	(Note 2)
P16	TDLY8	Delay Between Last PGC \downarrow and $\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \downarrow$	0	—	s	
P17	THLD3	$\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \downarrow$ to $\text{VDD} \downarrow$	—	100	ns	
P18	THLD4	$\overline{\text{MCLR}}/\text{VPP}/\text{RE3} \downarrow$ to PGM \downarrow	0	—	s	

- Note 1:** Do not allow excess time when transitioning $\overline{\text{MCLR}}$ between VIL and VIHH . This can cause spurious program executions to occur. The maximum transition time is:
1 $\text{T}_{\text{CY}} + \text{T}_{\text{PWRT}}$ (if enabled) + 1024 T_{OSC} (for LP, HS, HS/PLL and XT modes only) +
2 ms (for HS/PLL mode only) + 1.5 μs (for EC mode only)
where T_{CY} is the instruction cycle time, T_{PWRT} is the Power-up Timer period and T_{OSC} is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.
- 2:** When $\text{ICPRT} = 1$, this specification also applies to ICVPP .
- 3:** At 0°C-50°C.