What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4510t-i-pt

PIC18F2XXX/4XXX FAMILY

TABLE 2-1:   PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F2XXX/4XXX FAMILY

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
$\overline{MCLR}$/Vpp/RE3	VPP	P	Programming Enable
VDD[(2)]	VDD	P	Power Supply
VSS[(2)]	VSS	P	Ground
RB5	PGM	I	Low-Voltage ICSP™ Input when LVP Configuration bit equals '1'[(1)]
RB6	PGC	I	Serial Clock
RB7	PGD	I/O	Serial Data

Legend: I = Input, O = Output, P = Power
Note   1:   See Figure 5-1 for more information.
       2:   All power supply (VDD) and ground (VSS) pins must be connected.

The following devices are included in 28-pin SPDIP, PDIP and SOIC parts:

- PIC18F2221
- PIC18F2321
- PIC18F2410
- PIC18F2420
- PIC18F2423
- PIC18F2450
- PIC18F2455
- PIC18F2458

- PIC18F2480
- PIC18F2510
- PIC18F2515
- PIC18F2520
- PIC18F2523
- PIC18F2525
- PIC18F2550
- PIC18F2553

- PIC18F2580
- PIC18F2585
- PIC18F2610
- PIC18F2620
- PIC18F2680
- PIC18F2682
- PIC18F2685

The following devices are included in 28-pin SSOP parts:

- PIC18F2221

- PIC18F2321

**FIGURE 2-1:   28-Pin SPDIP, PDIP, SOIC, SSOP**

The following devices are included in 44-pin QFN parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4520
- PIC18F4515

- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

FIGURE 2-5: **44-PIN QFN**
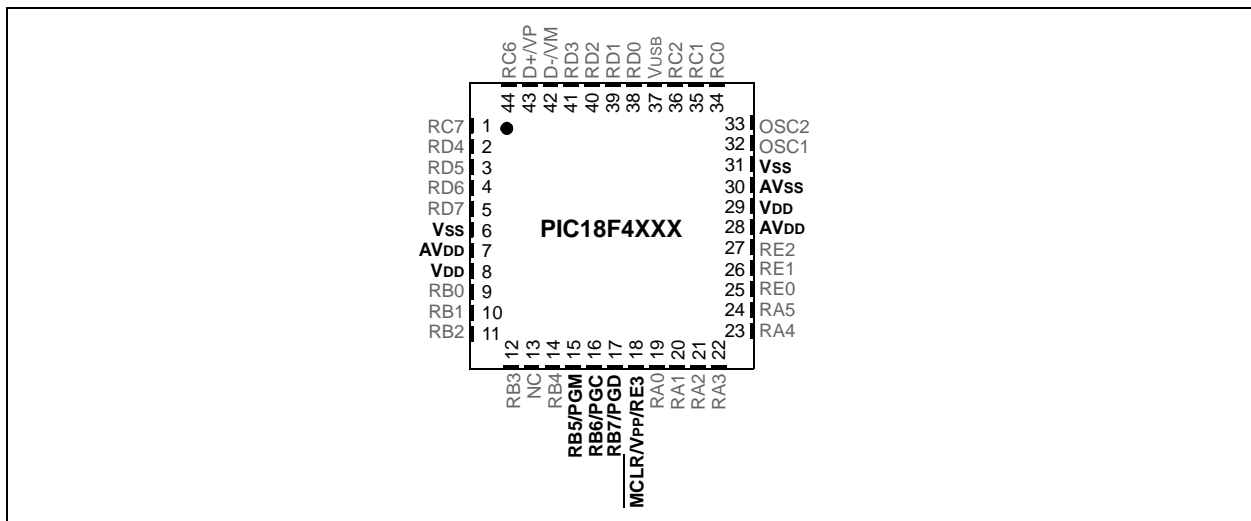
2.3 Memory Maps

For PIC18FX6X0 devices, the code memory space extends from 0000h to 0FFFFh (64 Kbytes) in four 16-Kbyte blocks. For PIC18FX5X5 devices, the code memory space extends from 0000h to 0BFFFFh (48 Kbytes) in three 16-Kbyte blocks. Addresses, 0000h through 07FFh, however, define a "Boot Block" region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

The size of the Boot Block in PIC18F2585/2680/4585/4680 devices can be configured as 1, 2 or 4K words (see Figure 2-6). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.
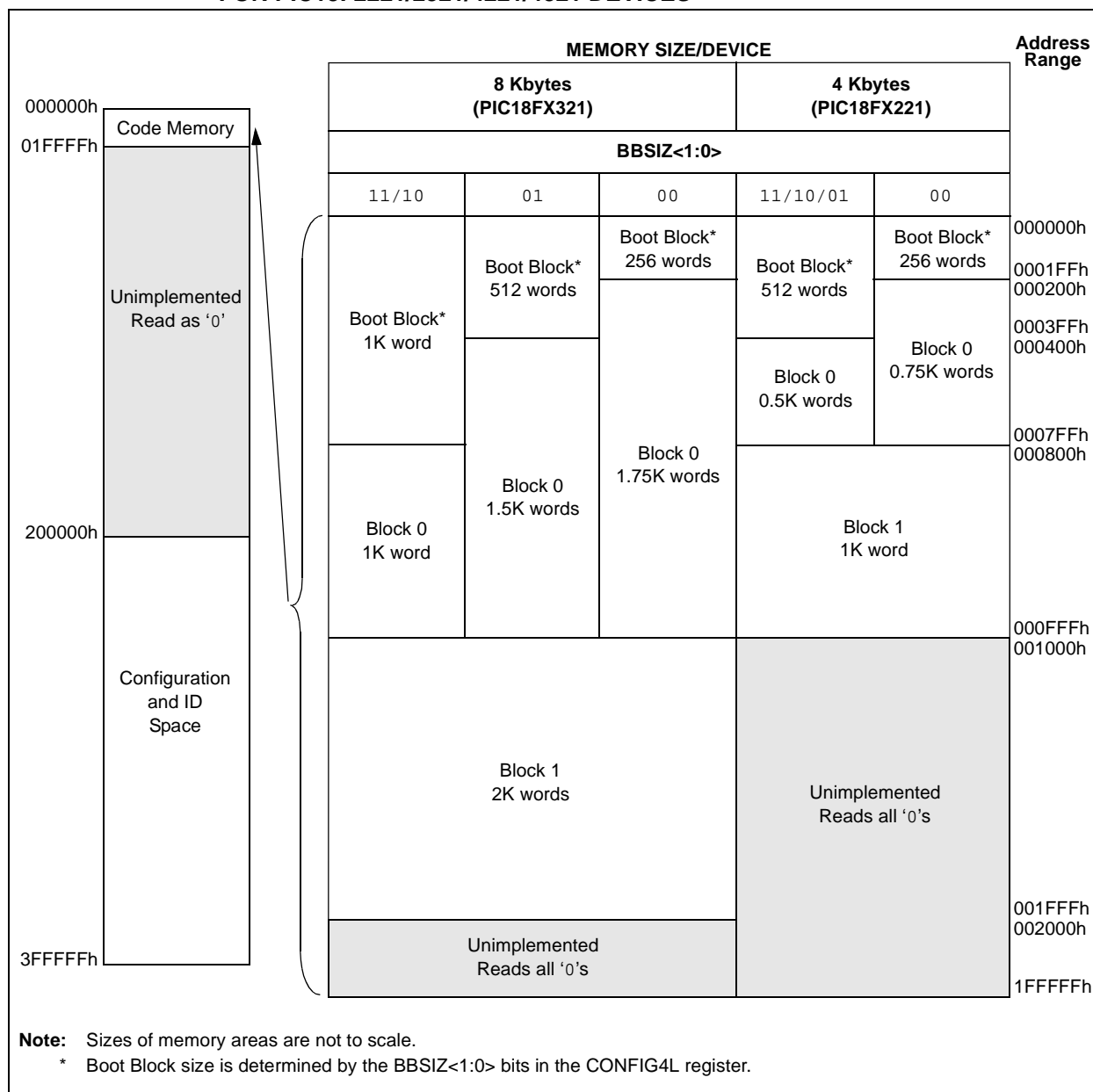
PIC18F2XXX/4XXX FAMILY

The size of the Boot Block in PIC18F2221/2321/4221/4321 devices can be configured as 256, 512 or 1024 words (see Figure 2-11). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L (see Figure 2-11). It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

TABLE 2-7: **IMPLEMENTATION OF CODE MEMORY**

Device	Code Memory Size (Bytes)
PIC18F2221	000000h-000FFFh (4K)
PIC18F4221	
PIC18F2321	000000h-001FFFh (8K)
PIC18F4321	

FIGURE 2-11: **MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2221/2321/4221/4321 DEVICES**

Note: Sizes of memory areas are not to scale.

* Boot Block size is determined by the BBSIZ<1:0> bits in the CONFIG4L register.

In addition to the code memory space, there are three blocks that are accessible to the user through Table Reads and Table Writes. Their locations in the memory map are shown in Figure 2-12.

Users may store identification information (ID) in eight ID registers. These ID registers are mapped in addresses, 200000h through 200007h. The ID locations read out normally, even after code protection is applied.

Locations, 300000h through 30000Dh, are reserved for the Configuration bits. These bits select various device options and are described in **Section 5.0 "Configuration Word"**. These Configuration bits read out normally, even after code protection.

Locations, 3FFFFEh and 3FFFFFh, are reserved for the Device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.0 "Configuration Word"**. These Device ID bits read out normally, even after code protection.

2.3.1 MEMORY ADDRESS POINTER

Memory in the address space, 0000000h to 3FFFFFh, is addressed via the Table Pointer register, which is comprised of three pointer registers:

- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

FIGURE 2-12: **CONFIGURATION AND ID LOCATIONS FOR PIC18F2XXX/4XXX FAMILY DEVICES**

ID Location 1	200000h	
ID Location 2	200001h	
ID Location 3	200002h	
ID Location 4	200003h	
ID Location 5	200004h	
ID Location 6	200005h	
ID Location 7	200006h	
ID Location 8	200007h	

CONFIG1L	300000h
CONFIG1H	300001h
CONFIG2L	300002h
CONFIG2H	300003h
CONFIG3L	300004h
CONFIG3H	300005h
CONFIG4L	300006h
CONFIG4H	300007h
CONFIG5L	300008h
CONFIG5H	300009h
CONFIG6L	30000Ah
CONFIG6H	30000Bh
CONFIG7L	30000Ch
CONFIG7H	30000Dh

Device ID1	3FFFFEh
Device ID2	3FFFFFh

Code Memory: 000000h – 01FFFFh

Unimplemented Read as '0'

1FFFFFh

Configuration and ID Space

2FFFFFh

3FFFFFh

Note: Sizes of memory areas are not to scale.

2.4   High-Level Overview of the Programming Process

Figure 2-13 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory, ID locations and data EEPROM are programmed (selected devices only, see **Section 3.3 "Data EEPROM Programming"**). These memories are then verified to ensure that programming was successful. If no errors are detected, the Configuration bits are then programmed and verified.

**FIGURE 2-13:**   **HIGH-LEVEL PROGRAMMING FLOW**

```
                    ( Start )
                       |
              ┌─────────────────┐
              │  Perform Bulk   │
              │     Erase       │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │ Program Memory  │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │   Program IDs   │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │ Program Data EE(1)│
              └─────────────────┘
                       |
              ┌─────────────────┐
              │ Verify Program  │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │   Verify IDs    │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │   Verify Data   │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │    Program      │
              │ Configuration   │
              │     Bits        │
              └─────────────────┘
                       |
              ┌─────────────────┐
              │    Verify       │
              │ Configuration   │
              │     Bits        │
              └─────────────────┘
                       |
                    ( Done )
```

Note   1:   Selected devices only, see **Section 3.3 "Data EEPROM Programming"**.

2.5 Entering and Exiting High-Voltage ICSP Program/Verify Mode

As shown in Figure 2-14, the High-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low and then raising MCLR/VPP/RE3 to VIHH (high voltage). Once in this mode, the code memory, data EEPROM (selected devices only, see **Section 3.3 "Data EEPROM Programming"**), ID locations and Configuration bits can be accessed and programmed in serial fashion. Figure 2-15 shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-14:   ENTERING HIGH-VOLTAGE PROGRAM/VERIFY MODE

FIGURE 2-15:   EXITING HIGH-VOLTAGE PROGRAM/VERIFY MODE

2.6   Entering and Exiting Low-Voltage ICSP Program/Verify Mode

When the LVP Configuration bit is '1' (see **Section 5.3 "Single-Supply ICSP Programming"**), the Low-Voltage ICSP mode is enabled. As shown in Figure 2-16, Low-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low, placing a logic high on PGM and then raising MCLR/VPP/RE3 to VIH. In this mode, the RB5/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. Figure 2-17 shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-16:   ENTERING LOW-VOLTAGE PROGRAM/VERIFY MODE
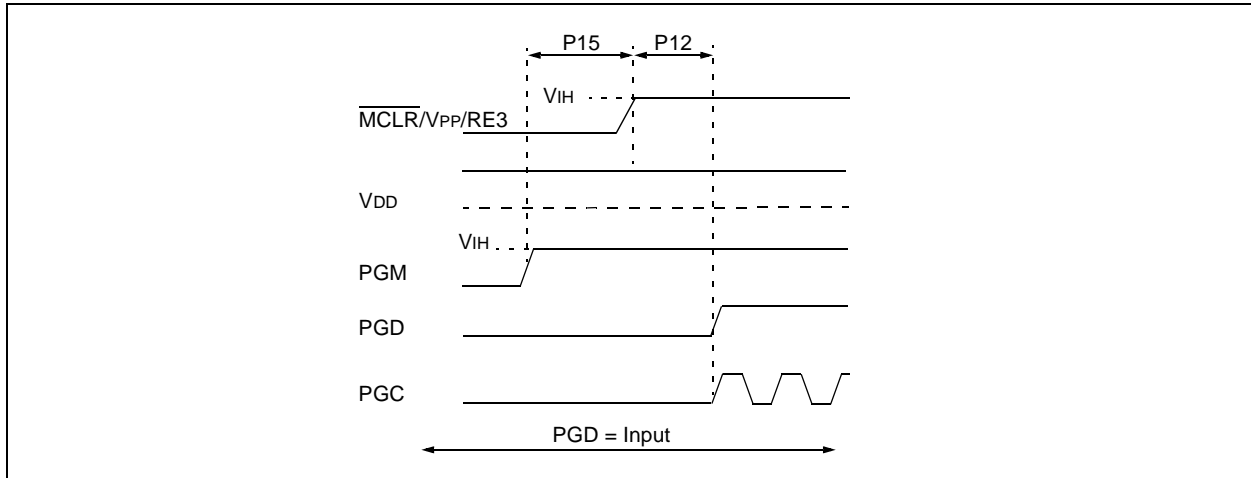
FIGURE 2-17:   EXITING LOW-VOLTAGE PROGRAM/VERIFY MODE
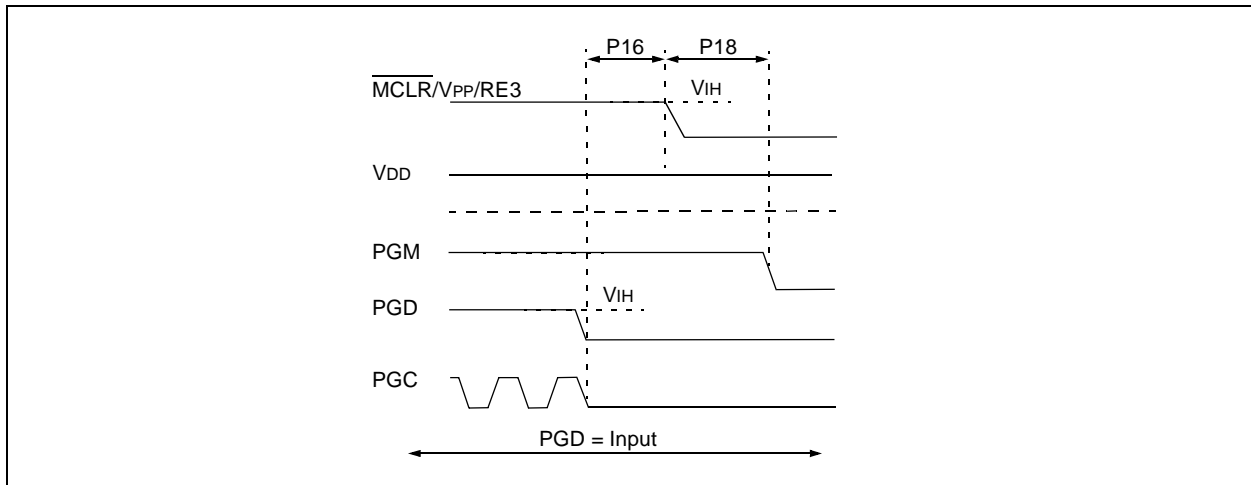
3.0   DEVICE PROGRAMMING

Programming includes the ability to erase or write the various memory regions within the device.

In all cases, except high-voltage ICSP Bulk Erase, the EECON1 register must be configured in order to operate on a particular memory region.

When using the EECON1 register to act on code memory, the EEPGD bit must be set (EECON1<7> = 1) and the CFGS bit must be cleared (EECON1<6> = 0). The WREN bit must be set (EECON1<2> = 1) to enable writes of any sort (e.g., erases) and this must be done prior to initiating a write sequence. The FREE bit must be set (EECON1<4> = 1) in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit (EECON1<1> = 1). It is strongly recommended that the WREN bit only be set immediately prior to a program erase.

3.1   ICSP Erase

3.1.1   HIGH-VOLTAGE ICSP BULK ERASE

Erasing code or data EEPROM is accomplished by configuring two Bulk Erase Control registers located at 3C0004h and 3C0005h. Code memory may be erased, portions at a time, or the user may erase the entire device in one action. Bulk Erase operations will also clear any code-protect settings associated with the memory block being erased. Erase options are detailed in Table 3-1. If data EEPROM is code-protected (CPD = 0), the user must request an erase of data EEPROM (e.g., 0084h as shown in Table 3-1).

TABLE 3-1:   BULK ERASE OPTIONS

Description	Data (3C0005h:3C0004h)
Chip Erase	3F8Fh
Erase Data EEPROM[1]	0084h
Erase Boot Block	0081h
Erase Configuration Bits	0082h
Erase Code EEPROM Block 0	0180h
Erase Code EEPROM Block 1	0280h
Erase Code EEPROM Block 2	0480h
Erase Code EEPROM Block 3	0880h
Erase Code EEPROM Block 4	1080h
Erase Code EEPROM Block 5	2080h

Note 1:   Selected devices only, see **Section 3.3 "Data EEPROM Programming"**.

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the NOP command), serial execution will cease until the erase completes (Parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

The code sequence to erase the entire device is shown in Table and the flowchart is shown in Figure 3-1.

> **Note:**   A Bulk Erase is the only way to reprogram code-protect bits from an ON state to an OFF state.

TABLE 3-3: **ERASE CODE MEMORY CODE SEQUENCE**

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in code memory.		
0000	6A F8	CLRF TBLPTRU
0000	6A F7	CLRF TBLPTRH
0000	6A F6	CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP – hold PGC high for time P9 and low for time P10.
Step 4: Repeat Step 3, with the Address Pointer incremented by 64 until all rows are erased.		

FIGURE 3-3: **SINGLE ROW ERASE CODE MEMORY FLOW**
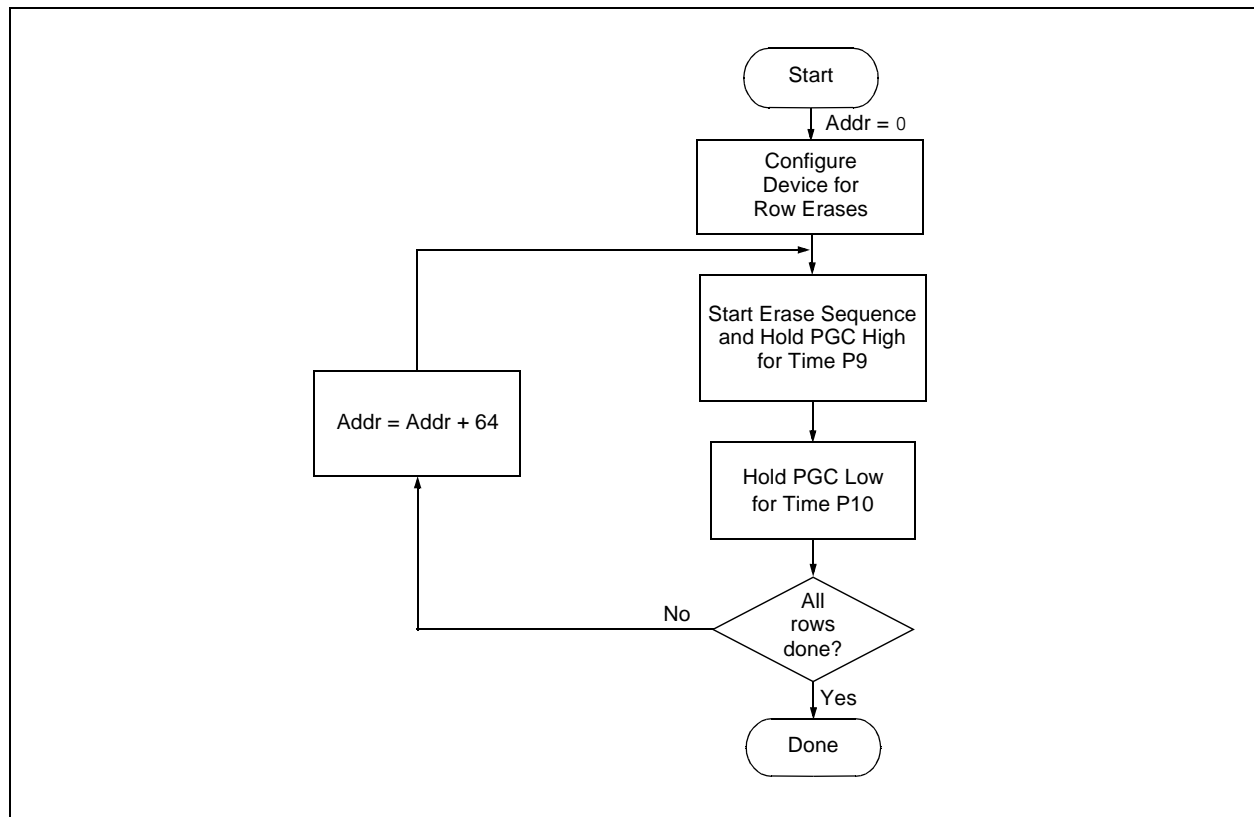
FIGURE 3-7: DATA EEPROM WRITE TIMING
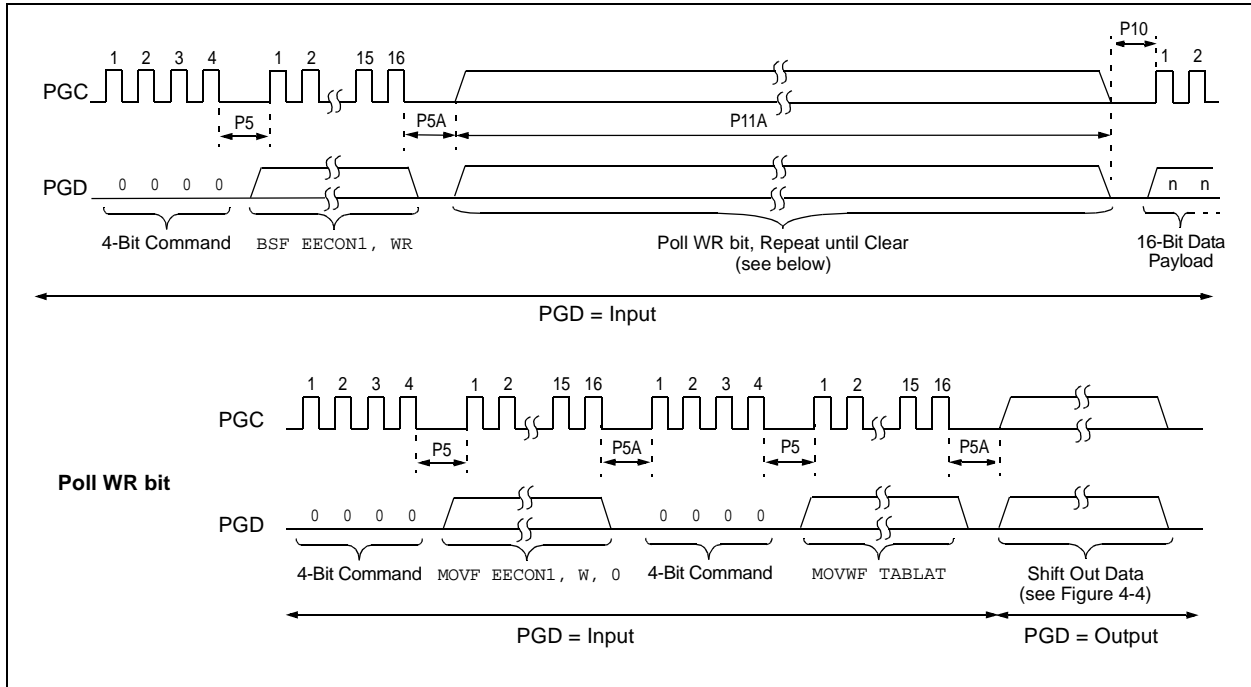
4.4 Read Data EEPROM Memory

Data EEPROM is accessed, one byte at a time, via an Address Pointer (register pair: EEADRH:EEADR) and a data latch (EEDATA). Data EEPROM is read by loading EEADRH:EEADR with the desired memory location and initiating a memory read by appropriately configuring the EECON1 register. The data will be loaded into EEDATA, where it may be serially output on PGD via the 4-bit command, '0010' (Shift Out Data Holding register). A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-4).

The command sequence to read a single byte of data is shown in Table 4-2.

FIGURE 4-3:   READ DATA EEPROM FLOW
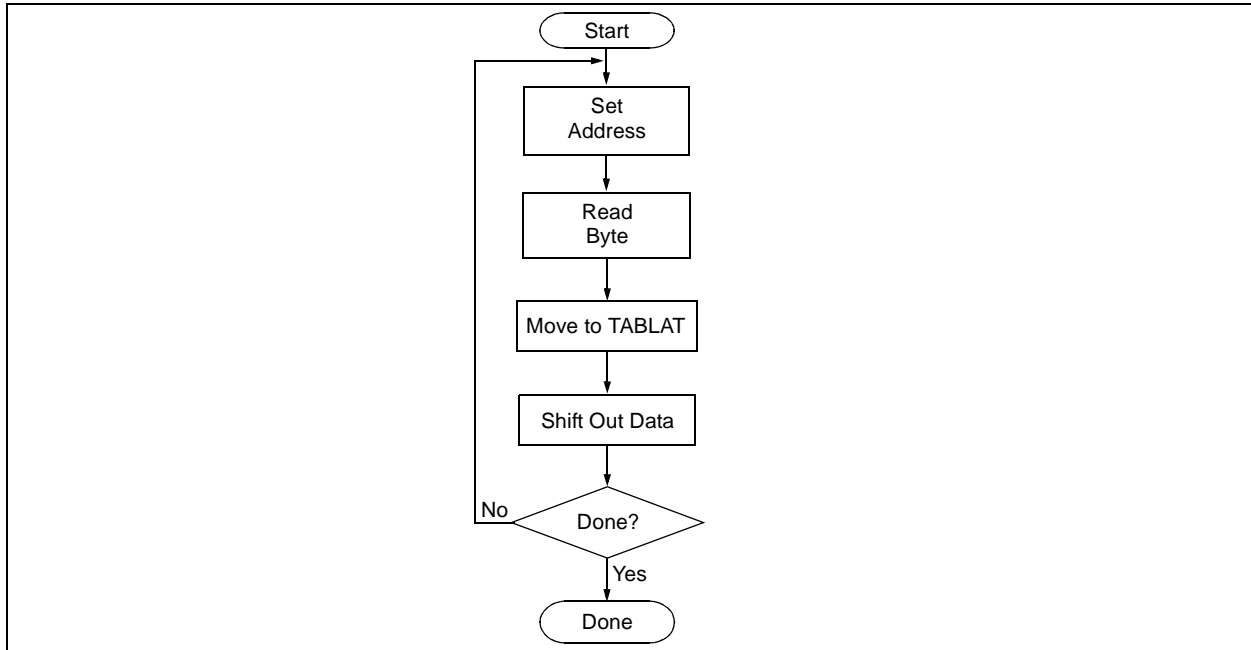
TABLE 4-2:   READ DATA EEPROM MEMORY

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to data EEPROM.		
0000 0000	9E A6 9C A6	BCF EECON1, EEPGD BCF EECON1, CFGS
Step 2: Set the data EEPROM Address Pointer.		
0000 0000 0000 0000	0E <Addr> 6E A9 OE <AddrH> 6E AA	MOVLW <Addr> MOVWF EEADR MOVLW <AddrH> MOVWF EEADRH
Step 3: Initiate a memory read.		
0000	80 A6	BSF EECON1, RD
Step 4: Load data into the Serial Data Holding register.		
0000 0000 0000 0010	50 A8 6E F5 00 00 <MSB><LSB>	MOVF EEDATA, W, 0 MOVWF TABLAT NOP Shift Out Data[1]

Note   1:   The <LSB> is undefined. The <MSB> is the data.

TABLE 5-2: DEVICE ID VALUES

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F2221	21h	`011x xxxx`
PIC18F2321	21h	`001x xxxx`
PIC18F2410	11h	`011x xxxx`
PIC18F2420	11h	`010x xxxx`[1]
PIC18F2423	11h	`010x xxxx`[2]
PIC18F2450	24h	`001x xxxx`
PIC18F2455	12h	`011x xxxx`
PIC18F2458	2Ah	`011x xxxx`
PIC18F2480	1Ah	`111x xxxx`
PIC18F2510	11h	`001x xxxx`
PIC18F2515	0Ch	`111x xxxx`
PIC18F2520	11h	`000x xxxx`[1]
PIC18F2523	11h	`000x xxxx`[2]
PIC18F2525	0Ch	`110x xxxx`
PIC18F2550	12h	`010x xxxx`
PIC18F2553	2Ah	`010x xxxx`
PIC18F2580	1Ah	`110x xxxx`
PIC18F2585	0Eh	`111x xxxx`
PIC18F2610	0Ch	`101x xxxx`
PIC18F2620	0Ch	`100x xxxx`
PIC18F2680	0Eh	`110x xxxx`
PIC18F2682	27h	`000x xxxx`
PIC18F2685	27h	`001x xxxx`
PIC18F4221	21h	`010x xxxx`
PIC18F4321	21h	`000x xxxx`
PIC18F4410	10h	`111x xxxx`
PIC18F4420	10h	`110x xxxx`[1]
PIC18F4423	10h	`110x xxxx`[2]
PIC18F4450	24h	`000x xxxx`
PIC18F4455	12h	`001x xxxx`
PIC18F4458	2Ah	`001x xxxx`
PIC18F4480	1Ah	`101x xxxx`
PIC18F4510	10h	`101x xxxx`
PIC18F4515	0Ch	`011x xxxx`
PIC18F4520	10h	`100x xxxx`[1]
PIC18F4523	10h	`100x xxxx`[2]
PIC18F4525	0Ch	`010x xxxx`
PIC18F4550	12h	`000x xxxx`
PIC18F4553	2Ah	`000x xxxx`
PIC18F4580	1Ah	`100x xxxx`

Legend: The 'x's in DEVID1 contain the device revision code.
Note 1: DEVID1 bit 4 is used to determine the device type (REV4 = `0`).
2: DEVID1 bit 4 is used to determine the device type (REV4 = `1`).

TABLE 5-2:   **DEVICE ID VALUES (CONTINUED)**

Device	Device ID Value	
	DEVID2	**DEVID1**
PIC18F4585	0Eh	`101x xxxx`
PIC18F4610	0Ch	`001x xxxx`
PIC18F4620	0Ch	`000x xxxx`
PIC18F4680	0Eh	`100x xxxx`
PIC18F4682	27h	`010x xxxx`
PIC18F4685	27h	`011x xxxx`

Legend: The 'x's in DEVID1 contain the device revision code.
Note 1:   DEVID1 bit 4 is used to determine the device type (REV4 = `0`).
      2:   DEVID1 bit 4 is used to determine the device type (REV4 = `1`).

PIC18F2XXX/4XXX FAMILY

TABLE 5-3: **PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)**

Bit Name	Configuration Words	Description
PLLDIV<2:0>	CONFIG1L	Oscillator Selection bits **(PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only)** Divider must be selected to provide a 4 MHz input into the 96 MHz PLL: 111 = Oscillator divided by 12 (48 MHz input) 110 = Oscillator divided by 10 (40 MHz input) 101 = Oscillator divided by 6 (24 MHz input) 100 = Oscillator divided by 5 (20 MHz input) 011 = Oscillator divided by 4 (16 MHz input) 010 = Oscillator divided by 3 (12 MHz input) 001 = Oscillator divided by 2 (8 MHz input) 000 = No divide – oscillator used directly (4 MHz input)
VREGEN	CONFIG2L	USB Voltage Regulator Enable bit **(PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only)** 1 = USB voltage regulator is enabled 0 = USB voltage regulator is disabled
BORV<1:0>	CONFIG2L	Brown-out Reset Voltage bits 11 = VBOR is set to 2.0V 10 = VBOR is set to 2.7V 01 = VBOR is set to 4.2V 00 = VBOR is set to 4.5V
BOREN<1:0>	CONFIG2L	Brown-out Reset Enable bits 11 = Brown-out Reset is enabled in hardware only (SBOREN is disabled) 10 = Brown-out Reset is enabled in hardware only and disabled in Sleep mode SBOREN is disabled) 01 = Brown-out Reset is enabled and controlled by software (SBOREN is enabled) 00 = Brown-out Reset is disabled in hardware and software
PWRTEN	CONFIG2L	Power-up Timer Enable bit 1 = PWRT is disabled 0 = PWRT is enabled
WDPS<3:0>	CONFIG2H	Watchdog Timer Postscaler Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

TABLE 5-3:   PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
WDTEN	CONFIG2H	Watchdog Timer Enable bit `1` = WDT is enabled `0` = WDT is disabled (control is placed on the SWDTEN bit)
MCLRE	CONFIG3H	$\overline{\text{MCLR}}$ Pin Enable bit `1` = $\overline{\text{MCLR}}$ pin is enabled, RE3 input pin is disabled `0` = RE3 input pin is enabled, $\overline{\text{MCLR}}$ pin is disabled
LPT1OSC	CONFIG3H	Low-Power Timer1 Oscillator Enable bit `1` = Timer1 is configured for low-power operation `0` = Timer1 is configured for high-power operation
PBADEN	CONFIG3H	PORTB A/D Enable bit `1` = PORTB A/D<4:0> pins are configured as analog input channels on Reset `0` = PORTB A/D<4:0> pins are configured as digital I/O on Reset
PBADEN	CONFIG3H	PORTB A/D Enable bit **(PIC18FXX8X devices only)** `1` = PORTB A/D<4:0> and PORTB A/D<1:0> pins are configured as analog input channels on Reset `0` = PORTB A/D<4:0> pins are configured as digital I/O on Reset
CCP2MX	CONFIG3H	CCP2 MUX bit `1` = CCP2 input/output is multiplexed with RC1[2] `0` = CCP2 input/output is multiplexed with RB3
$\overline{\text{DEBUG}}$	CONFIG4L	Background Debugger Enable bit `1` = Background debugger is disabled, RB6 and RB7 are configured as general purpose I/O pins `0` = Background debugger is enabled, RB6 and RB7 are dedicated to In-Circuit Debug
XINST	CONFIG4L	Extended Instruction Set Enable bit `1` = Instruction set extension and Indexed Addressing mode are enabled `0` = Instruction set extension and Indexed Addressing mode are disabled (Legacy mode)
ICPRT	CONFIG4L	Dedicated In-Circuit (ICD/ICSP™) Port Enable bit **(PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only)** `1` = ICPORT is enabled `0` = ICPORT is disabled
BBSIZ<1:0>[1]	CONFIG4L	Boot Block Size Select bits **(PIC18F2585/2680/4585/4680 devices only)** `11` = 4K words (8 Kbytes) Boot Block `10` = 4K words (8 Kbytes) Boot Block `01` = 2K words (4 Kbytes) Boot Block `00` = 1K word (2 Kbytes) Boot Block
BBSIZ<2:1>[1]	CONFIG4L	Boot Block Size Select bits **(PIC18F2682/2685/4582/4685 devices only)** `11` = 4K words (8 Kbytes) Boot Block `10` = 4K words (8 Kbytes) Boot Block `01` = 2K words (4 Kbytes) Boot Block `00` = 1K word (2 Kbytes) Boot Block

Note 1: The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

2: Not available in PIC18FXX8X and PIC18F2450/4450 devices.

5.6.3   ID LOCATIONS

Normally, the contents of these locations are defined by the user, but MPLAB® IDE provides the option of writing the device's unprotected 16-bit checksum in the 16 Most Significant bits of the ID locations (see MPLAB IDE Configure/ID Memory" menu). The lower 16 bits are not used and remain clear. This is the sum of all program memory contents and Configuration Words (appropriately masked) before any code protection is enabled.

If the user elects to define the contents of the ID locations, nothing about protected blocks can be known. If the user uses the preprotected checksum, provided by MPLAB IDE, an indirect characteristic of the programmed code is provided.

5.6.4   CODE PROTECTION

Blocks that are code-protected read back as all '0's and have no effect on checksum calculations. If any block is code-protected, then the contents of the ID locations are included in the checksum calculation.

All Configuration Words and the ID locations can always be read out normally, even when the device is fully code-protected. Checking the code protection settings in Configuration Words can direct which, if any, of the program memory blocks can be read, and if the ID locations should be used for checksum calculations.

TABLE 5-4: DEVICE BLOCK LOCATIONS AND SIZES (CONTINUED)

Device	Memory Size (Bytes)	Pins	Ending Address							Size (Bytes)			
			Boot Block	Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Boot Block	Block 0	Remaining Blocks	Device Total
PIC18F4455	24K	40	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F4458	24K	40	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F4480	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		
PIC18F4510	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F4515	48K	40	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F4520	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F4523	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F4525	48K	40	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F4550	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F4553	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F4580	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
			000FFF							4096	4096		
PIC18F4585	48K	40	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4610	64K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F4620	64K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F4680	64K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4682	80K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	—	2048	14336	65536	81920
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4685	96K	44	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	017FFF	2048	14336	81920	98304
			000FFF							4096	12288		
			001FFF							8192	8192		

Legend: — = unimplemented.

TABLE 5-5: **CONFIGURATION WORD MASKS FOR COMPUTING CHECKSUMS (CONTINUED)**

Device	Configuration Word (CONFIGxx)													
	1L	1H	2L	2H	3L	3H	4L	4H	5L	5H	6L	6H	7L	7H
	Address (30000xh)													
	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh
PIC18F4620	00	CF	1F	1F	00	87	C5	00	0F	C0	0F	E0	0F	40
PIC18F4680	00	CF	1F	1F	00	86	C5	00	0F	C0	0F	E0	0F	40
PIC18F4682	00	CF	1F	1F	00	86	C5	00	3F	C0	3F	E0	3F	40
PIC18F4685	00	CF	1F	1F	00	86	C5	00	3F	C0	3F	E0	3F	40

Legend: Shaded cells are unimplemented.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Sym	Characteristic	Min	Max	Units	Conditions
D110	VIHH	High-Voltage Programming Voltage on MCLR/VPP/RE3	VDD + 4.0	12.5	V	**(Note 2)**
D110A	VIHL	Low-Voltage Programming Voltage on MCLR/VPP/RE3	2.00	5.50	V	**(Note 2)**
D111	VDD	Supply Voltage During Programming	2.00	5.50	V	Externally timed, Row Erases and all writes
			3.0	5.50	V	Self-timed, Bulk Erases only **(Note 3)**
D112	IPP	Programming Current on MCLR/VPP/RE3	—	300	µA	**(Note 2)**
D113	IDDP	Supply Current During Programming	—	10	mA	
D031	VIL	Input Low Voltage	VSS	0.2 VDD	V	
D041	VIH	Input High Voltage	0.8 VDD	VDD	V	
D080	VOL	Output Low Voltage	—	0.6	V	IOL = 8.5 mA @ 4.5V
D090	VOH	Output High Voltage	VDD – 0.7	—	V	IOH = -3.0 mA @ 4.5V
D012	CIO	Capacitive Loading on I/O pin (PGD)	—	50	pF	To meet AC specifications
P1	TR	MCLR/VPP/RE3 Rise Time to Enter Program/Verify mode	—	1.0	µs	**(Notes 1, 2)**
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	VDD = 5.0V
			1	—	µs	VDD = 2.0V
P2A	TPGCL	Serial Clock (PGC) Low Time	40	—	ns	VDD = 5.0V
			400	—	ns	VDD = 2.0V
P2B	TPGCH	Serial Clock (PGC) High Time	40	—	ns	VDD = 5.0V
			400	—	ns	VDD = 2.0V
P3	TSET1	Input Data Setup Time to Serial Clock ↓	15	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	15	—	ns	
P5	TDLY1	Delay Between 4-Bit Command and Command Operand	40	—	ns	
P5A	TDLY1A	Delay Between 4-Bit Command Operand and Next 4-Bit Command	40	—	ns	
P6	TDLY2	Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	TDLY5	PGC High Time (minimum programming time)	1	—	ms	Externally timed
P10	TDLY6	PGC Low Time After Programming (high-voltage discharge time)	100	—	µs	
P11	TDLY7	Delay to Allow Self-Timed Data Write or Bulk Erase to Occur	5	—	ms	

Note 1: Do not allow excess time when transitioning MCLR between VIL and VIHH. This can cause spurious program executions to occur. The maximum transition time is:
    1 TCY + TPWRT (if enabled) + 1024 TOSC (for LP, HS, HS/PLL and XT modes only) +
    2 ms (for HS/PLL mode only) + 1.5 µs (for EC mode only)
where TCY is the instruction cycle time, TPWRT is the Power-up Timer period and TOSC is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.

2: When ICPRT = 1, this specification also applies to ICVPP.

3: At 0°C-50°C.