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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4515-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4515-i-ml</a>

# PIC18F2XXX/4XXX FAMILY

TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F2XXX/4XXX FAMILY

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
MCLR/VPP/RE3	VPP	P	Programming Enable
VDD <sup>(2)</sup>	VDD	P	Power Supply
VSS <sup>(2)</sup>	VSS	P	Ground
RB5	PGM	I	Low-Voltage ICSP™ Input when LVP Configuration bit equals '1' <sup>(1)</sup>
RB6	PGC	I	Serial Clock
RB7	PGD	I/O	Serial Data

**Legend:** I = Input, O = Output, P = Power  
**Note 1:** See Figure 5-1 for more information.  
**2:** All power supply (VDD) and ground (VSS) pins must be connected.

The following devices are included in 28-pin SPDIP, PDIP and SOIC parts:

- PIC18F2221
- PIC18F2321
- PIC18F2410
- PIC18F2420
- PIC18F2423
- PIC18F2450
- PIC18F2455
- PIC18F2458
- PIC18F2480
- PIC18F2510
- PIC18F2515
- PIC18F2520
- PIC18F2523
- PIC18F2525
- PIC18F2550
- PIC18F2553
- PIC18F2580
- PIC18F2585
- PIC18F2610
- PIC18F2620
- PIC18F2680
- PIC18F2682
- PIC18F2685

The following devices are included in 28-pin SSOP parts:

- PIC18F2221
- PIC18F2321

FIGURE 2-1: 28-Pin SPDIP, PDIP, SOIC,SSOP

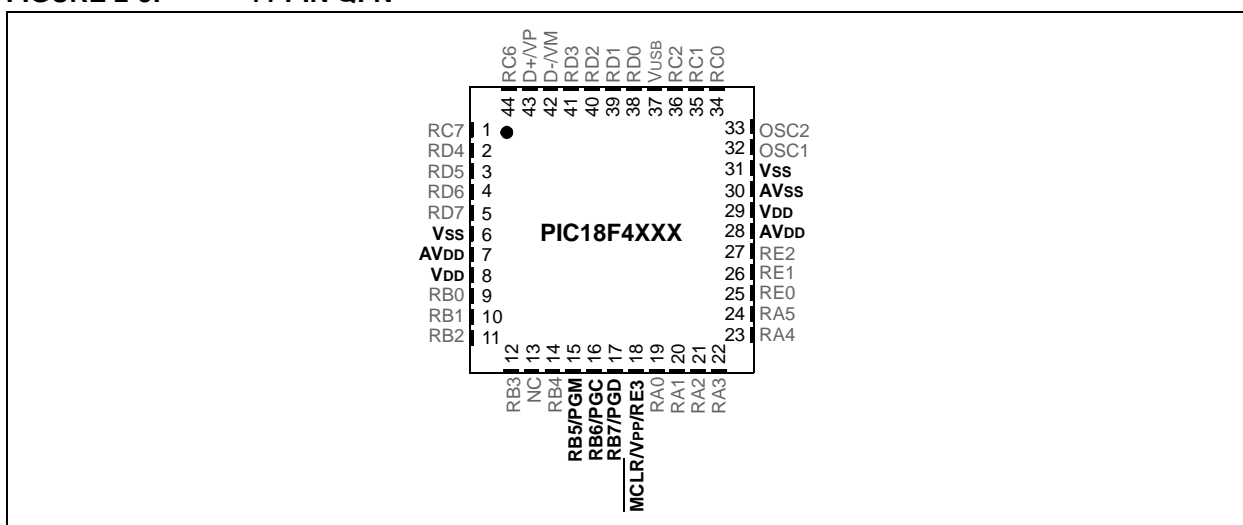


# PIC18F2XXX/4XXX FAMILY

The following devices are included in 44-pin QFN parts:

- PIC18F4221
- PIC18F4321
- PIC18F4410
- PIC18F4420
- PIC18F4423
- PIC18F4450
- PIC18F4455
- PIC18F4458
- PIC18F4480
- PIC18F4510
- PIC18F4520
- PIC18F4515
- PIC18F4523
- PIC18F4525
- PIC18F4550
- PIC18F4553
- PIC18F4580
- PIC18F4585
- PIC18F4610
- PIC18F4620
- PIC18F4680
- PIC18F4682
- PIC18F4685

**FIGURE 2-5: 44-PIN QFN**



## 2.3 Memory Maps

For PIC18FX6X0 devices, the code memory space extends from 0000h to 0FFFFh (64 Kbytes) in four 16-Kbyte blocks. For PIC18FX5X5 devices, the code memory space extends from 0000h to 0BFFFFh (48 Kbytes) in three 16-Kbyte blocks. Addresses, 0000h through 07FFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

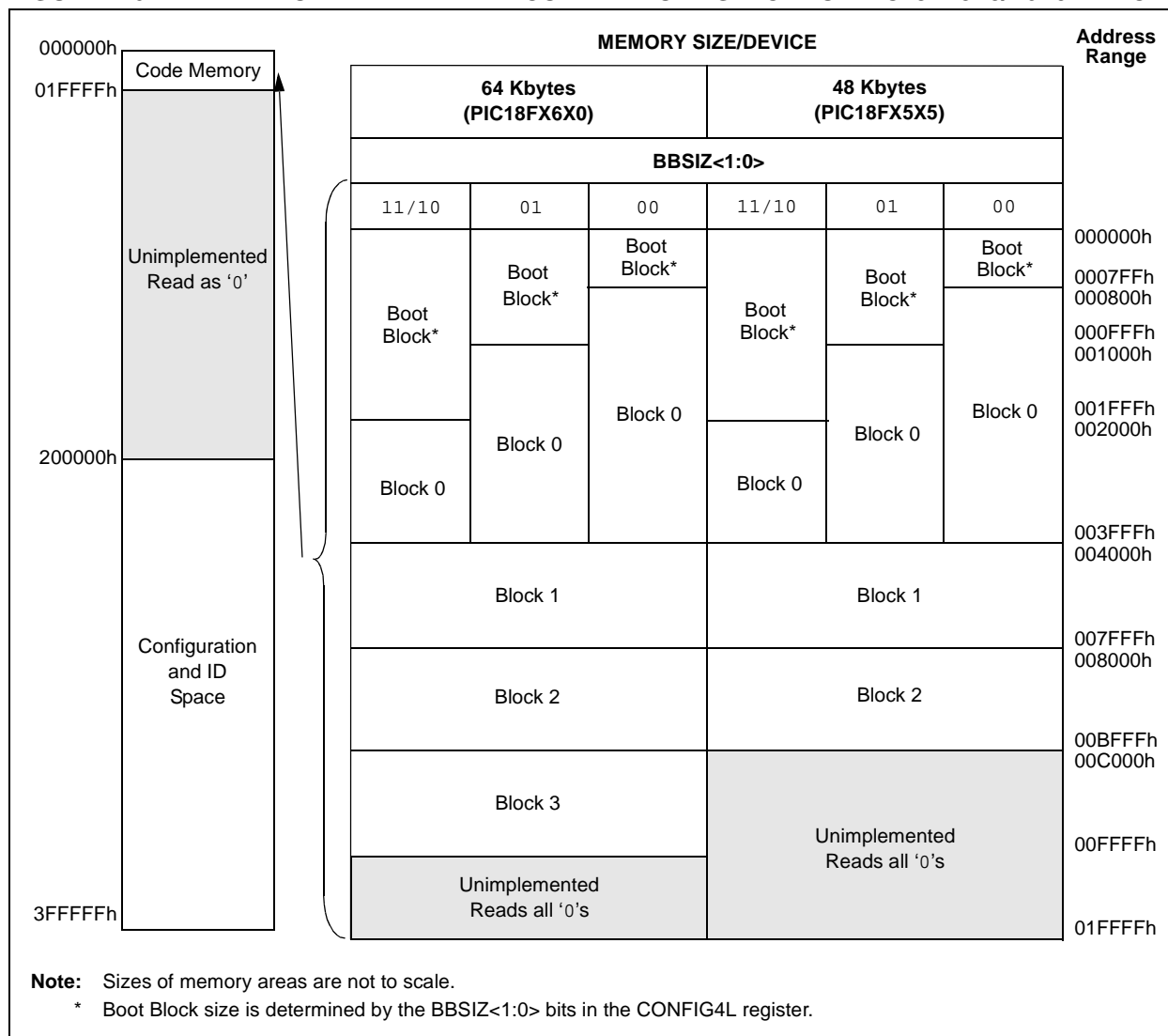
The size of the Boot Block in PIC18F2585/2680/4585/4680 devices can be configured as 1, 2 or 4K words (see [Figure 2-6](#)). This is done through the BBSIZ<1:0> bits in the Configuration register, CONFIG4L. It is important to note that increasing the size of the Boot Block decreases the size of Block 0.

# PIC18F2XXX/4XXX FAMILY

**TABLE 2-2: IMPLEMENTATION OF CODE MEMORY**

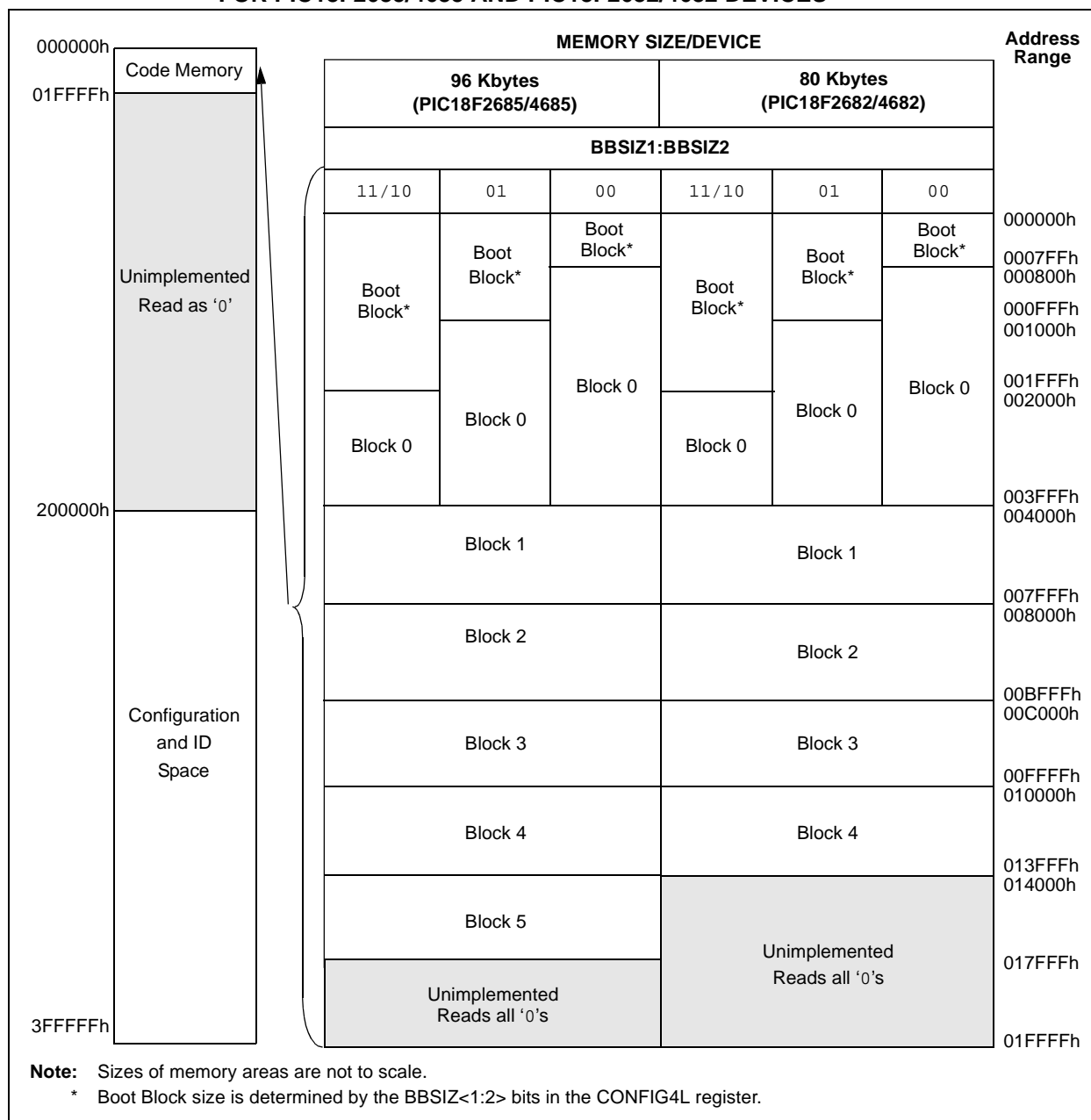
Device	Code Memory Size (Bytes)
PIC18F2515	000000h-00BFFFh (48K)
PIC18F2525	
PIC18F2585	
PIC18F4515	
PIC18F4525	
PIC18F4585	
PIC18F2610	000000h-00FFFFh (64K)
PIC18F2620	
PIC18F2680	
PIC18F4610	
PIC18F4620	
PIC18F4680	

**FIGURE 2-6: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX5X5/X6X0 DEVICES**



# PIC18F2XXX/4XXX FAMILY

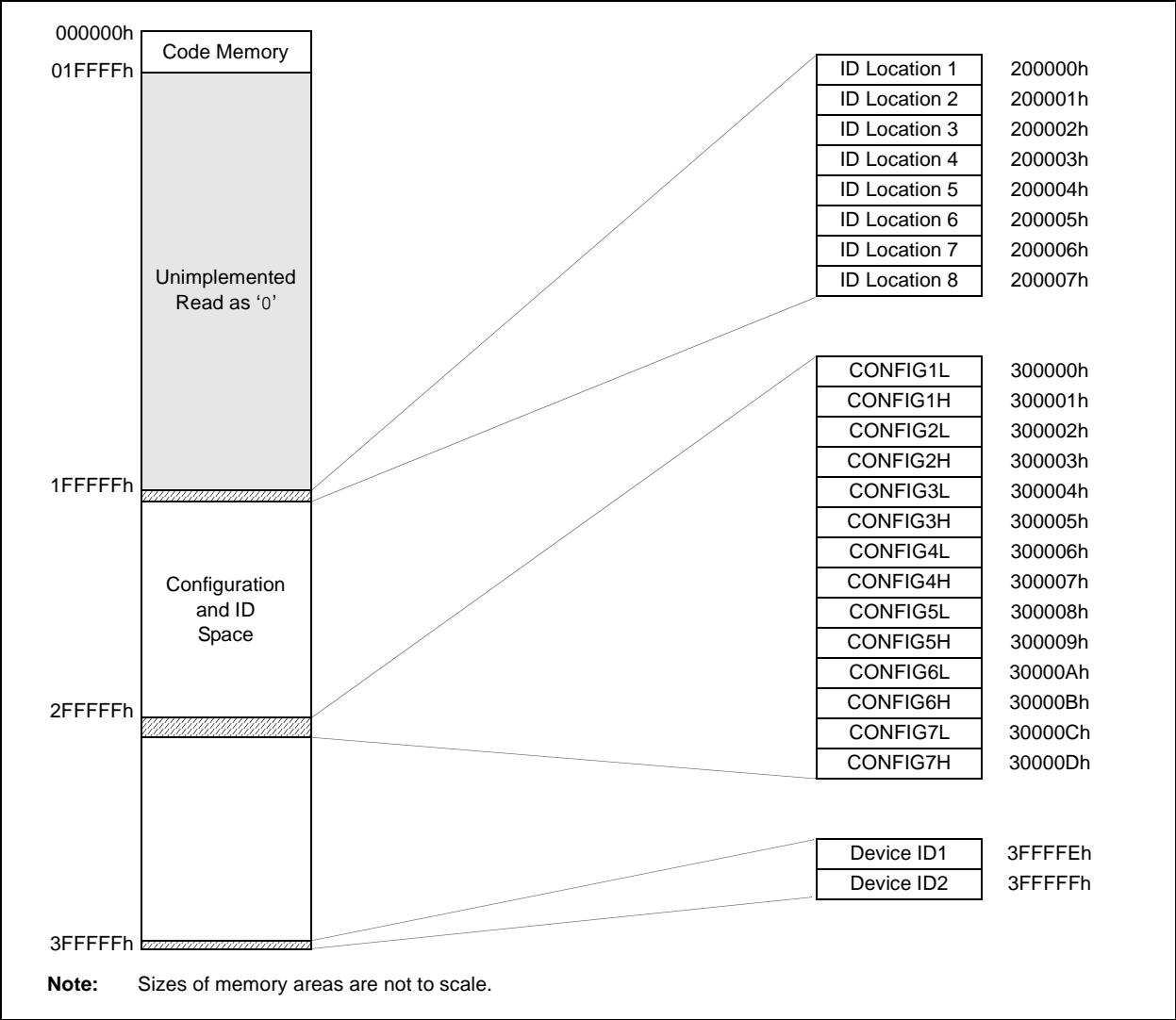
**FIGURE 2-7: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18F2685/4685 AND PIC18F2682/4682 DEVICES**



For PIC18FX5X0/X5X3 devices, the code memory space extends from 000000h to 007FFFh (32 Kbytes) in four 8-Kbyte blocks. For PIC18FX4X5/X4X8 devices, the code memory space extends from 000000h to 005FFFh (24 Kbytes) in three 8-Kbyte blocks. Addresses, 000000h through 0007FFFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

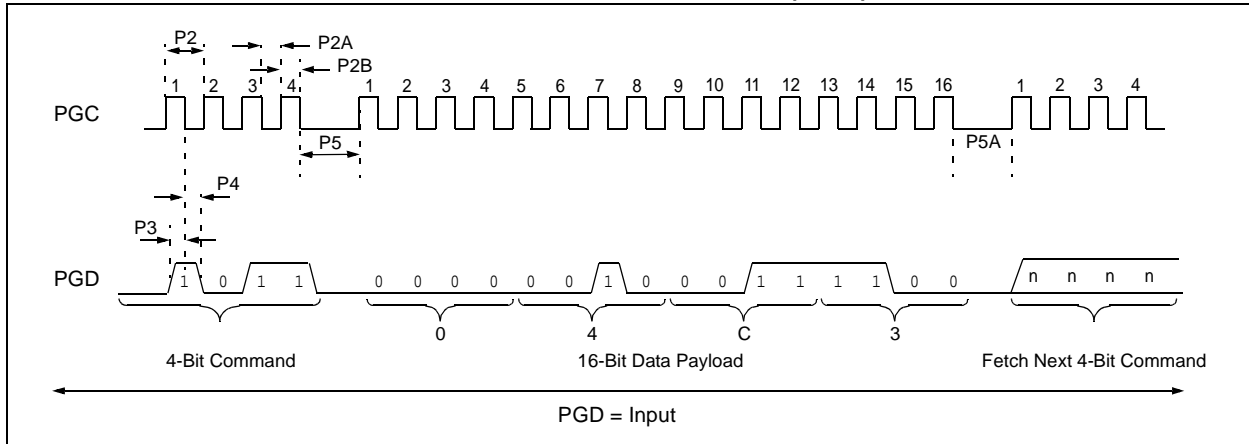
# PIC18F2XXX/4XXX FAMILY

FIGURE 2-12: CONFIGURATION AND ID LOCATIONS FOR PIC18F2XXX/4XXX FAMILY DEVICES



# PIC18F2XXX/4XXX FAMILY

**FIGURE 2-18: TABLE WRITE, POST-INCREMENT TIMING (1101)**



## 2.8 Dedicated ICSP/ICD Port (44-Pin TQFP Only)

The PIC18F4455/4458/4550/4553 44-pin TQFP devices are designed to support an alternate programming input: the dedicated ICSP/ICD port. The primary purpose of this port is to provide an alternate In-Circuit Debugging (ICD) option and free the pins (RB6, RB7 and MCLR) that would normally be used for debugging the application. In conjunction with ICD capability, however, the dedicated ICSP/ICD port also provides an alternate port for ICSP.

Setting the ICPRT Configuration bit enables the dedicated ICSP/ICD port. The dedicated ICSP/ICD port functions the same as the default ICSP/ICD port; however, alternate pins are used instead of the default pins. Table 2-10 identifies the functionally equivalent pins for ICSP purposes:

The dedicated ICSP/ICD port is an alternate port. Thus, ICSP is still available through the default port even though the ICPRT Configuration bit is set. When the  $V_{IH}$  is seen on the MCLR/VPP/RE3 pin prior to applying  $V_{IH}$  to the ICRST/ICVPP pin, then the state of the ICRST/ICVPP pin is ignored. Likewise, when the  $V_{IH}$  is seen on ICRST/ICVPP prior to applying  $V_{IH}$  to MCLR/VPP/RE3, then the state of the MCLR/VPP/RE3 pin is ignored.

**Note:** The ICPRT Configuration bit can only be programmed through the default ICSP port. Chip Erase functions through the dedicated ICSP/ICD port do not affect this bit.

When the ICPRT Configuration bit is set (dedicated ICSP/ICD port enabled), the NC/ICPORTS pin must be tied to either VDD or VSS.

The ICPRT Configuration bit must be maintained clear for all 28-pin and 40-pin devices; otherwise, unexpected operation may occur.

**TABLE 2-10: ICSP™ EQUIVALENT PINS**

Pin Name	During Programming			
	Pin Name	Pin Type	Dedicated Pins	Pin Description
MCLR/VPP/RE3	VPP	P	NC/ICRST/ICVPP	Programming Enable
RB6	PGC	I	NC/ICCK/ICPGC	Serial Clock
RB7	PGD	I/O	NC/ICDT/ICPGD	Serial Data

**Legend:** I = Input, O = Output, P = Power

# PIC18F2XXX/4XXX FAMILY

## 3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the various memory regions within the device.

In all cases, except high-voltage ICSP Bulk Erase, the EECON1 register must be configured in order to operate on a particular memory region.

When using the EECON1 register to act on code memory, the EEPGD bit must be set (EECON1<7> = 1) and the CFGS bit must be cleared (EECON1<6> = 0). The WREN bit must be set (EECON1<2> = 1) to enable writes of any sort (e.g., erases) and this must be done prior to initiating a write sequence. The FREE bit must be set (EECON1<4> = 1) in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit (EECON1<1> = 1). It is strongly recommended that the WREN bit only be set immediately prior to a program erase.

### 3.1 ICSP Erase

#### 3.1.1 HIGH-VOLTAGE ICSP BULK ERASE

Erasing code or data EEPROM is accomplished by configuring two Bulk Erase Control registers located at 3C0004h and 3C0005h. Code memory may be erased, portions at a time, or the user may erase the entire device in one action. Bulk Erase operations will also clear any code-protect settings associated with the memory block being erased. Erase options are detailed in [Table 3-1](#). If data EEPROM is code-protected (CPD = 0), the user must request an erase of data EEPROM (e.g., 0084h as shown in [Table 3-1](#)).

**TABLE 3-1: BULK ERASE OPTIONS**

Description	Data (3C0005h:3C0004h)
Chip Erase	3F8Fh
Erase Data EEPROM <sup>(1)</sup>	0084h
Erase Boot Block	0081h
Erase Configuration Bits	0082h
Erase Code EEPROM Block 0	0180h
Erase Code EEPROM Block 1	0280h
Erase Code EEPROM Block 2	0480h
Erase Code EEPROM Block 3	0880h
Erase Code EEPROM Block 4	1080h
Erase Code EEPROM Block 5	2080h

**Note 1:** Selected devices only, see [Section 3.3 “Data EEPROM Programming”](#).

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the NOP command), serial execution will cease until the erase completes (Parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

The code sequence to erase the entire device is shown in [Table](#) and the flowchart is shown in [Figure 3-1](#).

**Note:** A Bulk Erase is the only way to reprogram code-protect bits from an ON state to an OFF state.

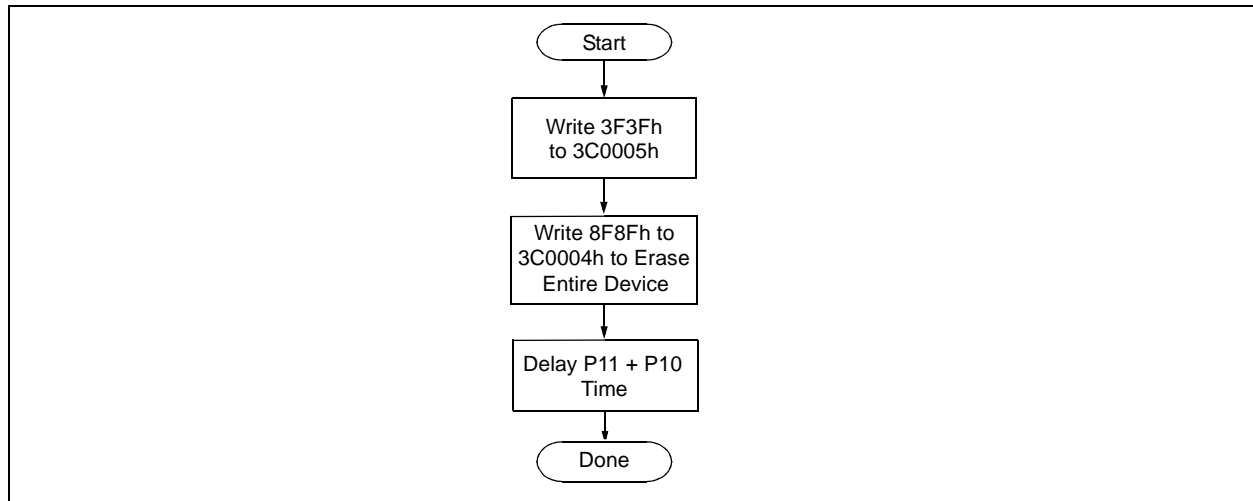


# PIC18F2XXX/4XXX FAMILY

**TABLE 3-2: BULK ERASE COMMAND SEQUENCE**

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	3F 3F	Write 3F3Fh to 3C0005h
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	8F 8F	Write 8F8Fh TO 3C0004h to erase entire device. NOP Hold PGD low until erase completes.
0000	00 00	
0000	00 00	

**FIGURE 3-1: BULK ERASE FLOW**



# PIC18F2XXX/4XXX FAMILY

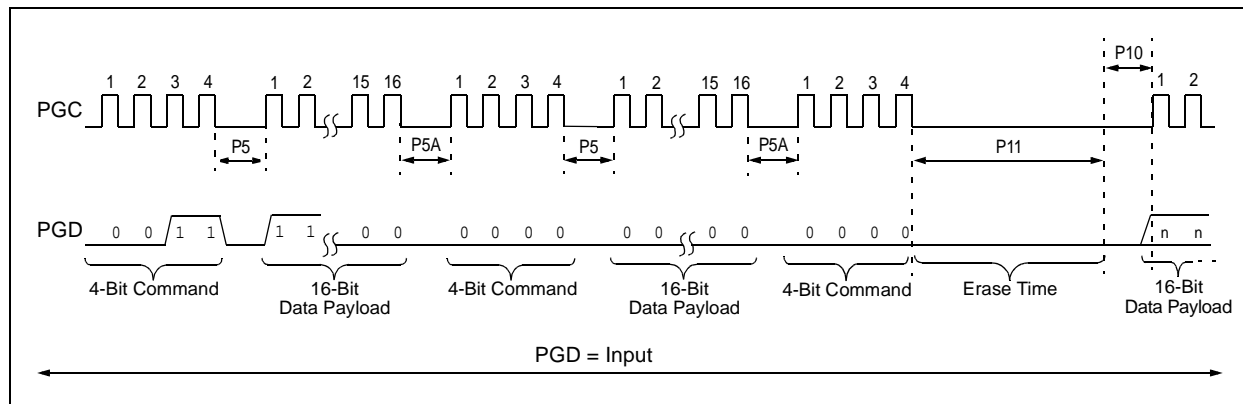
## 3.1.2 LOW-VOLTAGE ICSP BULK ERASE

When using low-voltage ICSP, the part must be supplied by the voltage specified in Parameter D111 if a Bulk Erase is to be executed. All other Bulk Erase details, as described above, apply.

If it is determined that a program memory erase must be performed at a supply voltage below the Bulk Erase limit, refer to the erase methodology described in [Section 3.1.3 “ICSP Row Erase”](#) and [Section 3.2.1 “Modifying Code Memory”](#).

If it is determined that a data EEPROM erase (selected devices only, see [Section 3.3 “Data EEPROM Programming”](#)) must be performed at a supply voltage below the Bulk Erase limit, follow the methodology described in [Section 3.3 “Data EEPROM Programming”](#) and write ‘1’s to the array.

**FIGURE 3-2: BULK ERASE TIMING**



## 3.1.3 ICSP ROW ERASE

Regardless of whether high or low-voltage ICSP is used, it is possible to erase one row (64 bytes of data), provided the block is not code or write-protected. Rows are located at static boundaries, beginning at program memory address, 000000h, extending to the internal program memory limit (see [Section 2.3 “Memory Maps”](#)).

The Row Erase duration is externally timed and is controlled by PGC. After the WR bit in EECON1 is set, a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by Parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to Row Erase a PIC18F2XXX/4XXX Family device is shown in [Table 3-3](#). The flowchart, shown in [Figure 3-3](#), depicts the logic necessary to completely erase a PIC18F2XXX/4XXX Family device. The timing diagram that details the Start Programming command and Parameters P9 and P10 is shown in [Figure 3-5](#).

**Note:** The TBLPTR register can point to any byte within the row intended for erase.

# PIC18F2XXX/4XXX FAMILY

## 3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write and erase buffer sizes, shown in [Table 3-4](#), can be mapped to any location of the same size, beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the proper amount of code memory that contains the Table Pointer.

The programming duration is externally timed and is controlled by PGC. After a Start Programming command is issued (4-bit command, '1111'), a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by Parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to program a PIC18F2XXX/4XXX Family device is shown in [Table 3-5](#). The flowchart, shown in [Figure 3-4](#), depicts the logic necessary to completely write a PIC18F2XXX/4XXX Family device. The timing diagram that details the Start Programming command and Parameters P9 and P10 is shown in [Figure 3-5](#).

**Note:** The TBLPTR register must point to the same region when initiating the programming sequence as it did when the write buffers were loaded.

**TABLE 3-4: WRITE AND ERASE BUFFER SIZES**

Devices (Arranged by Family)	Write Buffer Size (Bytes)	Erase Buffer Size (Bytes)
PIC18F2221, PIC18F2321, PIC18F4221, PIC18F4321	8	64
PIC18F2450, PIC18F4450	16	64
PIC18F2410, PIC18F2510, PIC18F4410, PIC18F4510	32	64
PIC18F2420, PIC18F2520, PIC18F4420, PIC18F4520		
PIC18F2423, PIC18F2523, PIC18F4423, PIC18F4523		
PIC18F2480, PIC18F2580, PIC18F4480, PIC18F4580		
PIC18F2455, PIC18F2550, PIC18F4455, PIC18F4550		
PIC18F2458, PIC18F2553, PIC18F4458, PIC18F4553		
PIC18F2515, PIC18F2610, PIC18F4515, PIC18F4610	64	64
PIC18F2525, PIC18F2620, PIC18F4525, PIC18F4620		
PIC18F2585, PIC18F2680, PIC18F4585, PIC18F4680		
PIC18F2682, PIC18F2685, PIC18F4682, PIC18F4685		

# PIC18F2XXX/4XXX FAMILY

FIGURE 3-4: PROGRAM CODE MEMORY FLOW

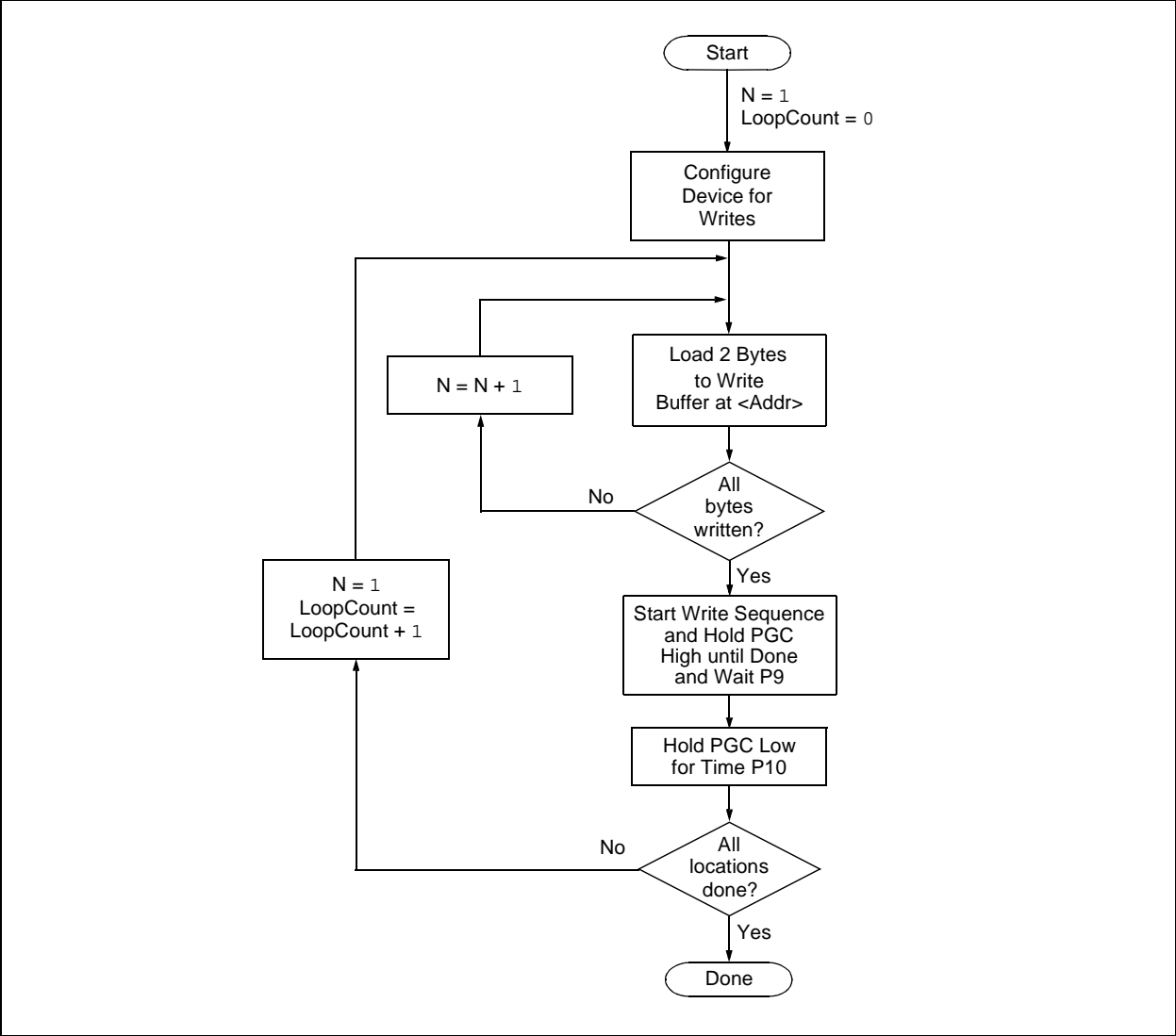
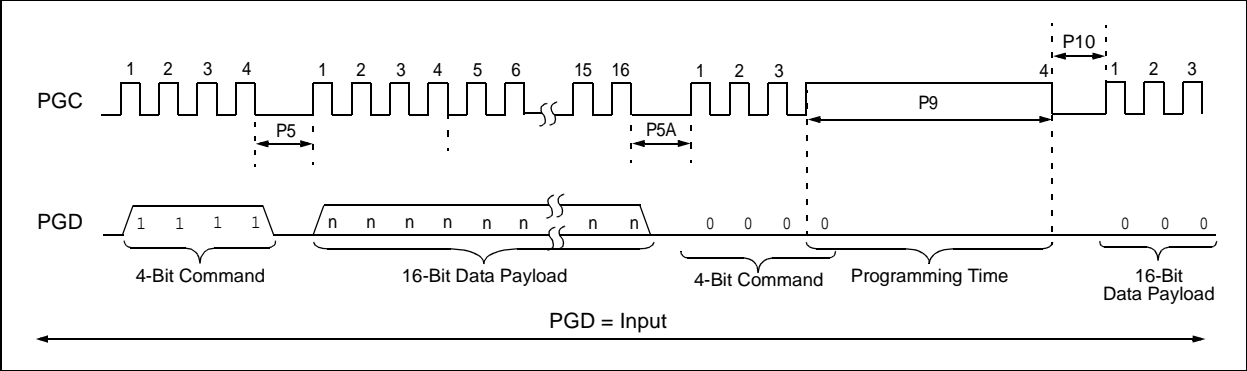
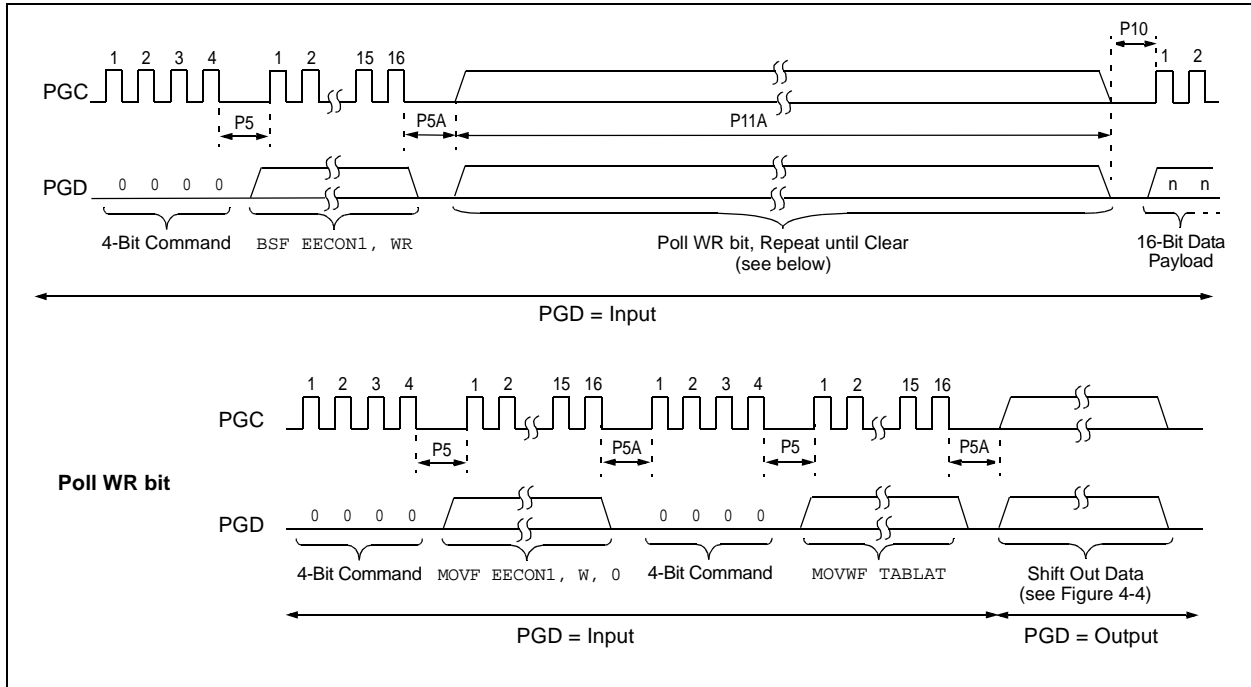


FIGURE 3-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



# PIC18F2XXX/4XXX FAMILY

**FIGURE 3-7: DATA EEPROM WRITE TIMING**



# PIC18F2XXX/4XXX FAMILY

**TABLE 3-7: PROGRAMMING DATA MEMORY**

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to data EEPROM.		
0000	9E A6	BCF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Set the data EEPROM Address Pointer.		
0000	0E <Addr>	MOVLW <Addr>
0000	6E A9	MOVWF EEADR
0000	0E <AddrH>	MOVLW <AddrH>
0000	6E AA	MOVWF EEADRH
Step 3: Load the data to be written.		
0000	0E <Data>	MOVLW <Data>
0000	6E A8	MOVWF EEDATA
Step 4: Enable memory writes.		
0000	84 A6	BSF EECON1, WREN
Step 5: Initiate write.		
0000	82 A6	BSF EECON1, WR
Step 6: Poll WR bit, repeat until the bit is clear.		
0000	50 A6	MOVF EECON1, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0010	<MSB><LSB>	Shift out data <sup>(1)</sup>
Step 7: Hold PGC low for time P10.		
Step 8: Disable writes.		
0000	94 A6	BCF EECON1, WREN
Repeat Steps 2 through 8 to write more data.		

**Note 1:** See [Figure 4-4](#) for details on shift out data timing.

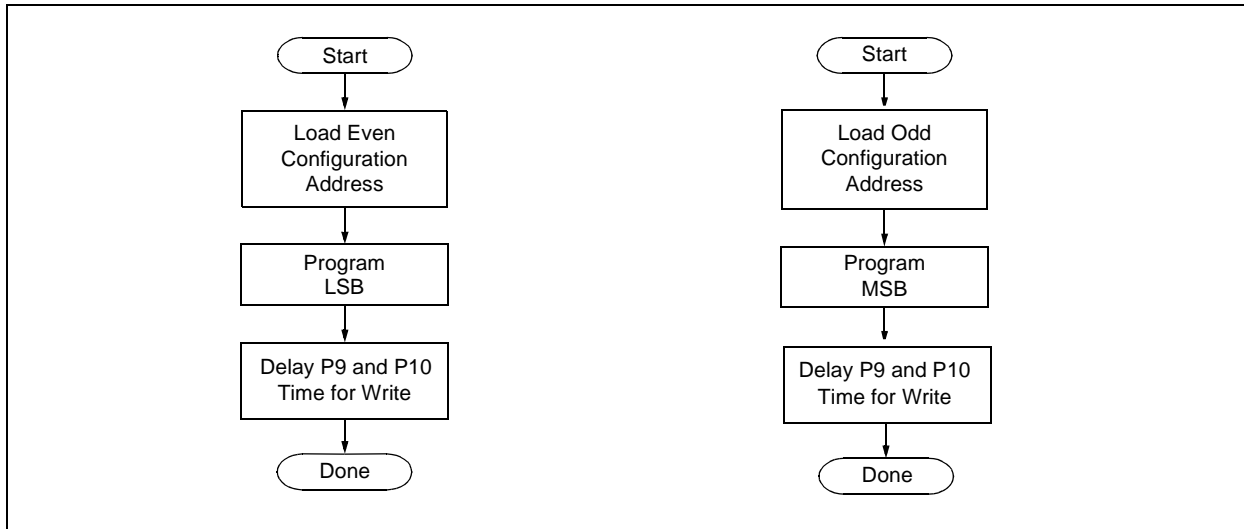
# PIC18F2XXX/4XXX FAMILY

**TABLE 3-9: SET ADDRESS POINTER TO CONFIGURATION LOCATION**

4-Bit Command	Data Payload	Core Instruction
Step 1: Enable writes and direct access to configuration memory.		
0000	8E A6	BSF EECON1, EEPGD
0000	8C A6	BSF EECON1, CFGS
Step 2: Set Table Pointer for configuration byte to be written. Write even/odd addresses. <sup>(1)</sup>		
0000	0E 30	MOVLW 30h
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPRTH
0000	0E 00	MOVLW 00h
0000	6E F6	MOVWF TBLPTRL
1111	<MSB ignored><LSB>	Load 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
0000	0E 01	MOVLW 01h
0000	6E F6	MOVWF TBLPTRL
1111	<MSB><LSB ignored>	Load 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.

**Note 1:** Enabling the write protection of Configuration bits (WRTC = 0 in CONFIG6H) will prevent further writing of the Configuration bits. Always write all the Configuration bits before enabling the write protection for Configuration bits.

**FIGURE 3-8: CONFIGURATION PROGRAMMING FLOW**



## 4.0 READING THE DEVICE

### 4.1 Read Code Memory, ID Locations and Configuration Bits

Code memory is accessed, one byte at a time, via the 4-bit command, '1001' (Table Read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

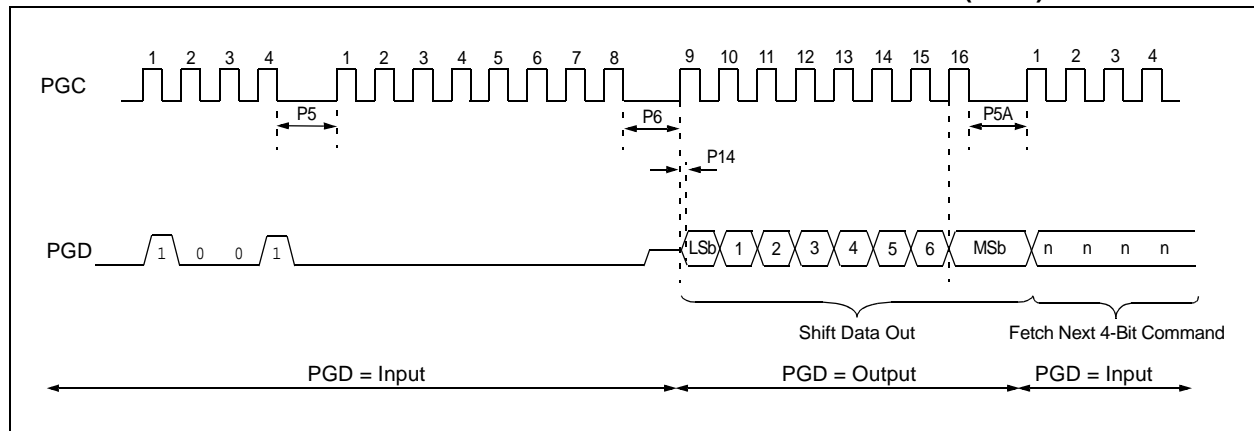
The 4-bit command is shifted in, LSb first. The read is executed during the next eight clocks, then shifted out on PGD during the last eight clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see [Figure 4-1](#)). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFFh address space, so it also applies to the reading of the ID and Configuration registers.

**TABLE 4-1: READ CODE MEMORY SEQUENCE**

4-Bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

**FIGURE 4-1: TABLE READ POST-INCREMENT INSTRUCTION TIMING (1001)**





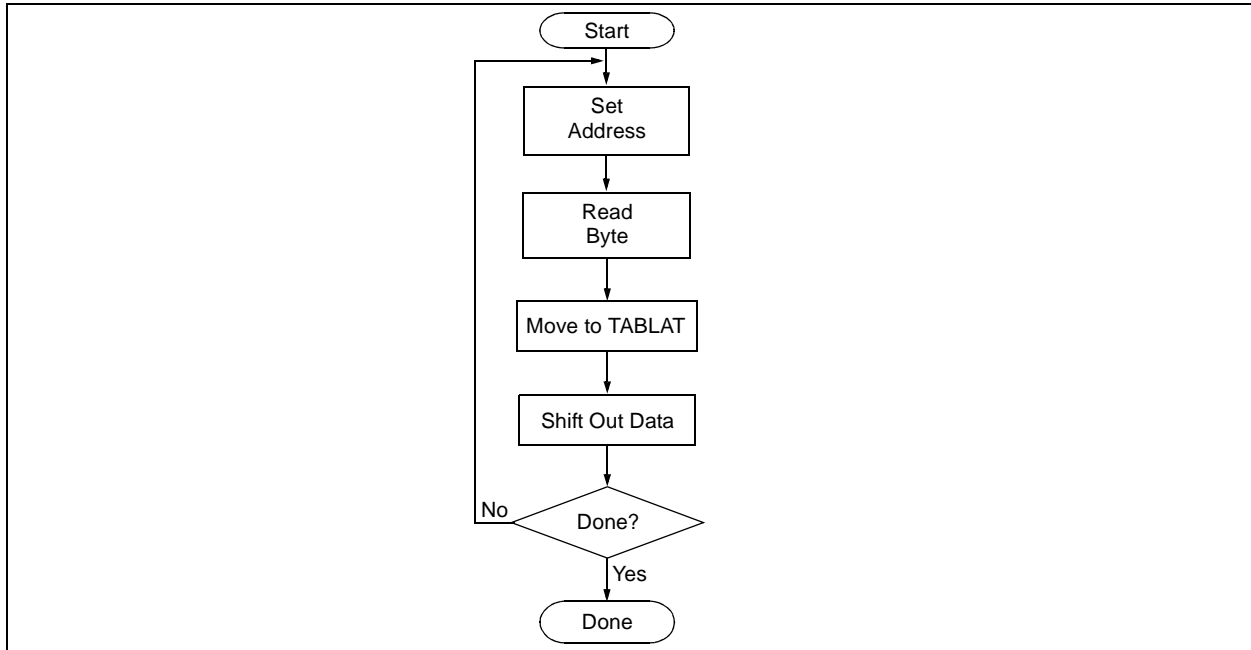
# PIC18F2XXX/4XXX FAMILY

## 4.4 Read Data EEPROM Memory

Data EEPROM is accessed, one byte at a time, via an Address Pointer (register pair: EEADRH:EEADR) and a data latch (EEDATA). Data EEPROM is read by loading EEADRH:EEADR with the desired memory location and initiating a memory read by appropriately configuring the EECON1 register. The data will be loaded into EEDATA, where it may be serially output on PGD via the 4-bit command, '0010' (Shift Out Data Holding register). A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see [Figure 4-4](#)).

The command sequence to read a single byte of data is shown in [Table 4-2](#).

**FIGURE 4-3: READ DATA EEPROM FLOW**



**TABLE 4-2: READ DATA EEPROM MEMORY**

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to data EEPROM.		
0000	9E A6	BCF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Set the data EEPROM Address Pointer.		
0000	0E <Addr>	MOVLW <Addr>
0000	6E A9	MOVWF EEADR
0000	0E <AddrH>	MOVLW <AddrH>
0000	6E AA	MOVWF EEADRH
Step 3: Initiate a memory read.		
0000	80 A6	BSF EECON1, RD
Step 4: Load data into the Serial Data Holding register.		
0000	50 A8	MOVF EEDATA, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0010	<MSB><LSB>	Shift Out Data <sup>(1)</sup>

**Note 1:** The <LSB> is undefined. The <MSB> is the data.

# PIC18F2XXX/4XXX FAMILY

**TABLE 5-2: DEVICE ID VALUES**

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F2221	21h	011x xxxx
PIC18F2321	21h	001x xxxx
PIC18F2410	11h	011x xxxx
PIC18F2420	11h	010x xxxx <sup>(1)</sup>
PIC18F2423	11h	010x xxxx <sup>(2)</sup>
PIC18F2450	24h	001x xxxx
PIC18F2455	12h	011x xxxx
PIC18F2458	2Ah	011x xxxx
PIC18F2480	1Ah	111x xxxx
PIC18F2510	11h	001x xxxx
PIC18F2515	0Ch	111x xxxx
PIC18F2520	11h	000x xxxx <sup>(1)</sup>
PIC18F2523	11h	000x xxxx <sup>(2)</sup>
PIC18F2525	0Ch	110x xxxx
PIC18F2550	12h	010x xxxx
PIC18F2553	2Ah	010x xxxx
PIC18F2580	1Ah	110x xxxx
PIC18F2585	0Eh	111x xxxx
PIC18F2610	0Ch	101x xxxx
PIC18F2620	0Ch	100x xxxx
PIC18F2680	0Eh	110x xxxx
PIC18F2682	27h	000x xxxx
PIC18F2685	27h	001x xxxx
PIC18F4221	21h	010x xxxx
PIC18F4321	21h	000x xxxx
PIC18F4410	10h	111x xxxx
PIC18F4420	10h	110x xxxx <sup>(1)</sup>
PIC18F4423	10h	110x xxxx <sup>(2)</sup>
PIC18F4450	24h	000x xxxx
PIC18F4455	12h	001x xxxx
PIC18F4458	2Ah	001x xxxx
PIC18F4480	1Ah	101x xxxx
PIC18F4510	10h	101x xxxx
PIC18F4515	0Ch	011x xxxx
PIC18F4520	10h	100x xxxx <sup>(1)</sup>
PIC18F4523	10h	100x xxxx <sup>(2)</sup>
PIC18F4525	0Ch	010x xxxx
PIC18F4550	12h	000x xxxx
PIC18F4553	2Ah	000x xxxx
PIC18F4580	1Ah	100x xxxx

**Legend:** The 'x's in DEVID1 contain the device revision code.

**Note 1:** DEVID1 bit 4 is used to determine the device type (REV4 = 0).

**2:** DEVID1 bit 4 is used to determine the device type (REV4 = 1).

# PIC18F2XXX/4XXX FAMILY

**TABLE 5-3: PIC18F2XXX/4XXX FAMILY BIT DESCRIPTIONS (CONTINUED)**

Bit Name	Configuration Words	Description
PLLDIV<2:0>	CONFIG1L	Oscillator Selection bits ( <b>PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only</b> ) Divider must be selected to provide a 4 MHz input into the 96 MHz PLL: 111 = Oscillator divided by 12 (48 MHz input) 110 = Oscillator divided by 10 (40 MHz input) 101 = Oscillator divided by 6 (24 MHz input) 100 = Oscillator divided by 5 (20 MHz input) 011 = Oscillator divided by 4 (16 MHz input) 010 = Oscillator divided by 3 (12 MHz input) 001 = Oscillator divided by 2 (8 MHz input) 000 = No divide – oscillator used directly (4 MHz input)
VREGEN	CONFIG2L	USB Voltage Regulator Enable bit ( <b>PIC18F2455/2550/4455/4550, PIC18F2458/2553/4458/4553 and PIC18F2450/4450 devices only</b> ) 1 = USB voltage regulator is enabled 0 = USB voltage regulator is disabled
BORV<1:0>	CONFIG2L	Brown-out Reset Voltage bits 11 = VBOR is set to 2.0V 10 = VBOR is set to 2.7V 01 = VBOR is set to 4.2V 00 = VBOR is set to 4.5V
BOREN<1:0>	CONFIG2L	Brown-out Reset Enable bits 11 = Brown-out Reset is enabled in hardware only (SBOREN is disabled) 10 = Brown-out Reset is enabled in hardware only and disabled in Sleep mode (SBOREN is disabled) 01 = Brown-out Reset is enabled and controlled by software (SBOREN is enabled) 00 = Brown-out Reset is disabled in hardware and software
PWRTEN	CONFIG2L	Power-up Timer Enable bit 1 = PWRT is disabled 0 = PWRT is enabled
WDPS<3:0>	CONFIG2H	Watchdog Timer Postscaler Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1

**Note 1:** The BBSIZ bits, BBSIZ<1:0> and BBSIZ<2:1> bits, cannot be changed once any of the following code-protect bits are enabled: CPB or CP0, WRTB or WRT0, EBTRB or EBTR0.

**2:** Not available in PIC18FXX8X and PIC18F2450/4450 devices.

# PIC18F2XXX/4XXX FAMILY

**TABLE 5-4: DEVICE BLOCK LOCATIONS AND SIZES (CONTINUED)**

Device	Memory Size (Bytes)	Pins	Ending Address							Size (Bytes)			
			Boot Block	Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Boot Block	Block 0	Remaining Blocks	Device Total
PIC18F4455	24K	40	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F4458	24K	40	0007FF	001FFF	003FFF	005FFF	—	—	—	2048	6144	16384	24576
PIC18F4480	16K	40	0007FF	001FFF	003FFF	—	—	—	—	2048	6144	8192	16384
			000FFF							4096	4096		
PIC18F4510	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F4515	48K	40	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F4520	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F4523	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	14336	16384	32768
PIC18F4525	48K	40	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
PIC18F4550	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F4553	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
PIC18F4580	32K	40	0007FF	001FFF	003FFF	005FFF	007FFF	—	—	2048	6144	24576	32768
			000FFF							4096	4096		
PIC18F4585	48K	40	0007FF	003FFF	007FFF	00BFFF	—	—	—	2048	14336	32768	49152
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4610	64K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F4620	64K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
PIC18F4680	64K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	—	—	2048	14336	49152	65536
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4682	80K	40	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	—	2048	14336	65536	81920
			000FFF							4096	12288		
			001FFF							8192	8192		
PIC18F4685	96K	44	0007FF	003FFF	007FFF	00BFFF	00FFFF	013FFF	017FFF	2048	14336	81920	98304
			000FFF							4096	12288		
			001FFF							8192	8192		

**Legend:** — = unimplemented.

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