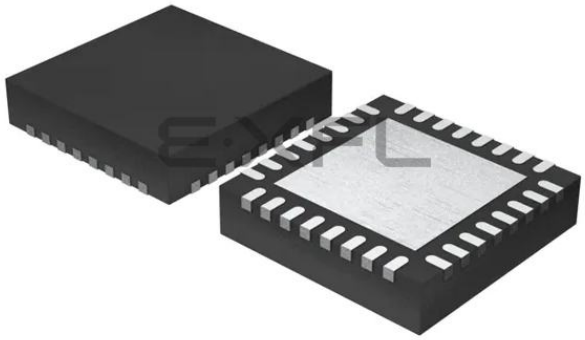

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32zg210f16-qfn32

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		115	132	µA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		117	136	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		114	128	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		116	132	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		117	131	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		118	133	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		118	133	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		120	135	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		124	139	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		125	142	µA/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		155	177	µA/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		162	181	µA/ MHz
I_{EM1}	EM1 current (Production test condition = 14 MHz)	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		48	57	µA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		49	59	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		48	52	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		49	53	µA/ MHz

Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

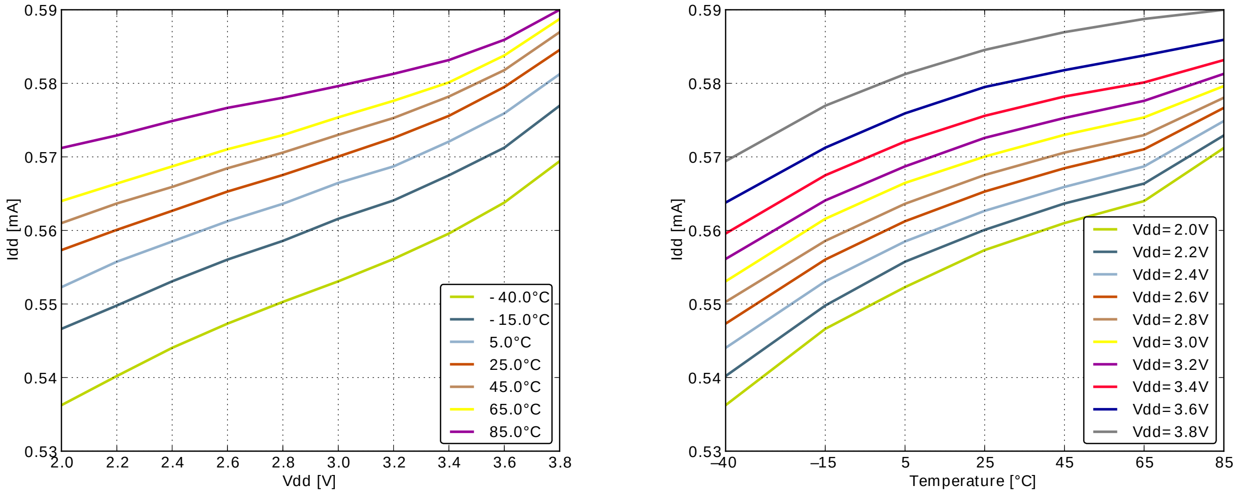


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz

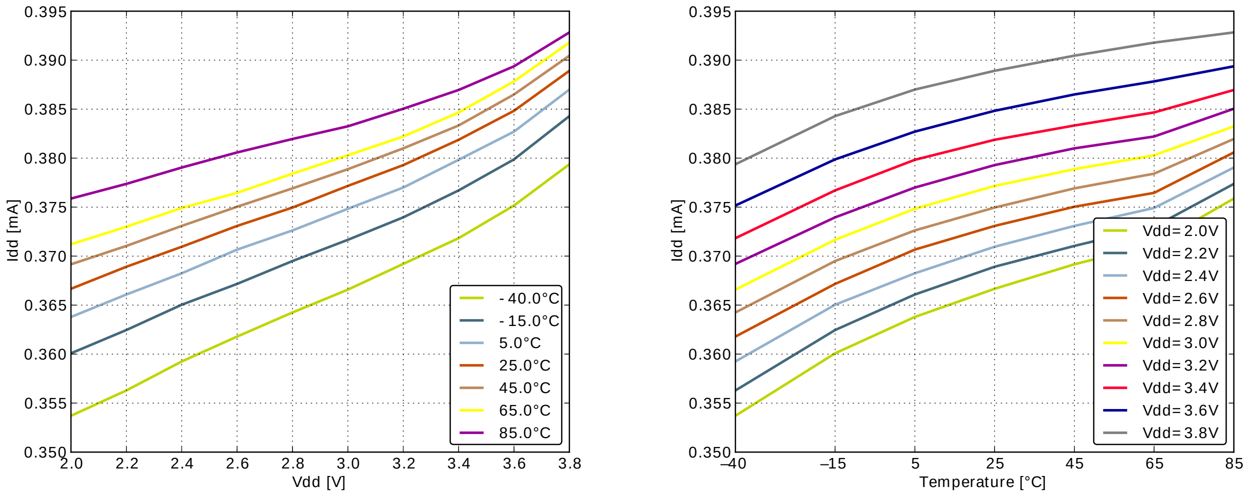
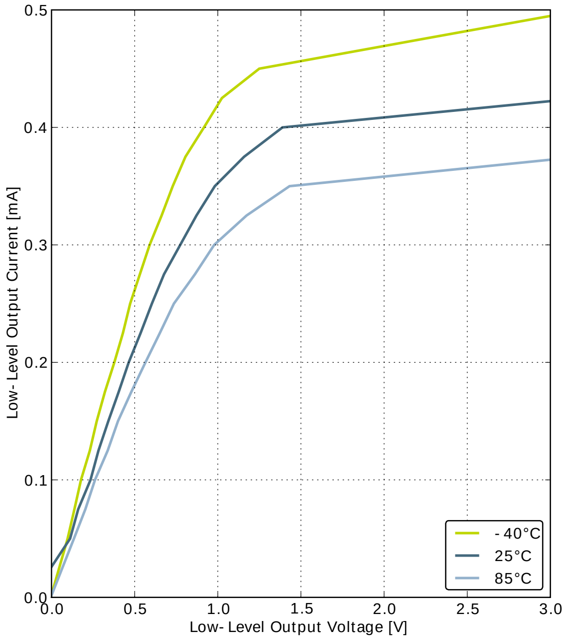
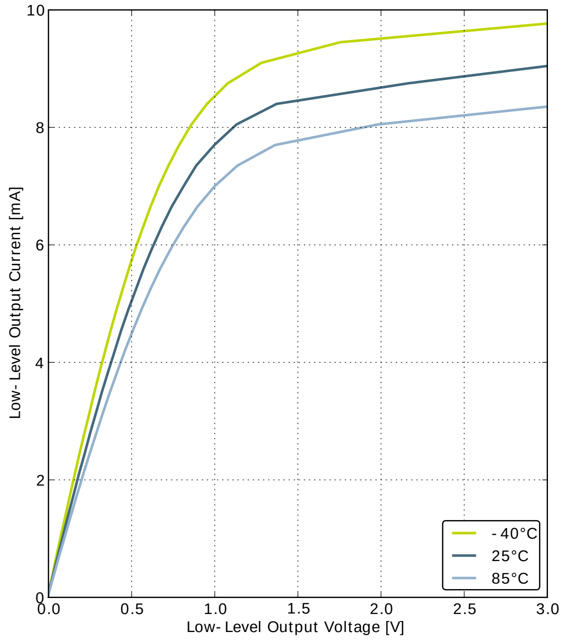


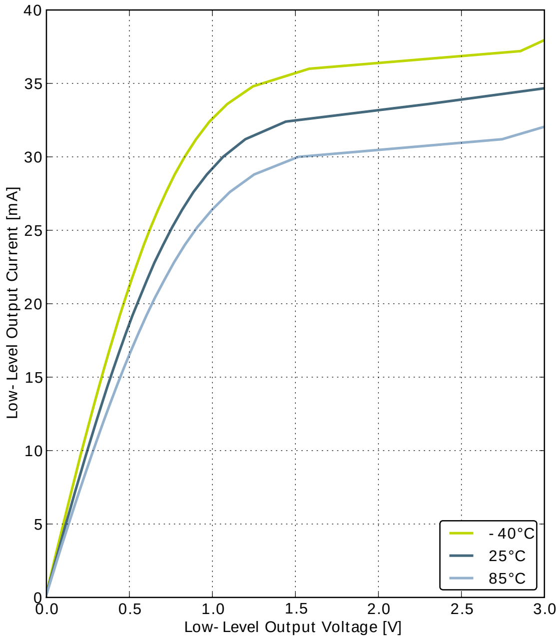
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



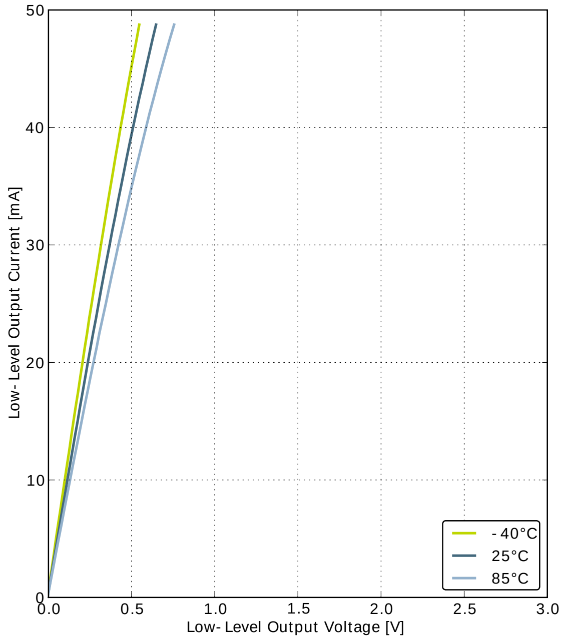
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

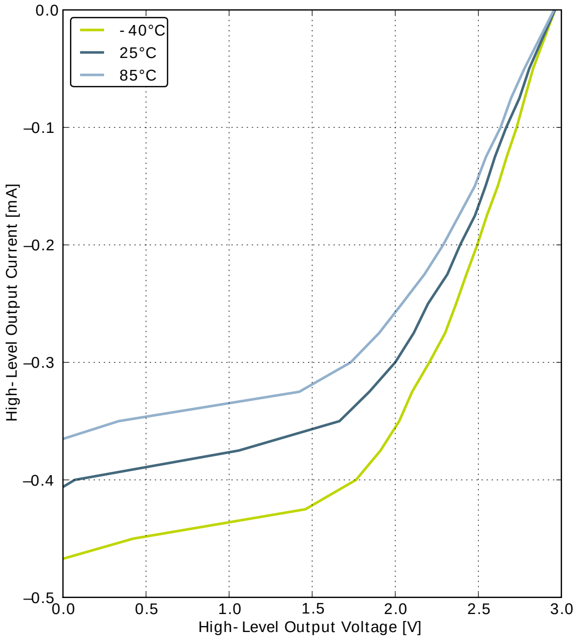


GPIO_Px_CTRL DRIVEMODE = STANDARD

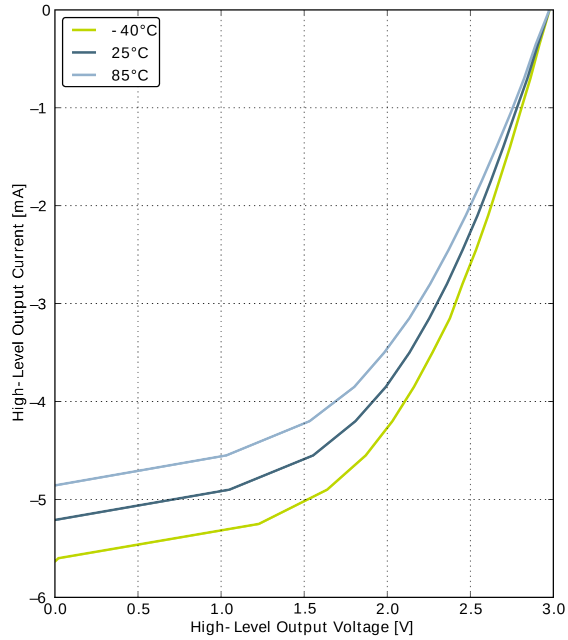


GPIO_Px_CTRL DRIVEMODE = HIGH

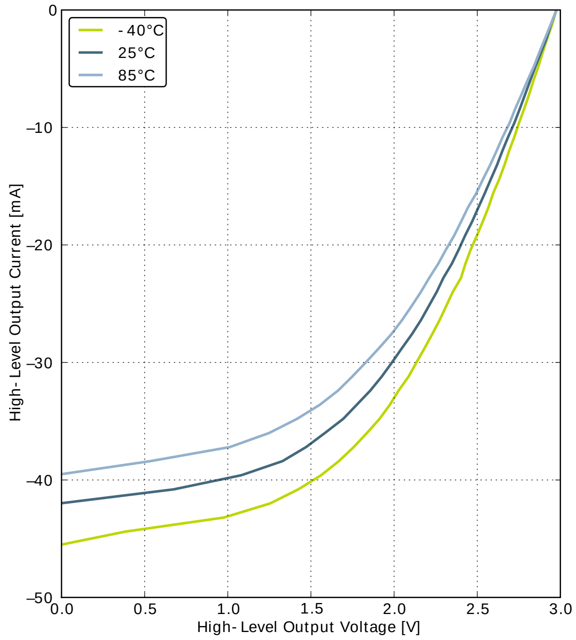
Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



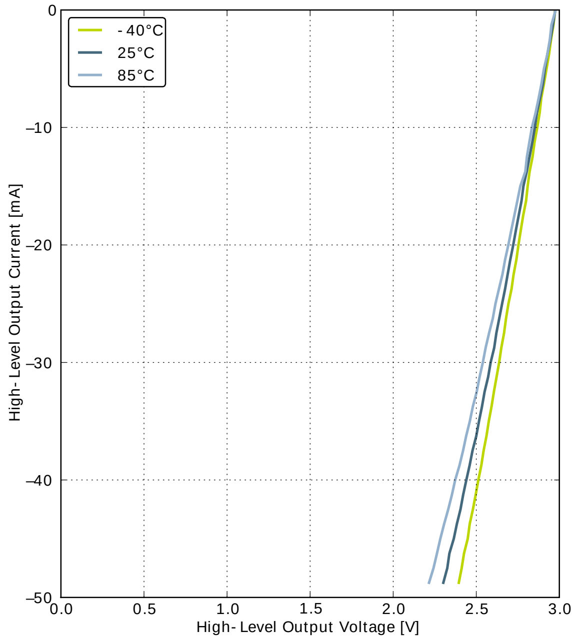
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



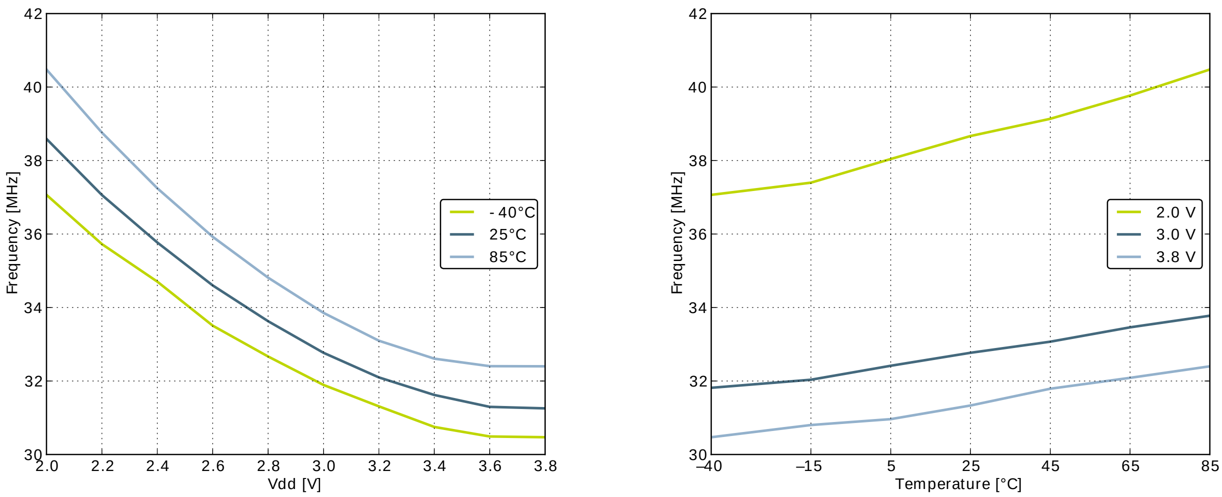
GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.29	32.768	34.28	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			190		nA
$TUNESTEP_{LFRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



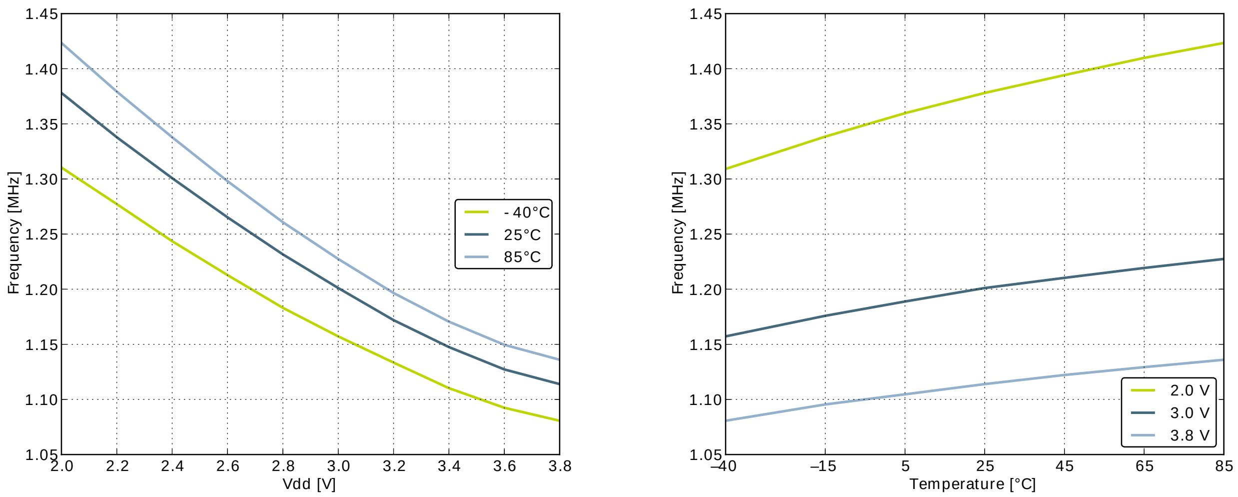
3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption (Production test condition = 14 MHz)	f_{HFRCO} = 21 MHz		93	175	µA
		f_{HFRCO} = 14 MHz		77	140	µA
		f_{HFRCO} = 11 MHz		72	125	µA
		f_{HFRCO} = 6.6 MHz		63	105	µA
		f_{HFRCO} = 1.2 MHz		22	40	µA
$TUNESTEP_{HFRCO}$	Frequency step for LSB change in TUNING value			0.3[1]		%

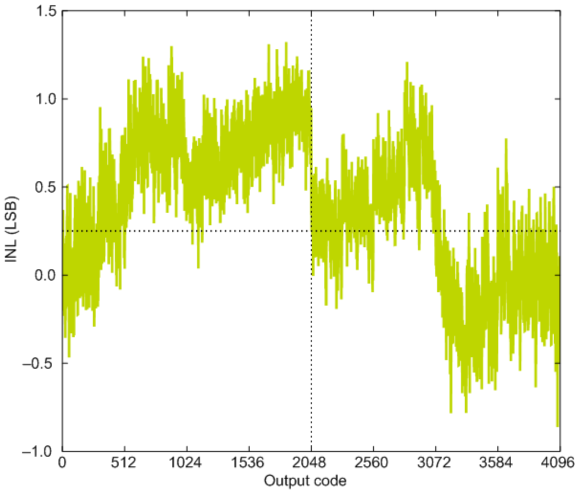
[1]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

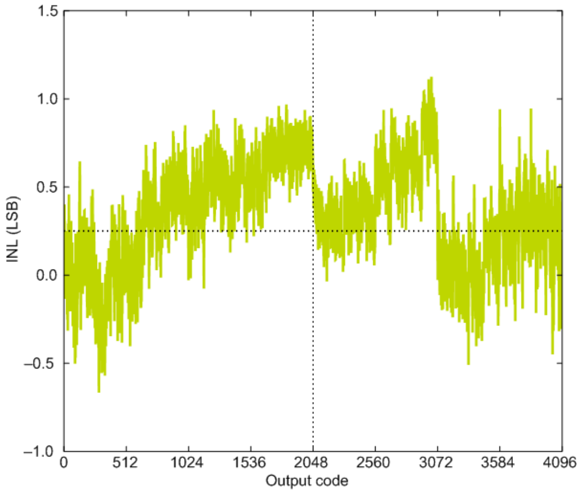


Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		70		dB
$SINAD_{ADC}$	SIgnal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc

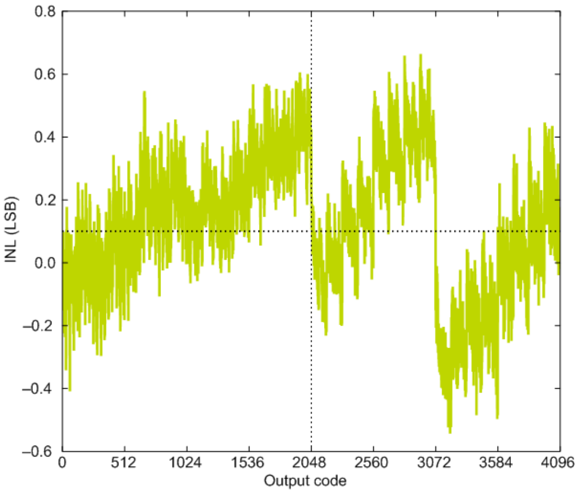
Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C



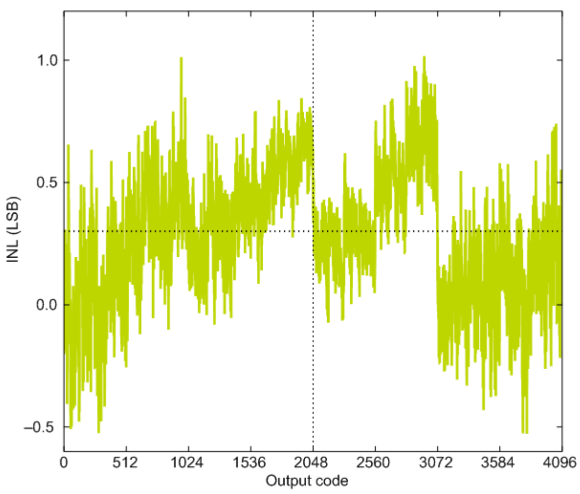
1.25V Reference



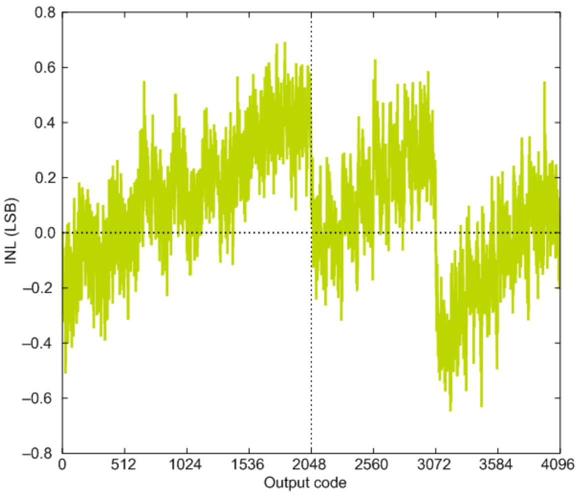
2.5V Reference



2XVDDVSS Reference

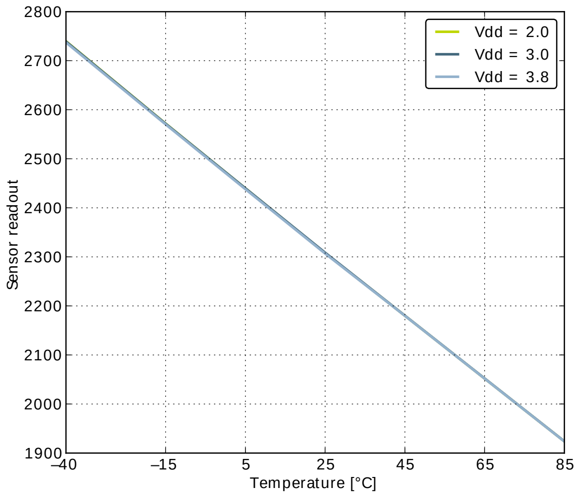


5VDIFF Reference



VDD Reference

Figure 3.33. ADC Temperature sensor readout



3.11 Current Digital Analog Converter (IDAC)

Table 3.15. IDAC Range 0 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		11.7		µA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			0.84		µA
I_{STEP}	Step size			0.049		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = V_{DD} - 100mV		0.73		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0V, STEPSEL=0x10		0.3		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		11.7		nA/V

Table 3.16. IDAC Range 0 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		13.7		µA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			0.84		µA
I_{STEP}	Step size			0.050		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		0.16		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		0.2		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		12.5		nA/V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			8.44		µA
I_{STEP}	Step size			0.495		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		0.55		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		2.8		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		94.4		nA/V

Table 3.21. IDAC Range 3 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		18.3		µA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			34.03		µA
I_{STEP}	Step size			1.996		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = V_{DD} - 100 mV		3.18		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		10.9		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		159.5		nA/V

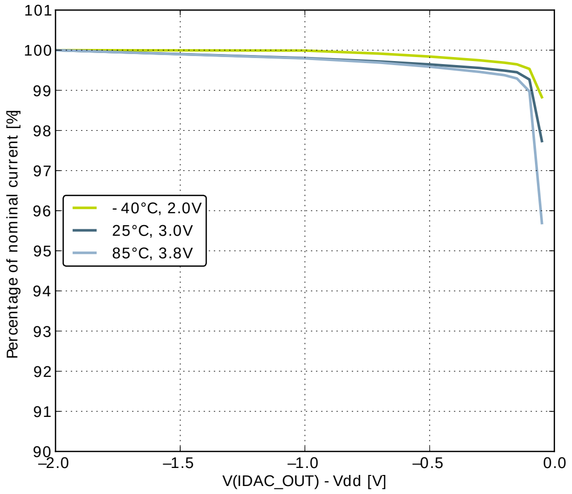
Table 3.22. IDAC Range 3 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		62.9		µA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			34.16		µA
I_{STEP}	Step size			2.003		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		1.65		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		10.9		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		148.6		nA/V

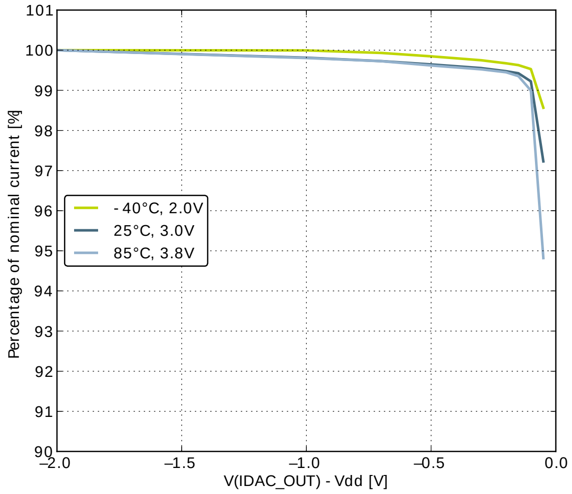
Table 3.23. IDAC

Symbol	Parameter	Min	Typ	Max	Unit
$t_{IDACSTART}$	Start-up time, from enabled to output settled		40		µs

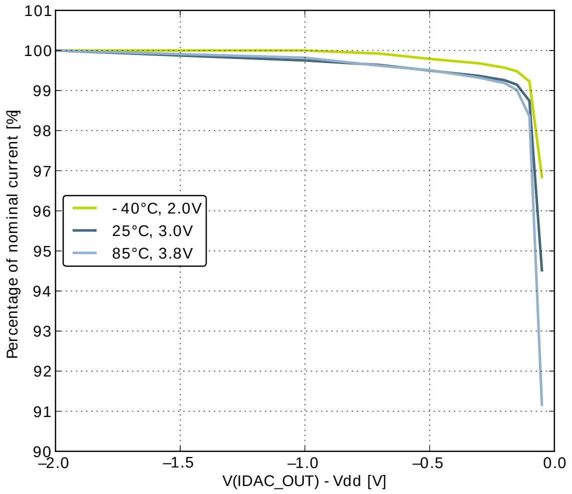
Figure 3.34. IDAC Source Current as a function of voltage on IDAC_OUT



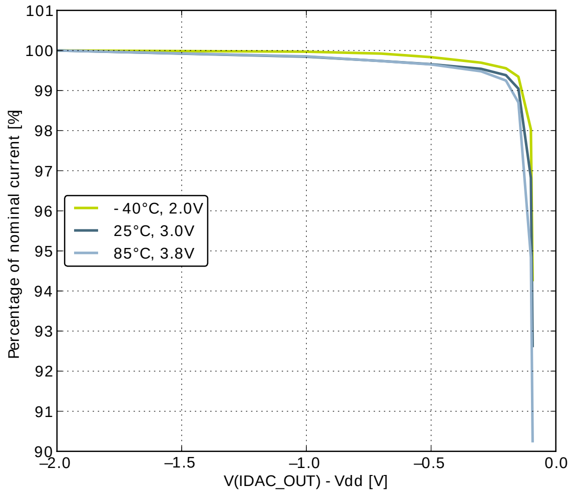
Range 0



Range 1



Range 2



Range 3

Table 3.27. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400[1]	kHz
t_{LOW}	SCL clock low time	1.3			µs
t_{HIGH}	SCL clock high time	0.6			µs
$t_{SU,DAT}$	SDA set-up time	100			ns
$t_{HD,DAT}$	SDA hold time	8		900[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	0.6			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.6			µs
$t_{SU,STO}$	STOP condition set-up time	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32ZG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 5).

Table 3.28. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32ZG Reference Manual.

3.15 Digital Peripherals

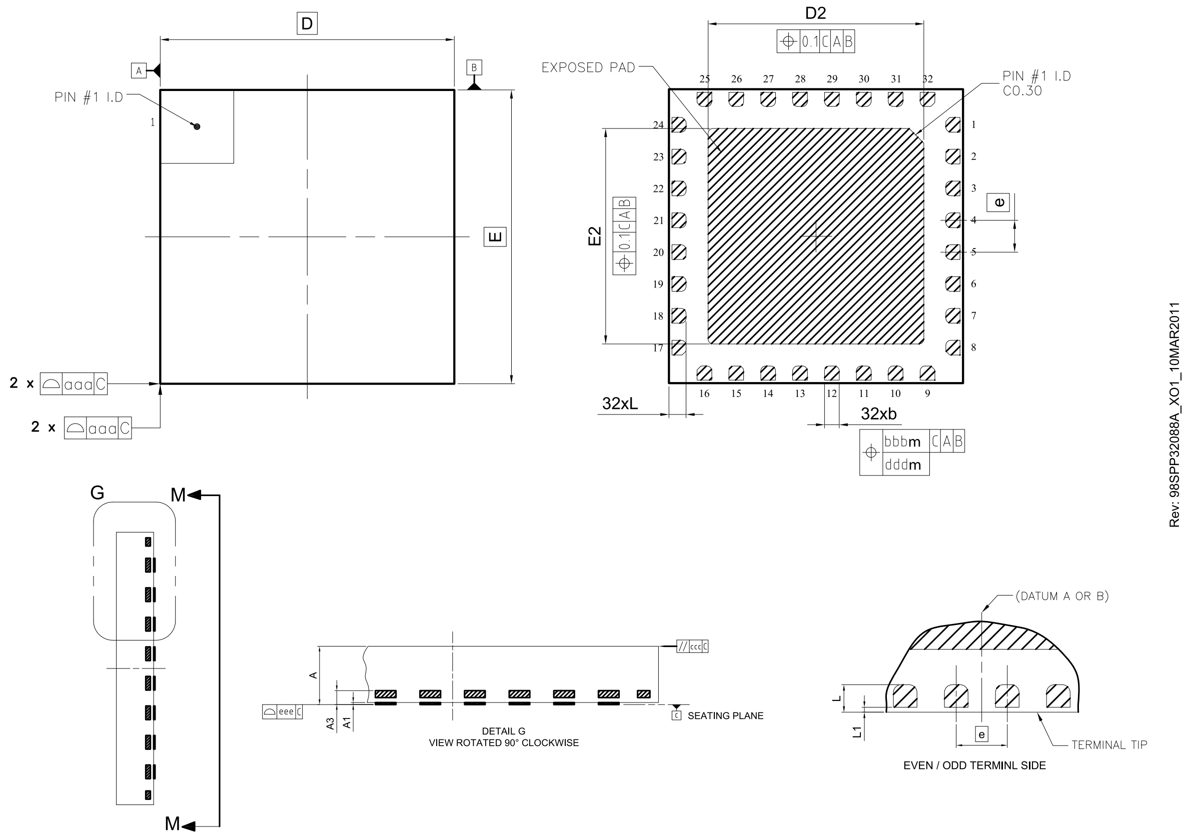
Table 3.29. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{AES}	AES current	AES idle current, clock enabled		2.5		µA/ MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/ MHz
I_{PRS}	PRS current	PRS idle current		2.81		µA/ MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/ MHz

4.4 QFN32 Package

Figure 4.2. QFN32



Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Table 4.4. QFN32 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00		0.25			4.30	4.30		0.35	0.00					
Nom	0.85	-	0.203 REF	0.30	6.00 BSC	6.00 BSC	4.40	4.40	0.65 BSC	0.40		0.10	0.10	0.10	0.05	0.08
Max	0.90	0.05		0.35			4.50	4.50		0.45	0.10					

The QFN32 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

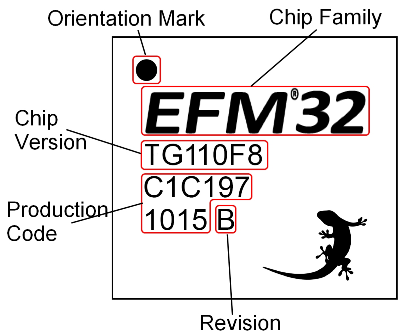
For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 59) .

6.3 Errata

Please see the errata document for EFM32ZG210 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

7 Revision History

7.1 Revision 1.10

March 6th, 2015

Updated ADC data, updated temperature sensor graph and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Updated Max ESR_{HFXO} value for Crystal Frequency of 24 MHz.

Updated current consumption.

Updated LFXO and HFXO data.

Updated LFRCO and HFRCO data.

Updated ACMP data.

Updated VCMP data.

Updated Memory Map.

Added DMA current in Digital Peripherals section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated Package dimensions table.

Updated block diagram.

7.2 Revision 1.00

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Removed "Preliminary" markings.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ADC data.

Updated ACMP data.

7.3 Revision 0.61

November 21st, 2013

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B Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

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