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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 66 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 33x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn128vll10 |

# 1 Ratings

## 1.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

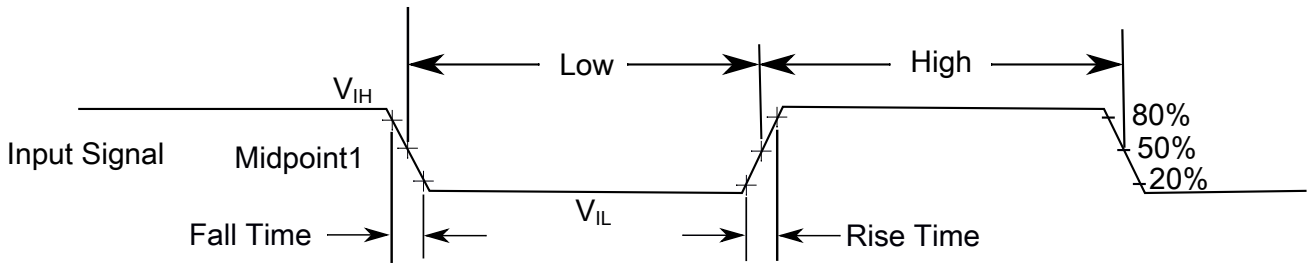
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $USBV_{DD}$ | USB Transceiver supply voltage | –0.3 | 3.8 | V |
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 145 | mA |
| $V_{DIO}$ | Digital input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{AIO}$ | Analog[1] | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Maximum current single pin limit (applies to all digital pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{USB0\_DP}$ | USB0_DP input voltage | –0.3 | 3.63 | V |
| $V_{USB0\_DM}$ | USB0_DM input voltage | –0.3 | 3.63 | V |
| $V_{BAT}$ | RTC battery supply voltage | –0.3 | 3.8 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 2 General

## 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.




The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 2. Input signal measurement reference**

## 2.2 Nonswitching electrical specifications

**Table 5. Power mode transition operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | µs | 1 |
| | • VLLS0 → RUN | — | — | 135 | µs | |
| | • VLLS1 → RUN | — | — | 135 | µs | |
| | • VLLS2 → RUN | — | — | 75 | µs | |
| | • VLLS3 → RUN | — | — | 75 | µs | |
| | • LLS2 → RUN | — | — | 6 | µs | |
| | • LLS3 → RUN | — | — | 6 | µs | |
| | • VLPS → RUN | — | — | 5.7 | µs | |
| | • STOP → RUN | — | — | 5.7 | µs | |

1. Normal boot (FTFA_OPT[LPBOOT]=1)

## 2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 6. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash | | | | | |

*Table continues on the next page...*

## Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | @ 1.8V | — | 19.51 | 20.24 | mA | 2, 3, 4 |
| | @ 3.0V | — | 19.51 | 20.24 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, code executing from flash | | | | | |
| | @ 1.8V | — | 16.9 | 17.63 | mA | 5 |
| | @ 3.0V | — | 17.0 | 17.73 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current — all peripheral clocks enabled, code executing from flash | | | | | |
| | @ 1.8V | — | 22.8 | 23.53 | mA | 6 |
| | @ 3.0V | — | 22.9 | 23.63 | mA | |
| $I_{DD\_RUN}$ | Run mode current in Compute operation — CoreMark benchmark code executing from flash | | | | | |
| | @ 1.8V | — | 11.39 | 12.12 | mA | 2, 3, 7 |
| | @ 3.0V | — | 11.58 | 12.31 | mA | |
| $I_{DD\_RUN}$ | Run mode current in Compute operation — code executing from flash | | | | | |
| | @ 1.8V | — | 10.90 | 11.90 | mA | 7 |
| | @ 3.0V | — | 10.90 | 12.23 | mA | |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash | | | | | |
| | @ 1.8V | — | 11.8 | 12.53 | mA | 8 |
| | @ 3.0V | — | 11.9 | 12.63 | mA | |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | |
| | @ 1.8V | — | 15.5 | 16.23 | mA | 9 |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 15.6 | 16.33 | mA | |
| | • @ 70°C | — | 15.6 | 16.33 | mA | |
| | • @ 85°C | — | 15.6 | 16.33 | mA | |
| | • @ 105°C | — | 16.3 | 17.03 | mA | |
| $I_{DD\_RUN}$ | Run mode current — Compute operation, code executing from flash | | | | | |
| | @ 1.8V | — | 10.9 | 11.63 | mA | 10 |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 10.9 | 11.63 | mA | |
| | • @ 70°C | — | 10.9 | 11.63 | mA | |
| | • @ 85°C | — | 10.9 | 11.63 | mA | |
| | • @ 105°C | — | 11.5 | 12.23 | mA | |

*Table continues on the next page...*

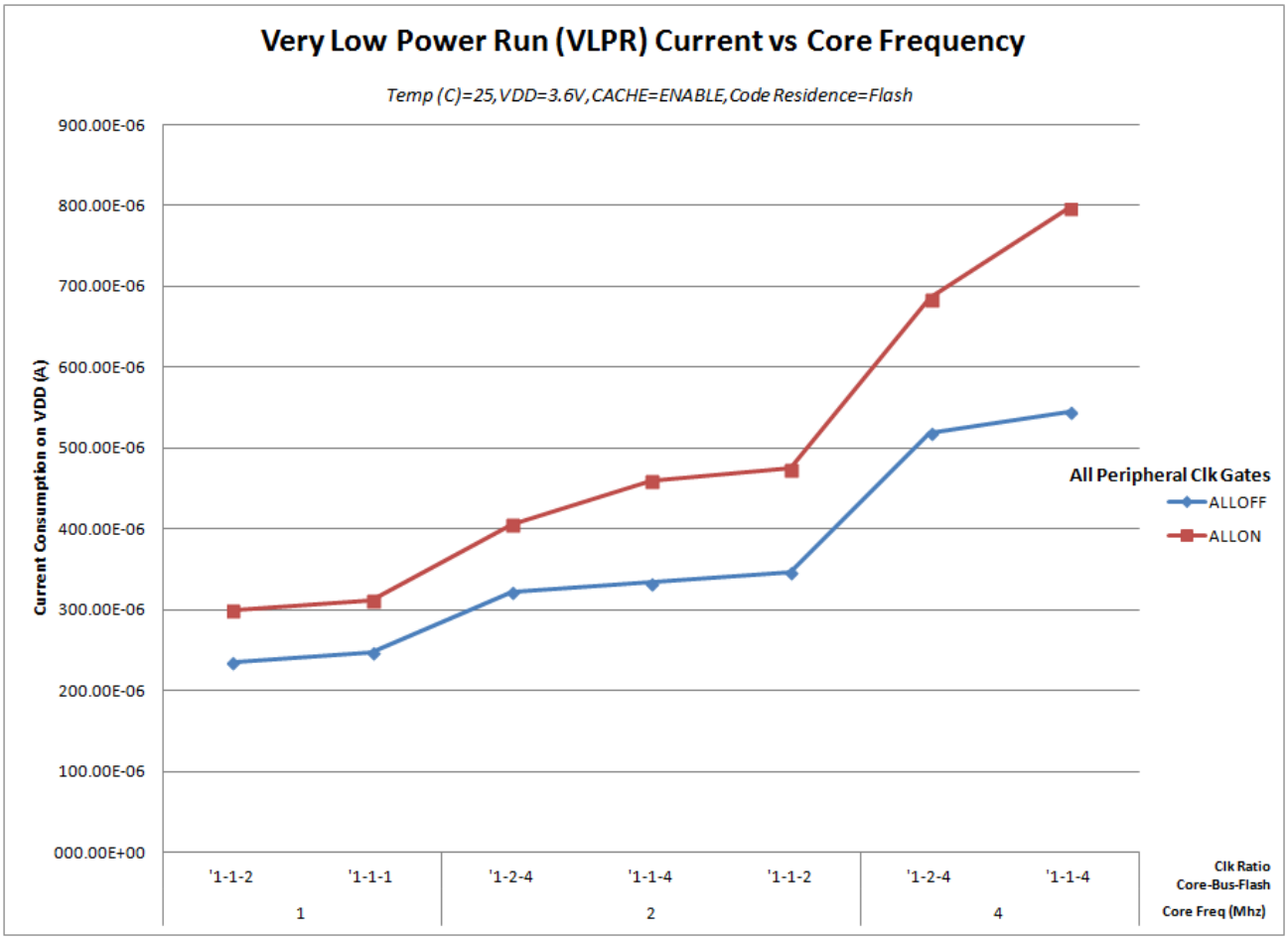



**Figure 4. VLPR mode supply current vs. core frequency**

## 2.2.6 EMC radiated emissions operating behaviors

**Table 8. EMC radiated emissions operating behaviors for 64 LQFP package**

| Parameter | Conditions | Clocks | Frequency range | Level (Typ.) | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{EME}$ | Device configuration, test conditions and EM testing per standard IEC 61967-2.<br>Supply voltages:<br>Temp = 25°C | FSYS = 100 MHz<br>FBUS = 50 MHz<br>External crystal = 10 MHz | 150 kHz–50 MHz | 13 | dBuV | 1, 2, 3 |
| | | | 50 MHz–150 MHz | 24 | | |
| | | | 150 MHz–500 MHz | 23 | | |
| | | | 500 MHz–1000 MHz | 7 | | |
| | | | IEC level | L | | 4 |

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MK22FN128VLH10 .
3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

# 2.4 Thermal specifications

## 2.4.1 Thermal operating requirements

**Table 12. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C | |
| $T_A$ | Ambient temperature | –40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

## 2.4.2 Thermal attributes

| Board type | Symbol | Description | 121 XFBGA | 100 LQFP | 64 LQFP | 64 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 46.6 | 63 | 69 | 53.8 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 39.3 | 50 | 51 | 46.0 | °C/W | 2 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 39.0 | 53 | 57 | 45.8 | °C/W | 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 35.3 | 44 | 44 | 41.0 | °C/W | 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 36.7 | 36 | 33 | 43.4 | °C/W | 4 |

*Table continues on the next page...*

**Table 16. MCG specifications (continued)**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | 2197 × $f_{fll\_ref}$ | | | | | |
| | | High range (DRS=11)<br>2929 × $f_{fll\_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc\_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz<br>• $f_{VCO}$ = 98 MHz | | —<br>— | —<br>180<br>150 | —<br>— | ps | |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 7 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2.0 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 3.3.2 IRC48M specifications

**Table 17. IRC48M specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DD48M}$ | Supply current | — | 400 | 500 | µA | |
| $f_{irc48m}$ | Internal reference frequency | — | 48 | — | MHz | |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C<br>Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | —<br>— | <br>± 0.2 | <br>± 0.5 | <br>%$f_{irc48m}$ | <br>1 |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature<br>Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | <br>— | <br>± 0.4 | <br>± 1.0 | <br>%$f_{irc48m}$ | <br>1 |
| $\Delta f_{irc48m\_ol\_lv}$ | Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature<br>Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0)<br>Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | <br>—<br>— | <br>± 0.4<br>± 0.5 | <br>± 1.0<br>± 1.5 | <br>%$f_{irc48m}$ | 1 |

*Table continues on the next page...*

**Table 18. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$ and $C_y$ can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 3.3.3.2 Oscillator frequency specifications

**Table 19. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |

*Table continues on the next page...*

### 3.6.3.2 12-bit DAC operating behaviors

**Table 31. 12-bit DAC operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 330 | μA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 1200 | μA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | μs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ ≥ 2.4 V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | μV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance (load = 3 kΩ) | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h<br>• High power ($SP_{HP}$)<br>• Low power ($SP_{LP}$) | <br>1.2<br>0.05 | <br>1.7<br>0.12 | <br>—<br>— | V/μs | |
| BW | 3dB bandwidth<br>• High power ($SP_{HP}$)<br>• Low power ($SP_{LP}$) | <br>550<br>40 | <br>—<br>— | <br>—<br>— | kHz | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

### 3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

**NOTE**

The MCGFLLCLK does not meet the USB jitter or signaling rate specifications for certification.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

### 3.8.2 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 36. Master mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 25 | MHz | |
| DS1 | DSPI_SCK output cycle time | 2 x $t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns | |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | ($t_{BUS}$ x 2) – 2 | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 2 | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 16.2 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

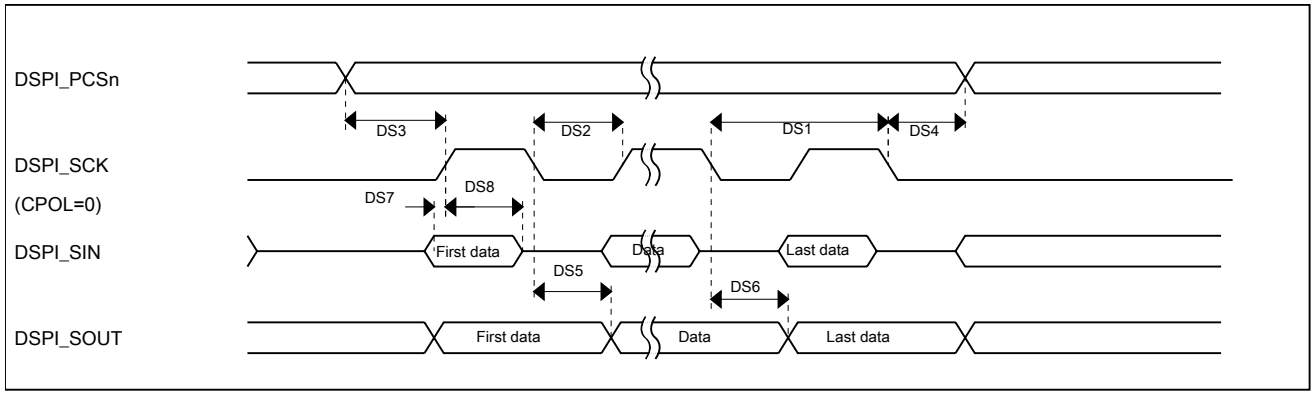



**Figure 19. DSPI classic SPI timing — master mode**

## Table 37. Slave mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 12.5 | MHz | 1 |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns | |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 21.4 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.6 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | $\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven | — | 17 | ns | |
| DS16 | $\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven | — | 17 | ns | |

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

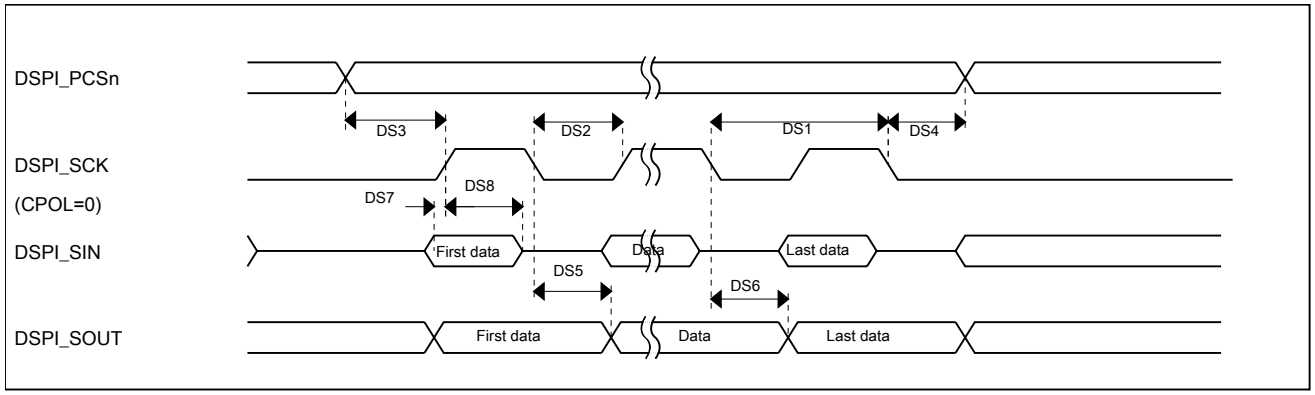



**Figure 21. DSPI classic SPI timing — master mode**

**Table 39. Slave mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6.25 | MHz |
| DS9 | DSPI_SCK input cycle time | 8 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2)}$ + 4 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 29.5 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 3.2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven | — | 25 | ns |
| DS16 | $\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven | — | 25 | ns |

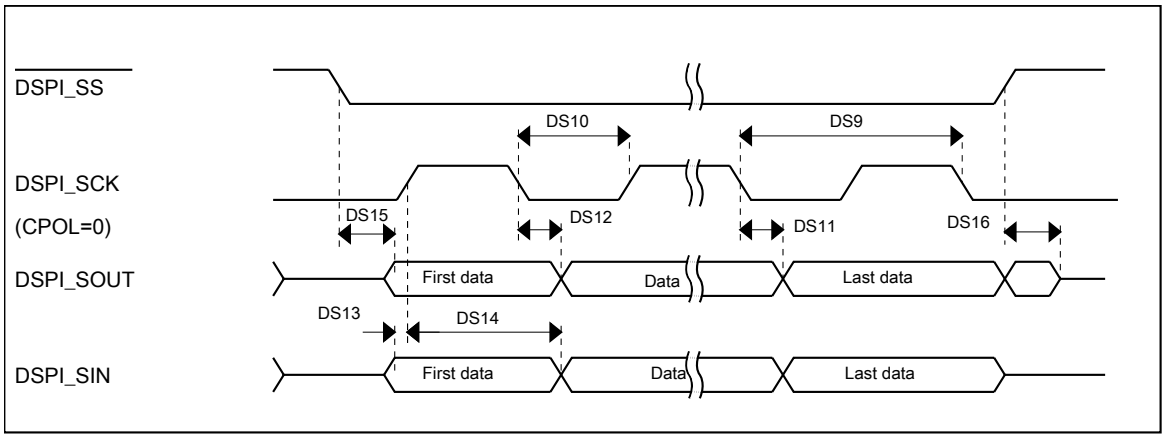



**Figure 22. DSPI classic SPI timing — slave mode**

**Table 41. I²C 1 Mbps timing (continued)**

| Characteristic | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Data set-up time | $t_{SU}$; DAT | 50 | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | 20 +0.1$C_b$, [2] | 120 | ns |
| Fall time of SDA and SCL signals | $t_f$ | 20 +0.1$C_b$ [2] | 120 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 0.26 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 0.5 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | 0 | 50 | ns |

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. $C_b$ = total capacitance of the one bus line in pF.

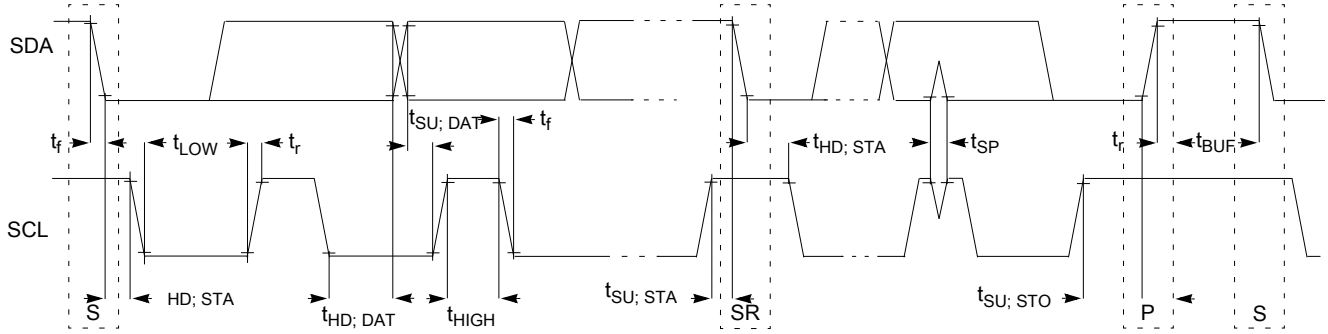



**Figure 23. Timing definition for devices on the I²C bus**

## 3.8.5 UART switching specifications

See General switching specifications.

## 3.8.6 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

## Table 44. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | -1.0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 27 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

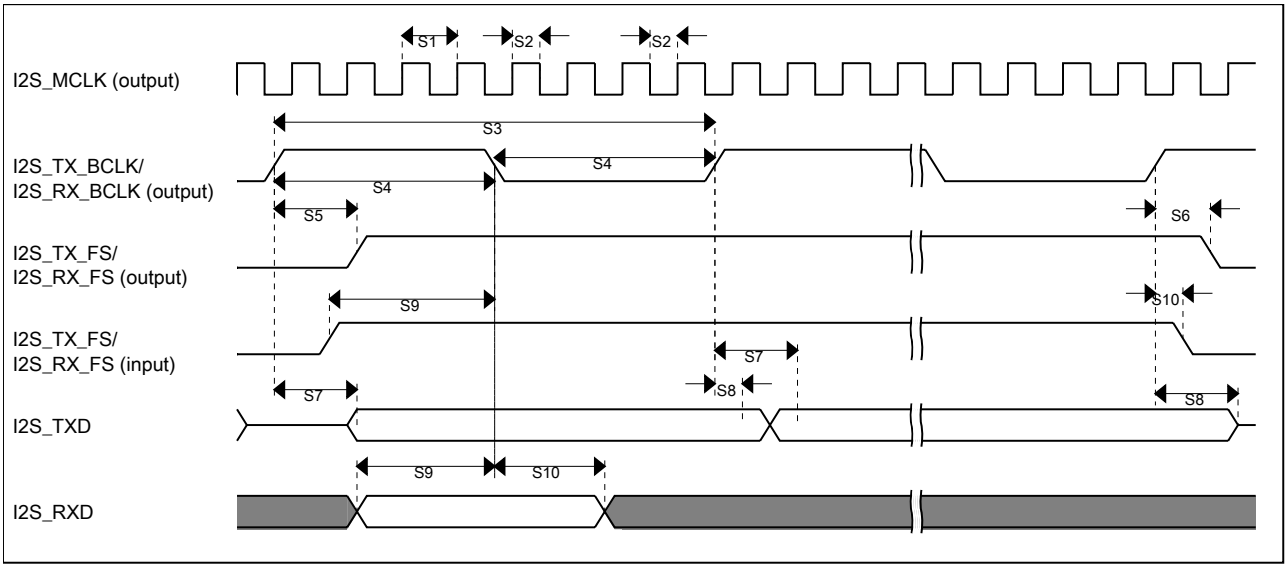



**Figure 26. I2S/SAI timing — master modes**

## Table 45. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |

*Table continues on the next page...*

| If you want the drawing for this package | Then use this document number |
|---|---|
| 64-pin LQFP | 98ASS23234W |
| 64-pin MAPBGA | 98ASA00420D |
| 100-pin LQFP | 98ASS23308W |
| 121-pin XFBGA | 98ASA00595D |

# 5 Pinout

## 5.1 K22 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 121 BGA | 100 LQFP | 64 LQFP | 64 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E4 | 1 | 1 | A1 | PTE0/ CLKOUT32 K | ADC1_ SE4a | ADC1_ SE4a | PTE0/ CLKOUT32 K | SPI1_ PCS1 | UART1_TX | | | I2C1_SDA | RTC_ CLKOUT | |
| E3 | 2 | 2 | B1 | PTE1/ LLWU_P0 | ADC1_ SE5a | ADC1_ SE5a | PTE1/ LLWU_P0 | SPI1_ SOUT | UART1_RX | | | I2C1_SCL | SPI1_SIN | |
| E2 | 3 | — | — | PTE2/ LLWU_P1 | ADC1_ SE6a | ADC1_ SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_ CTS_b | | | | | |
| F4 | 4 | — | — | PTE3 | ADC1_ SE7a | ADC1_ SE7a | PTE3 | SPI1_SIN | UART1_ RTS_b | | | | SPI1_ SOUT | |
| H7 | 5 | — | — | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_ PCS0 | LPUART0_ TX | | | | | |
| G4 | 6 | — | — | PTE5 | DISABLED | | PTE5 | SPI1_ PCS2 | LPUART0_ RX | | | | | |
| F3 | 7 | — | — | PTE6 | DISABLED | | PTE6 | SPI1_ PCS3 | LPUART0_ CTS_b | I2S0_ MCLK | | | USB_SOF_ OUT | |
| E6 | 8 | 3 | C5 | VDD | VDD | VDD | | | | | | | | |
| G7 | 9 | 4 | C4 | VSS | VSS | VSS | | | | | | | | |
| L6 | — | — | — | VSS | VSS | VSS | | | | | | | | |
| F1 | 10 | 5 | E1 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |
| F2 | 11 | 6 | D1 | USB0_DM | USB0_DM | USB0_DM | | | | | | | | |
| G1 | 12 | 7 | E2 | USBVDD | USBVDD | USBVDD | | | | | | | | |
| G2 | 13 | 8 | D2 | NC | NC | NC | | | | | | | | |
| H1 | 14 | — | — | ADC0_DP1 | ADC0_DP1 | ADC0_DP1 | | | | | | | | |

| 121 BGA | 100 LQFP | 64 LQFP | 64 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J5 | 32 | — | — | PTE25 | ADC0_ SE18 | ADC0_ SE18 | PTE25 | | | | I2C0_SDA | EWM_IN | | |
| H6 | 33 | — | — | PTE26/ CLKOUT32 K | DISABLED | | PTE26/ CLKOUT32 K | | | | | RTC_ CLKOUT | USB_ CLKIN | |
| J6 | 34 | 22 | D3 | PTA0 | JTAG_ TCLK/ SWD_CLK/ EZP_CLK | | PTA0 | UART0_ CTS_b | FTM0_CH5 | | | | JTAG_ TCLK/ SWD_CLK | EZP_CLK |
| H8 | 35 | 23 | D4 | PTA1 | JTAG_TDI/ EZP_DI | | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| J7 | 36 | 24 | E5 | PTA2 | JTAG_ TDO/ TRACE_ SWO/ EZP_DO | | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_ TDO/ TRACE_ SWO | EZP_DO |
| H9 | 37 | 25 | D5 | PTA3 | JTAG_ TMS/ SWD_DIO | | PTA3 | UART0_ RTS_b | FTM0_CH0 | | | | JTAG_ TMS/ SWD_DIO | |
| J8 | 38 | 26 | G5 | PTA4/ LLWU_P3 | NMI_b/ EZP_CS_b | | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| K7 | 39 | 27 | F5 | PTA5 | DISABLED | | PTA5 | USB_ CLKIN | FTM0_CH2 | | | I2S0_TX_ BCLK | JTAG_ TRST_b | |
| E5 | 40 | — | — | VDD | VDD | VDD | | | | | | | | |
| G3 | 41 | — | — | VSS | VSS | VSS | | | | | | | | |
| K8 | 42 | 28 | H6 | PTA12 | DISABLED | | PTA12 | | FTM1_CH0 | | | I2S0_TXD0 | FTM1_QD_ PHA | |
| L8 | 43 | 29 | G6 | PTA13/ LLWU_P4 | DISABLED | | PTA13/ LLWU_P4 | | FTM1_CH1 | | | I2S0_TX_ FS | FTM1_QD_ PHB | |
| K9 | 44 | — | — | PTA14 | DISABLED | | PTA14 | SPI0_ PCS0 | UART0_TX | | | I2S0_RX_ BCLK | | |
| L9 | 45 | — | — | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | | | I2S0_RXD0 | | |
| J10 | 46 | — | — | PTA16 | DISABLED | | PTA16 | SPI0_ SOUT | UART0_ CTS_b | | | I2S0_RX_ FS | | |
| H10 | 47 | — | — | PTA17 | ADC1_ SE17 | ADC1_ SE17 | PTA17 | SPI0_SIN | UART0_ RTS_b | | | I2S0_ MCLK | | |
| L10 | 48 | 30 | G7 | VDD | VDD | VDD | | | | | | | | |
| K10 | 49 | 31 | H7 | VSS | VSS | VSS | | | | | | | | |
| L11 | 50 | 32 | H8 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_ FLT2 | FTM_ CLKIN0 | | | | |
| K11 | 51 | 33 | G8 | PTA19 | XTAL0 | XTAL0 | PTA19 | | FTM1_ FLT0 | FTM_ CLKIN1 | | LPTMR0_ ALT1 | | |
| J11 | 52 | 34 | F8 | RESET_b | RESET_b | RESET_b | | | | | | | | |
| G11 | 53 | 35 | F7 | PTB0/ LLWU_P5 | ADC0_ SE8/ ADC1_SE8 | ADC0_ SE8/ ADC1_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_ PHA | | |

| 121 BGA | 100 LQFP | 64 LQFP | 64 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K3 | — | — | — | NC | NC | NC | | | | | | | | |
| H4 | — | — | — | NC | NC | NC | | | | | | | | |
| B11 | — | — | — | NC | NC | NC | | | | | | | | |
| C11 | — | — | — | NC | NC | NC | | | | | | | | |
| H11 | — | — | — | NC | NC | NC | | | | | | | | |
| C1 | — | — | — | NC | NC | NC | | | | | | | | |
| D2 | — | — | — | NC | NC | NC | | | | | | | | |
| D1 | — | — | — | NC | NC | NC | | | | | | | | |
| E1 | — | — | — | NC | NC | NC | | | | | | | | |
| J3 | — | — | — | NC | NC | NC | | | | | | | | |
| H3 | — | — | — | NC | NC | NC | | | | | | | | |
| J9 | — | — | — | NC | NC | NC | | | | | | | | |
| J4 | — | — | — | NC | NC | NC | | | | | | | | |
| A10 | — | — | — | NC | NC | NC | | | | | | | | |
| A9 | — | — | — | NC | NC | NC | | | | | | | | |
| B1 | — | — | — | NC | NC | NC | | | | | | | | |
| C2 | — | — | — | NC | NC | NC | | | | | | | | |
| L7 | — | — | — | NC | NC | NC | | | | | | | | |
| F11 | — | — | — | NC | NC | NC | | | | | | | | |
| E11 | — | — | — | NC | NC | NC | | | | | | | | |
| A4 | — | — | — | NC | NC | NC | | | | | | | | |

## 5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

**Table 48. Recommended connection for unused analog interfaces**

| Pin Type | | Short recommendation | Detailed recommendation |
|---|---|---|---|
| Analog/non GPIO | PGAx/ADCx | Float | Analog input - Float |
| Analog/non GPIO | ADCx/CMPx | Float | Analog input - Float |
| Analog/non GPIO | VREF_OUT | Float | Analog output - Float |
| Analog/non GPIO | DACx_OUT | Float | Analog output - Float |
| Analog/non GPIO | RTC_WAKEUP_B | Float | Analog output - Float |
| Analog/non GPIO | XTAL32 | Float | Analog output - Float |
| Analog/non GPIO | EXTAL32 | Float | Analog input - Float |

*Table continues on the next page...*

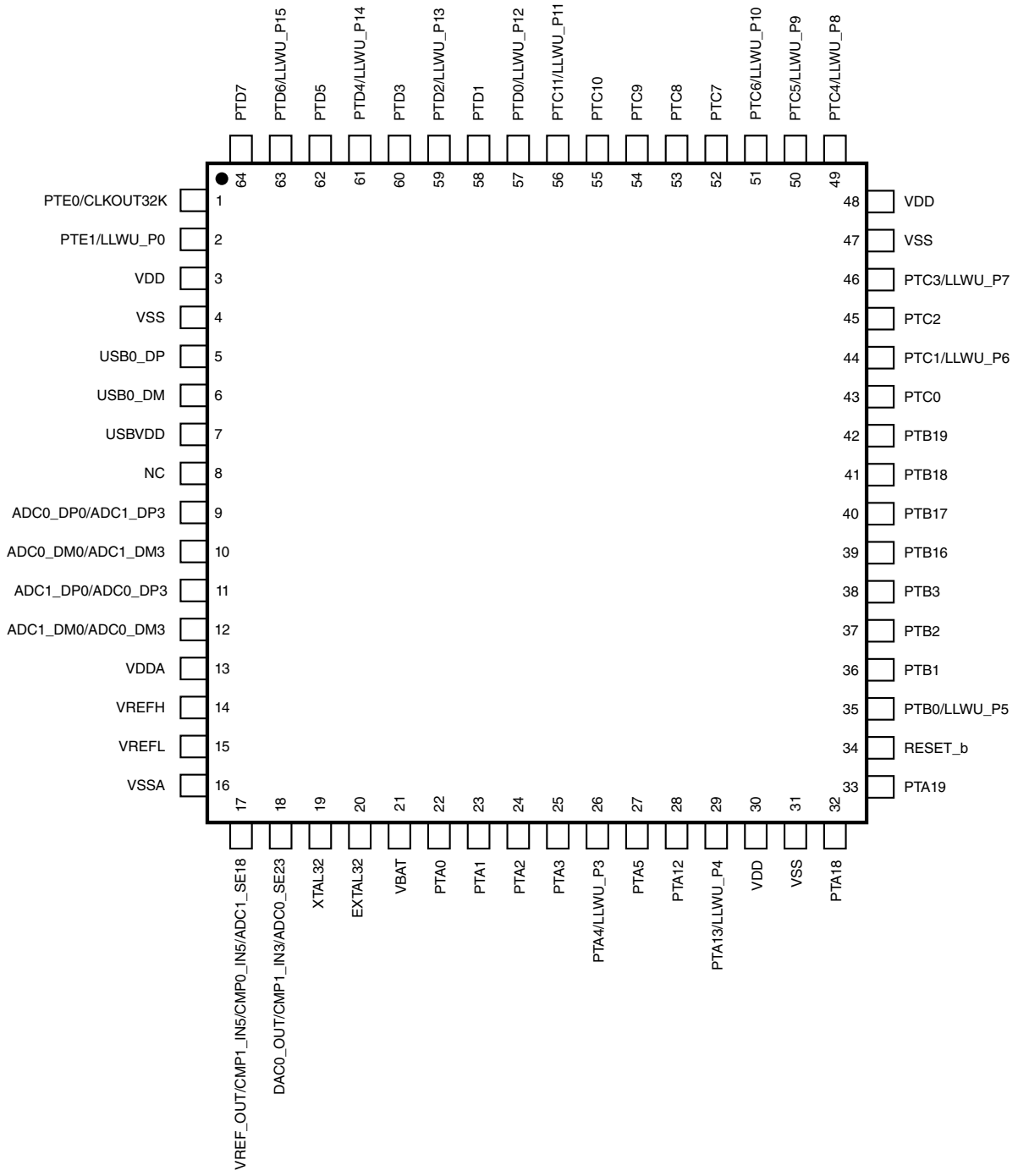



**Figure 30. K22 64 LQFP Pinout Diagram (top view)**

## 6.4 Example

This is an example part number:

MK22FN128VDC10

## 6.5 121-pin XFBGA part marking

The 121-pin XFBGA package parts follow the part-marking scheme in the following table.

**Table 49. 121-pin XFBGA part marking**

| MK Partnumber | MK Part Marking |
|---|---|
| MK22FN128VDC10 | M22J7VDC |

## 6.6 64-pin MAPBGA part marking

The 64-pin MAPBGA package parts follow the part-marking scheme in the following table.

**Table 50. 64-pin MAPBGA part marking**

| MK Partnumber | MK Part Marking |
|---|---|
| MK22FN128VMP10 | M22J7V |

# 7 Terminology and guidelines

## 7.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered. |

*Table continues on the next page...*

## Table 51. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 7 | 08/2016 | • Added Terminology and Guidelines section<br>• Updated the front matter section<br>• Added Device Revision Number Table<br>• Updated Chip Errata naming convention in Related Resource table |
| 6 | 10/2015 | • In "Power consumption operating behaviors" section, added "Low power mode peripheral adders—typical value" table<br>• In "Thermal operating requirements" table, in footnote, corrected "$T_J = T_A + \Theta_{JA}$" to "$T_J = T_A + R_{\Theta JA}$"<br>• Updated "IRC48M specifications" table<br>• Updated "NVM program/erase timing specifications" table; updated values for $t_{hversall}$ (Erase All high-voltage time)<br>• In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation<br>• Added new section, "Recommended connections for unused analog and digital pins" |
| 5 | 4/2015 | • On page 1:<br>  • In first bullet of introduction, updated power consumption data to align with the data in the "Power consumption operating behaviors" table<br>  • In second bullet of introduction, added "USB FS device crystal-less functionality"<br>  • Under "Communication interfaces," updated $I^2C$ bullet to indicate support for up to 1 Mbps operation<br>  • Under "Operating characteristics," specified that voltage range includes flash writes<br>• In "Voltage and current operating requirements" table:<br>  • Removed content related to positive injection<br>  • Updated footnote 1 to say that all analog and I/O pins are internally clamped to $V_{SS}$ only (not $V_{SS}$ and $V_{DD}$)through ESD protection diodes.<br>• In"Power consumption operating behaviors" table:<br>  • Added additional temperature data in power consumption table<br>  • Added Max IDD values based on characterization results equivalent to mean + 3 sigma<br>• Updated "EMC radiated emissions operating behaviors" table<br>• In "Thermal operating requirements" table, added the following footnote for ambient temperature: "Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + \Theta_{JA}$ x chip power dissipation"<br>• Updated "IRC48M Specifications":<br>  • Updated maximum values for $\Delta_{firc48m\_ol\_lv}$ and $\Delta_{firc48m\_ol\_hv}$ (full temperature)<br>  • Added specifications for $\Delta_{firc48m\_ol\_hv}$ (-40°C to 85°C)<br>• Updated notes in "USB electrical specifications" section<br>• In "$I^2C$ timing" table,<br>  • Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V."<br>  • Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 µ<br>• Added "$I^2C$ 1 Mbps timing" table<br>• Specified that the figure, "K22F 64 LQFP Pinout Diagram" is a top view<br>• Specified that the figure, "K22F 64 MAPBGA Pinout Diagram" is a transparent top view<br>• Specified that the figure, "K22F 100 LQFP Pinout Diagram" is a top view |

*Table continues on the next page...*