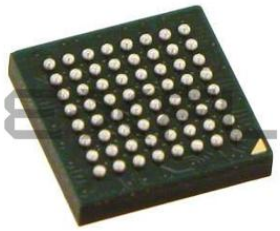

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 22x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk22fn128vmp10

Table of Contents

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
$USBV_{DD}$	USB Transceiver supply voltage	3.0	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	— —	0.35 × V_{DD} 0.3 × V_{DD}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	Analog and I/O pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection)	-3	—	mA	2
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	3
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. USB nominal operating voltage is 3.3 V.
2. All analog and I/O pins are internally clamped to V_{SS} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$.
3. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 1.8V	—	19.51	20.24	mA	2, 3, 4
	@ 3.0V	—	19.51	20.24	mA	
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	16.9	17.63	mA	5
	@ 3.0V	—	17.0	17.73	mA	
I_{DD_HSRUN}	High Speed Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	22.8	23.53	mA	6
	@ 3.0V	—	22.9	23.63	mA	
I_{DD_RUN}	Run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	11.39	12.12	mA	2, 3, 7
	@ 3.0V	—	11.58	12.31	mA	
I_{DD_RUN}	Run mode current in Compute operation — code executing from flash					
	@ 1.8V	—	10.90	11.90	mA	7
	@ 3.0V	—	10.90	12.23	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	11.8	12.53	mA	8
	@ 3.0V	—	11.9	12.63	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	15.5	16.23	mA	9
	@ 3.0V					
	• @ 25°C	—	15.6	16.33	mA	
	• @ 70°C	—	15.6	16.33	mA	
	• @ 85°C	—	15.6	16.33	mA	
	• @ 105°C	—	16.3	17.03	mA	
I_{DD_RUN}	Run mode current — Compute operation, code executing from flash					
	@ 1.8V	—	10.9	11.63	mA	10
	@ 3.0V					
	• @ 25°C	—	10.9	11.63	mA	
	• @ 70°C	—	10.9	11.63	mA	
	• @ 85°C	—	10.9	11.63	mA	
	• @ 105°C	—	11.5	12.23	mA	

Table continues on the next page...

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

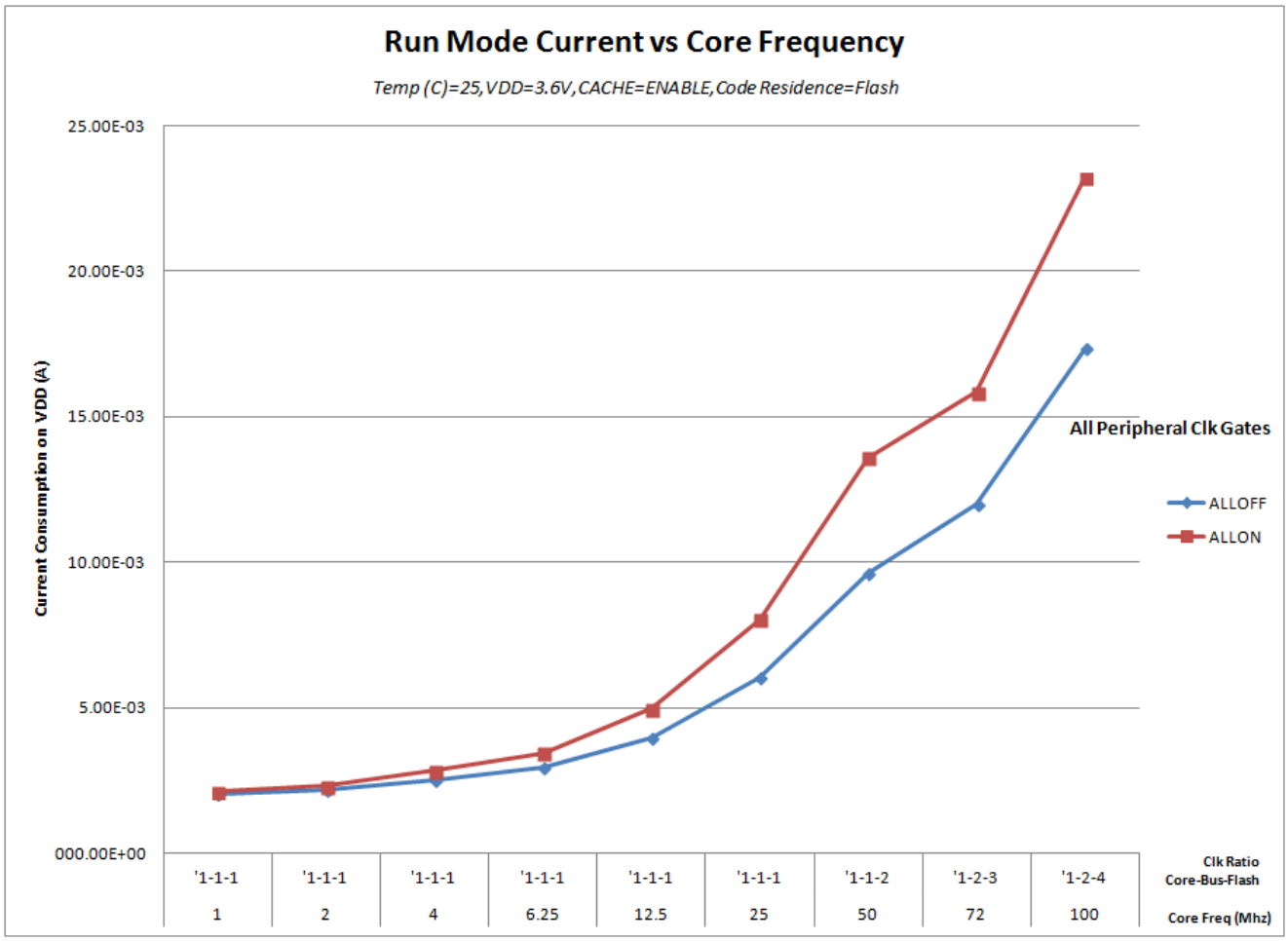


Figure 3. Run mode supply current vs. core frequency

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{BUS}	Bus clock	—	50	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	72	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	

Table continues on the next page...

Table 16. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		2197 × f_{fll_ref}					
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	— 180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2.0 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	— —	 ± 0.2	 ± 0.5	 %f_{irc48m}	 1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	 —	 ± 0.4	 ± 1.0	 %f_{irc48m}	 1
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	 — —	 ± 0.4 ± 0.5	 ± 1.0 ± 1.5	 %f_{irc48m}	1

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	

Table continues on the next page...

3.3.4.2 32 kHz oscillator frequency specifications

Table 21. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 22. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 23. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1

Table continues on the next page...

Table 23. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	140	1150	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 24. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

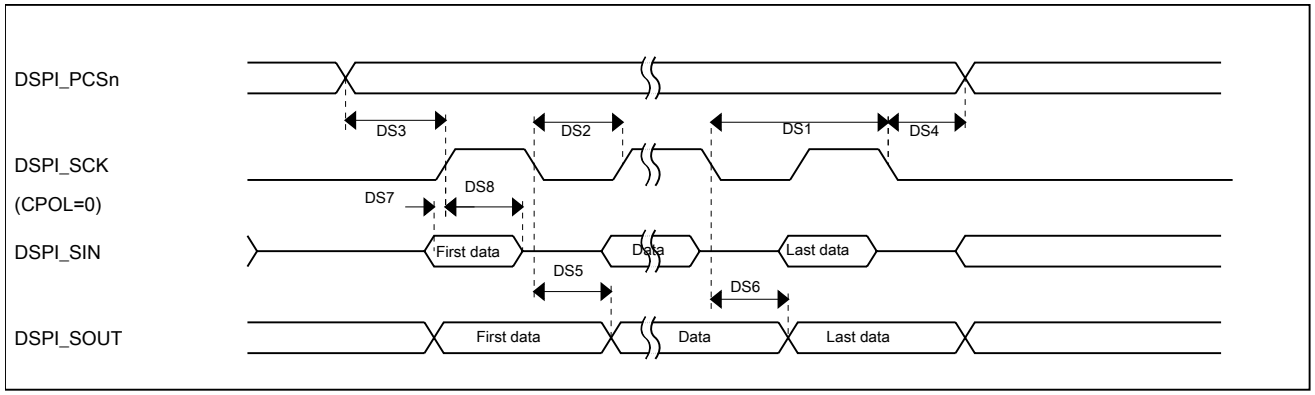


Figure 19. DSPI classic SPI timing — master mode

Table 37. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	12.5	MHz	1
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	17	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	17	ns	

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

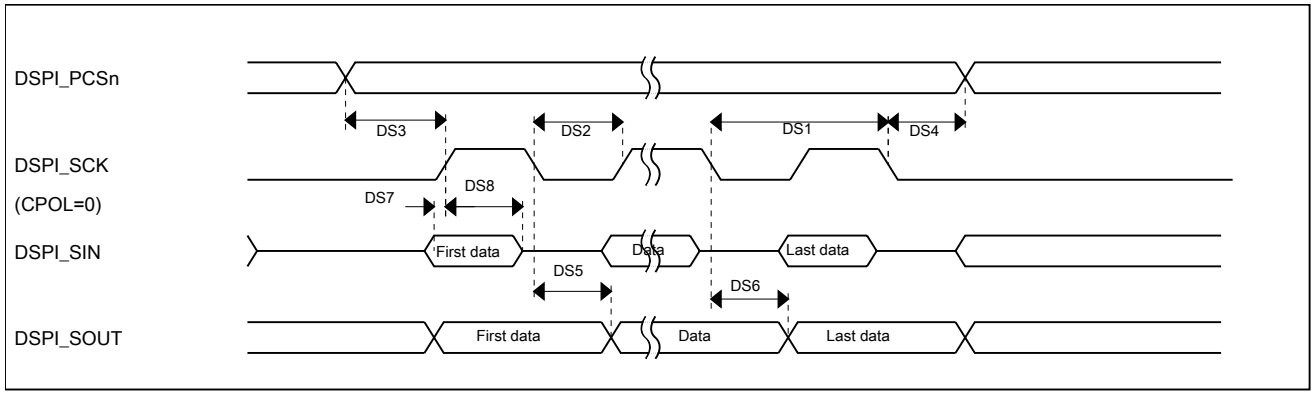


Figure 21. DSPI classic SPI timing — master mode

Table 39. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

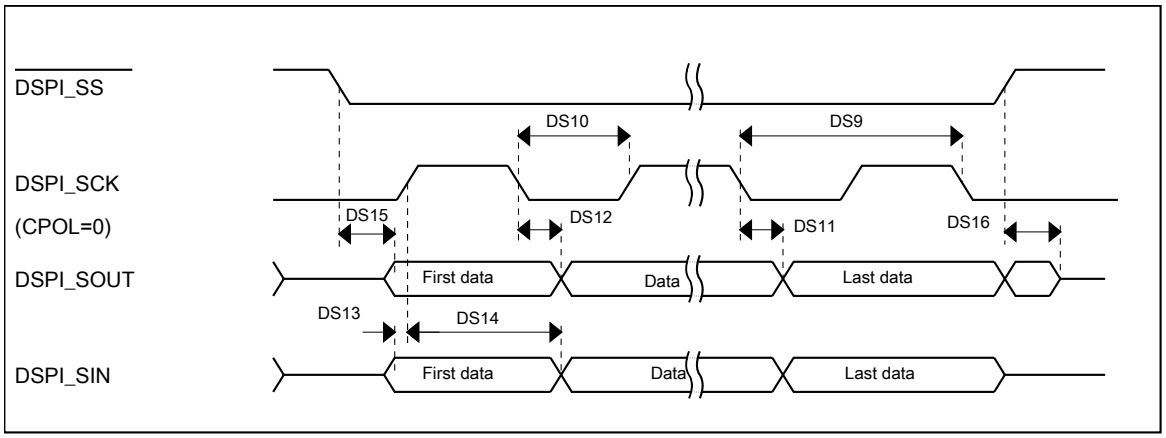


Figure 22. DSPI classic SPI timing — slave mode

Table 47. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	4	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

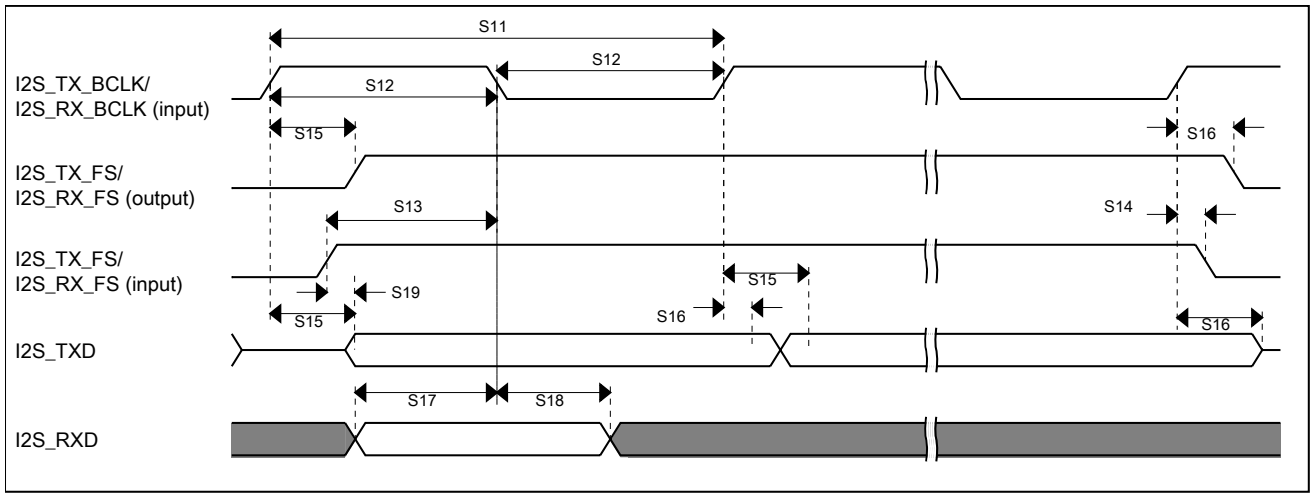


Figure 29. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

121 BGA	100 LQFP	64 LQFP	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J5	32	—	—	PTE25	ADC0_ SE18	ADC0_ SE18	PTE25				I2C0_SDA	EWM_IN		
H6	33	—	—	PTE26/ CLKOUT32 K	DISABLED		PTE26/ CLKOUT32 K					RTC_ CLKOUT	USB_ CLKIN	
J6	34	22	D3	PTA0	JTAG_ TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_ CTS_b	FTM0_CH5				JTAG_ TCLK/ SWD_CLK	EZP_CLK
H8	35	23	D4	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	36	24	E5	PTA2	JTAG_ TDO/ TRACE_ SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_ TDO/ TRACE_ SWO	EZP_DO
H9	37	25	D5	PTA3	JTAG_ TMS/ SWD_DIO		PTA3	UART0_ RTS_b	FTM0_CH0				JTAG_ TMS/ SWD_DIO	
J8	38	26	G5	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	39	27	F5	PTA5	DISABLED		PTA5	USB_ CLKIN	FTM0_CH2			I2S0_TX_ BCLK	JTAG_ TRST_b	
E5	40	—	—	VDD	VDD	VDD								
G3	41	—	—	VSS	VSS	VSS								
K8	42	28	H6	PTA12	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
L8	43	29	G6	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_ FS	FTM1_QD_ PHB	
K9	44	—	—	PTA14	DISABLED		PTA14	SPI0_ PCS0	UART0_TX			I2S0_RX_ BCLK		
L9	45	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
J10	46	—	—	PTA16	DISABLED		PTA16	SPI0_ SOUT	UART0_ CTS_b			I2S0_RX_ FS		
H10	47	—	—	PTA17	ADC1_ SE17	ADC1_ SE17	PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_ MCLK		
L10	48	30	G7	VDD	VDD	VDD								
K10	49	31	H7	VSS	VSS	VSS								
L11	50	32	H8	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_ FLT2	FTM_ CLKIN0				
K11	51	33	G8	PTA19	XTAL0	XTAL0	PTA19		FTM1_ FLT0	FTM_ CLKIN1		LPTMR0_ ALT1		
J11	52	34	F8	RESET_b	RESET_b	RESET_b								
G11	53	35	F7	PTB0/ LLWU_P5	ADC0_ SE8/ ADC1_SE8	ADC0_ SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		

121 BGA	100 LQFP	64 LQFP	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
D7	77	50	A8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0		CMP0_ OUT	FTM0_CH2	
C7	78	51	A7	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_ SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK		I2S0_ MCLK		
B7	79	52	B6	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_ FS				
A7	80	53	A6	PTC8	ADC1_ SE4b/ CMP0_IN2	ADC1_ SE4b/ CMP0_IN2	PTC8			I2S0_ MCLK				
D6	81	54	B5	PTC9	ADC1_ SE5b/ CMP0_IN3	ADC1_ SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_ FLT0		
C6	82	55	B4	PTC10	ADC1_ SE6b	ADC1_ SE6b	PTC10	I2C1_SCL		I2S0_RX_ FS				
C5	83	56	A5	PTC11/ LLWU_P11	ADC1_ SE7b	ADC1_ SE7b	PTC11/ LLWU_P11	I2C1_SDA						
B6	84	—	—	PTC12	DISABLED		PTC12							
A6	85	—	—	PTC13	DISABLED		PTC13							
A5	86	—	—	PTC14	DISABLED		PTC14							
B5	87	—	—	PTC15	DISABLED		PTC15							
F7	88	—	—	VSS	VSS	VSS								
E7	89	—	—	VDD	VDD	VDD								
D5	90	—	—	PTC16	DISABLED		PTC16		LPUART0_ RX					
C4	91	—	—	PTC17	DISABLED		PTC17		LPUART0_ TX					
B4	92	—	—	PTC18	DISABLED		PTC18		LPUART0_ RTS_b					
D4	93	57	C3	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_ PCS0	UART2_ RTS_b			LPUART0_ RTS_b		
D3	94	58	A4	PTD1	ADC0_ SE5b	ADC0_ SE5b	PTD1	SPI0_SCK	UART2_ CTS_b			LPUART0_ CTS_b		
C3	95	59	C2	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_ SOUT	UART2_RX			LPUART0_ RX	I2C0_SCL	
B3	96	60	B3	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX			LPUART0_ TX	I2C0_SDA	
A3	97	61	A3	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_ PCS1	UART0_ RTS_b	FTM0_CH4		EWM_IN	SPI1_ PCS0	
A2	98	62	C1	PTD5	ADC0_ SE6b	ADC0_ SE6b	PTD5	SPI0_ PCS2	UART0_ CTS_b	FTM0_CH5		EWM_ OUT_b	SPI1_SCK	
B2	99	63	B2	PTD6/ LLWU_P15	ADC0_ SE7b	ADC0_ SE7b	PTD6/ LLWU_P15	SPI0_ PCS3	UART0_RX	FTM0_CH6		FTM0_ FLT0	SPI1_ SOUT	
A1	100	64	A2	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7		FTM0_ FLT1	SPI1_SIN	
A11	—	—	—	NC	NC	NC								

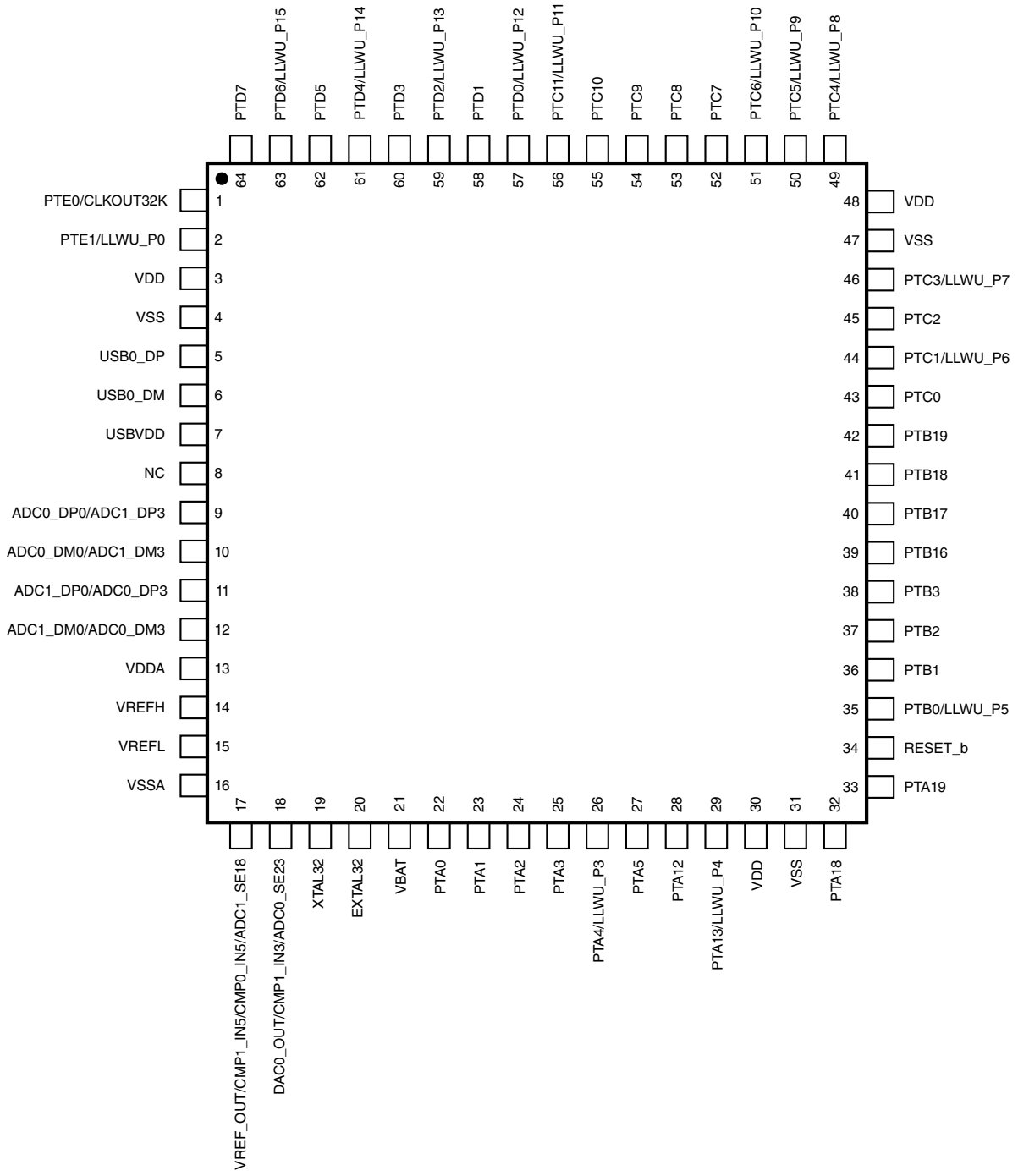


Figure 30. K22 64 LQFP Pinout Diagram (top view)

6.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow, full reel • P = Prequalification • K = Fully qualified, general market flow, 100 piece reel
K##	Kinetis family	• K22
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB • 512 = 512 KB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 XFBGA (8 mm x 8 mm) • DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel

Term	Definition
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

7.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

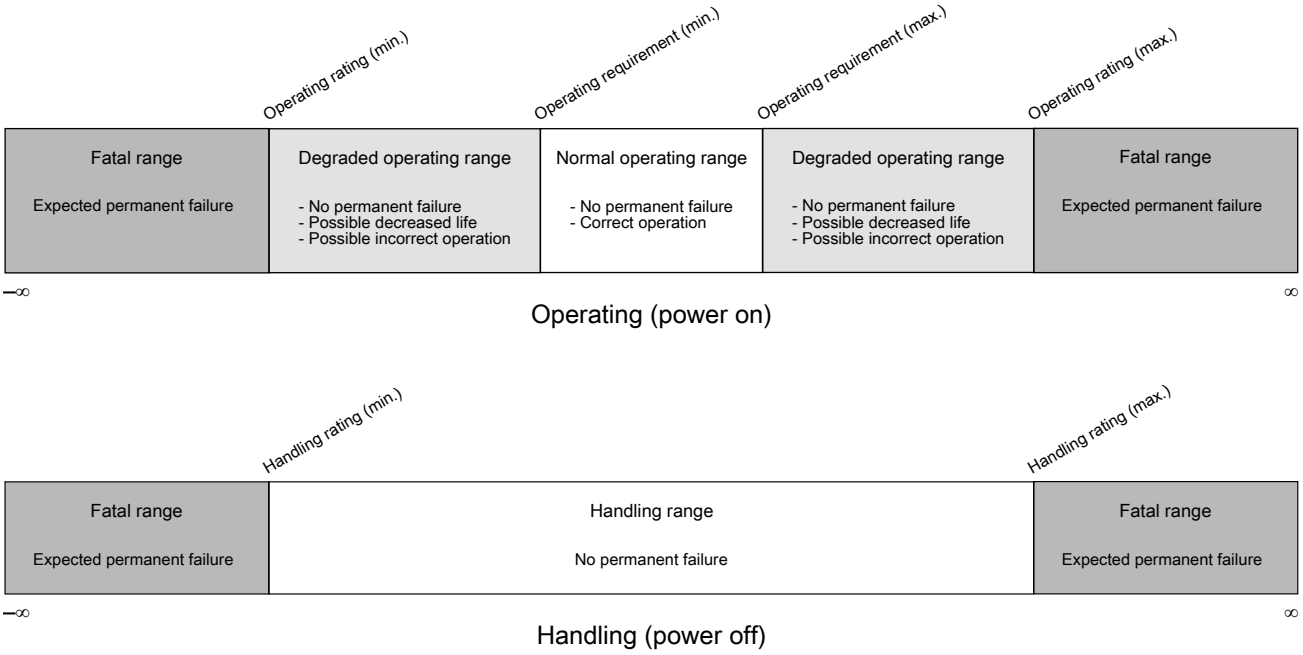
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

7.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

7.4 Relationship between ratings and operating requirements



7.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8 Revision History

The following table provides a revision history for this document.

Table 51. Revision History

Rev. No.	Date	Substantial Changes
7	08/2016	• Added Terminology and Guidelines section • Updated the front matter section • Added Device Revision Number Table • Updated Chip Errata naming convention in Related Resource table
6	10/2015	• In "Power consumption operating behaviors" section, added "Low power mode peripheral adders—typical value" table • In "Thermal operating requirements" table, in footnote, corrected "$T_J = T_A + \Theta_{JA}$" to "$T_J = T_A + R_{\Theta JA}$" • Updated "IRC48M specifications" table • Updated "NVM program/erase timing specifications" table; updated values for $t_{hversall}$ (Erase All high-voltage time) • In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation • Added new section, "Recommended connections for unused analog and digital pins"

5	4/2015	• On page 1:
		  • In first bullet of introduction, updated power consumption data to align with the data in the "Power consumption operating behaviors" table
		  • In second bullet of introduction, added "USB FS device crystal-less functionality"
		  • Under "Communication interfaces," updated I^2C bullet to indicate support for up to 1 Mbps operation
		  • Under "Operating characteristics," specified that voltage range includes flash writes
		• In "Voltage and current operating requirements" table:
		  • Removed content related to positive injection
		  • Updated footnote 1 to say that all analog and I/O pins are internally clamped to V_{SS} only (not V_{SS} and V_{DD})through ESD protection diodes.
		• In"Power consumption operating behaviors" table:
		  • Added additional temperature data in power consumption table
		  • Added Max IDD values based on characterization results equivalent to mean + 3 sigma
		• Updated "EMC radiated emissions operating behaviors" table
		• In "Thermal operating requirements" table, added the following footnote for ambient temperature: "Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + \Theta_{JA}$ x chip power dissipation"
		• Updated "IRC48M Specifications":
		  • Updated maximum values for $\Delta_{firc48m\_ol\_lv}$ and $\Delta_{firc48m\_ol\_hv}$ (full temperature)
		  • Added specifications for $\Delta_{firc48m\_ol\_hv}$ (-40°C to 85°C)
		• Updated notes in "USB electrical specifications" section
		• In "I^2C timing" table,
		  • Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V."
		  • Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 µ
		• Added "I^2C 1 Mbps timing" table
		• Specified that the figure, "K22F 64 LQFP Pinout Diagram" is a top view
		• Specified that the figure, "K22F 64 MAPBGA Pinout Diagram" is a transparent top view
		• Specified that the figure, "K22F 100 LQFP Pinout Diagram" is a top view

Table continues on the next page...

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