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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2500K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FBGA, FC (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/1sx250ln3f43e2lg

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1. Intel® Stratix® 10 GX/SX Device Overview

Intel's 14-nm Intel® Stratix® 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

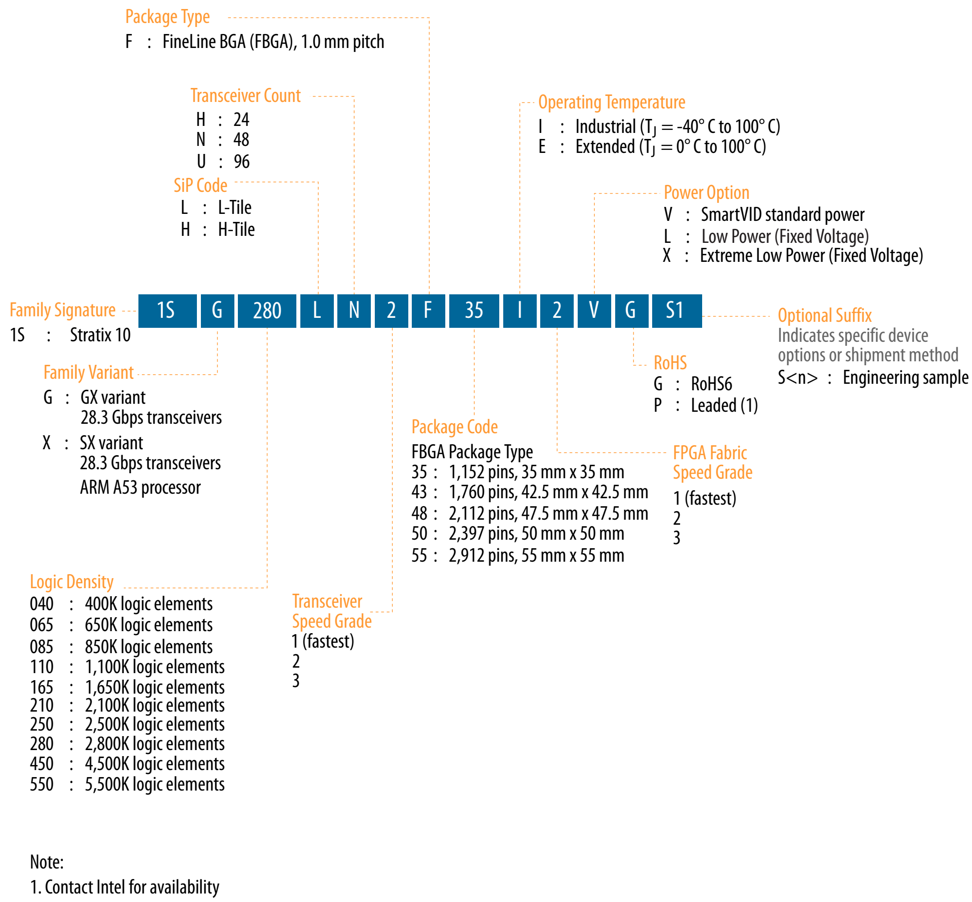
- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.

1.1.1. Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices



1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices

Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Process technology	28-nm TSMC (planar transistor)	14 nm Intel Tri-Gate (FinFET)
Hard processor core	None	Quad-core 64-bit ARM Cortex-A53 (SoC only)
Core architecture	Conventional core architecture with conventional interconnect	HyperFlex core architecture with Hyper-Registers in the interconnect
Core performance	500 MHz	1 GHz
Power dissipation	1x	As low as 0.3x

continued...

- **Additional Hard IP**: Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking**: Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs**: The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

1.3. FPGA and SoC Features Summary

Table 2. Intel Stratix 10 FPGA and SoC Common Device Features

Feature	Description
Technology	• 14-nm Intel Tri-Gate (FinFET) process technology • SmartVID controlled core voltage, standard power devices • 0.85-V fixed core voltage, low static power devices available
Low power serial transceivers	• Up to 96 total transceivers available • Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices • Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)
General purpose I/Os	• Up to 1640 total GPIO available • 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port • DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller) • Multiple hard IP instantiations in each device • Single Root I/O Virtualization (SR-IOV)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols

continued...

Feature	Description
Configuration	• Dedicated Secure Device Manager • Software programmable device configuration • Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication • Physically Unclonable Function (PUF) service
Packaging	• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology • Multiple devices with identical package footprints allows seamless migration across different device densities • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Software and tools	• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • Fast Forward compiler to allow HyperFlex architecture performance exploration • Transceiver toolkit • Platform designer integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Table 3. Intel Stratix 10 SoC Specific Device Features

SoC Subsystem	Feature	Description
Hard Processor System	Multi-processor unit (MPU) core	• Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology • Scalar floating-point unit supporting single and double precision • ARM NEON media processing engine for each processor
	System Controllers	• System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
	Layer 1 Cache	• 32 KB L1 instruction cache with parity • 32 KB L1 data cache with ECC
	Layer 2 Cache	• 1 MB Shared L2 Cache with ECC
	On-Chip Memory	• 256 KB On-Chip RAM
	Direct memory access (DMA) controller	• 8-Channel DMA
	Ethernet media access controller (EMAC)	• Three 10/100/1000 EMAC with integrated DMA
	USB On-The-Go controller (OTG)	• 2 USB OTG with integrated DMA
	UART controller	• 2 UART 16550 compatible
	Serial Peripheral Interface (SPI) controller	• 4 SPI
	I^2C controller	• 5 I^2C controllers
	SD/SDIO/MMC controller	• 1 eMMC version 4.5 with DMA and CE-ATA support • SD, including eSD, version 3.0 • SDIO, including eSDIO, version 3.0 • CE-ATA - version 1.1

continued...

Table 4. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—FPGA Core (part 1)

Intel Stratix 10 GX/SX Device Name	Logic Elements (KLE)	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multi-pliers (1)
GX 400/ SX 400	378	1,537	30	3,204	2	1,296
GX 650/ SX 650	612	2,489	49	5,184	3	2,304
GX 850/ SX 850	841	3,477	68	7,124	4	4,032
GX 1100/ SX 1100	1,092	4,401	86	9,540	6	5,040
GX 1650/ SX 1650	1,624	5,851	114	13,764	8	6,290
GX 2100/ SX 2100	2,005	6,501	127	17,316	11	7,488
GX 2500/ SX 2500	2,422	9,963	195	20,529	13	10,022
GX 2800/ SX 2800	2,753	11,721	229	23,796	15	11,520
GX 4500/ SX 4500	4,463	7,033	137	37,821	23	3,960
GX 5500/ SX 5500	5,510	7,033	137	47,700	29	3,960

Table 5. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—Interconnects, PLLs and Hard IP (part 2)

Intel Stratix 10 GX/SX Device Name	Interconnects		PLLs		Hard IP
	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 400/ SX 400	392	24	8	8	1
GX 650/ SX 650	400	48	16	8	2
GX 850/ SX 850	736	48	16	15	2
GX 1100/ SX 1100	736	48	16	15	2
GX 1650/ SX 1650	704	96	32	14	4
GX 2100/ SX 2100	704	96	32	14	4
GX 2500/ SX 2500	1160	96	32	24	4

continued...

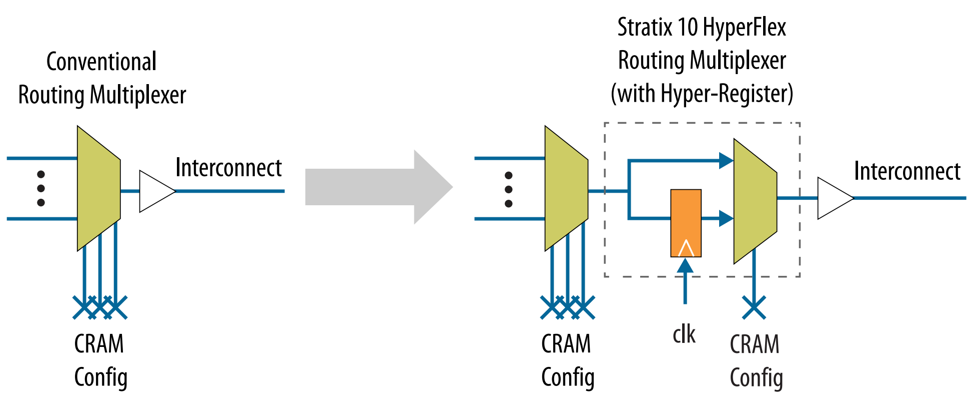
1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 3. Bypassable Hyper-Register



The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

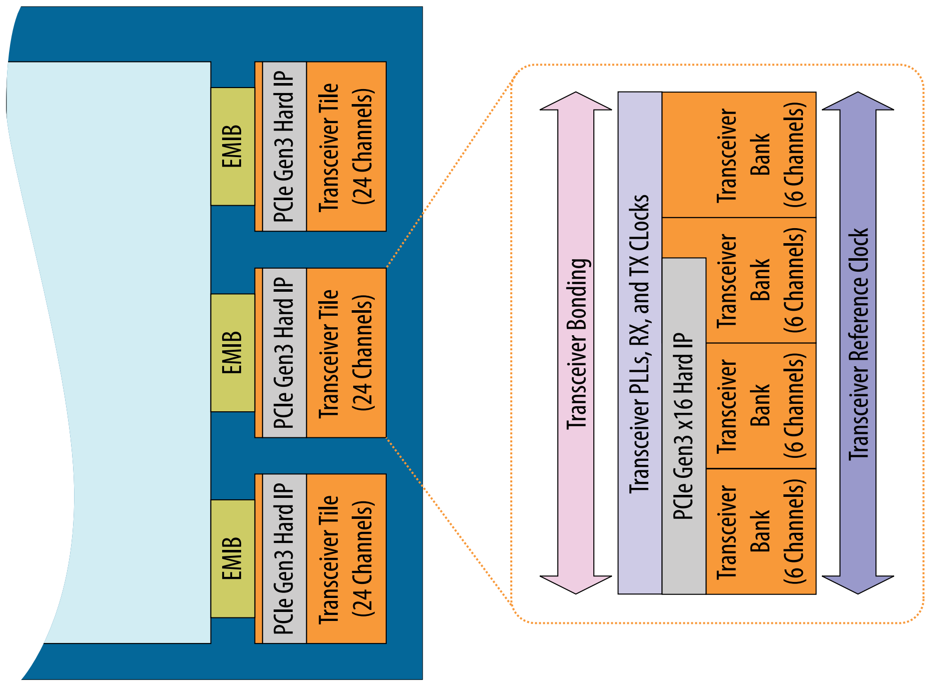
- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

Each transceiver tile contains:

- 24 full-duplex transceiver channels (PMA and PCS)
- Reference clock distribution network
- Transmit PLLs
- High-speed clocking and bonding networks
- One instance of PCI Express hard IP

Figure 6. Heterogeneous 3D SiP Transceiver Tile Architecture



1.8. Intel Stratix 10 Transceivers

Intel Stratix 10 devices offer up to 96 total full-duplex transceiver channels. These channels provide continuous data rates from 1 Gbps to 28.3 Gbps for chip-to-chip, chip-to-module, and backplane applications. In each device,two thirds of the transceivers can be configured up to the maximum data rate of 28.3 Gbps to drive 100G interfaces and C form-factor pluggable CFP2/CFP4 optical modules. For longer-reach backplane driving applications, advanced adaptive equalization circuits are used to equalize over 30 dB of system loss.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

1.8.1. PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- **ATX PLL**—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.
- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.
- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- **Variable Gain Amplifier (VGA)**—to optimize the receiver's dynamic range
- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation
- **Decision Feedback Equalizer (DFE)**—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections
- **On-Die Instrumentation (ODI)**—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing

1.11. 10G Ethernet Hard IP

Intel Stratix 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

The integrated serial transceivers simplify multi-port 10GbE systems compared to 10 GbE Attachment Unit Interface (XAUI) interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated transceivers incorporate signal conditioning circuits, which enable direct connection to standard 10G XFP and SFP+ pluggable optical modules. The transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

1.12. External Memory and General Purpose I/O

Intel Stratix 10 devices offer substantial external memory bandwidth, with up to ten 72-bit wide DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth is provided along with the ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. The external memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers.

Figure 8. Hard Memory Controller

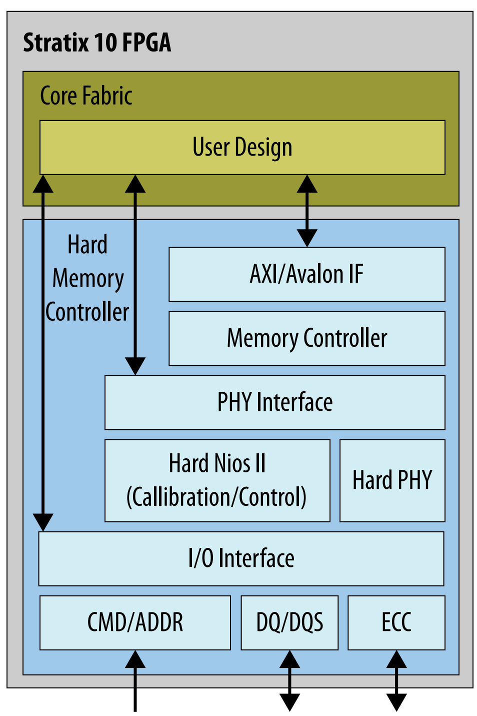
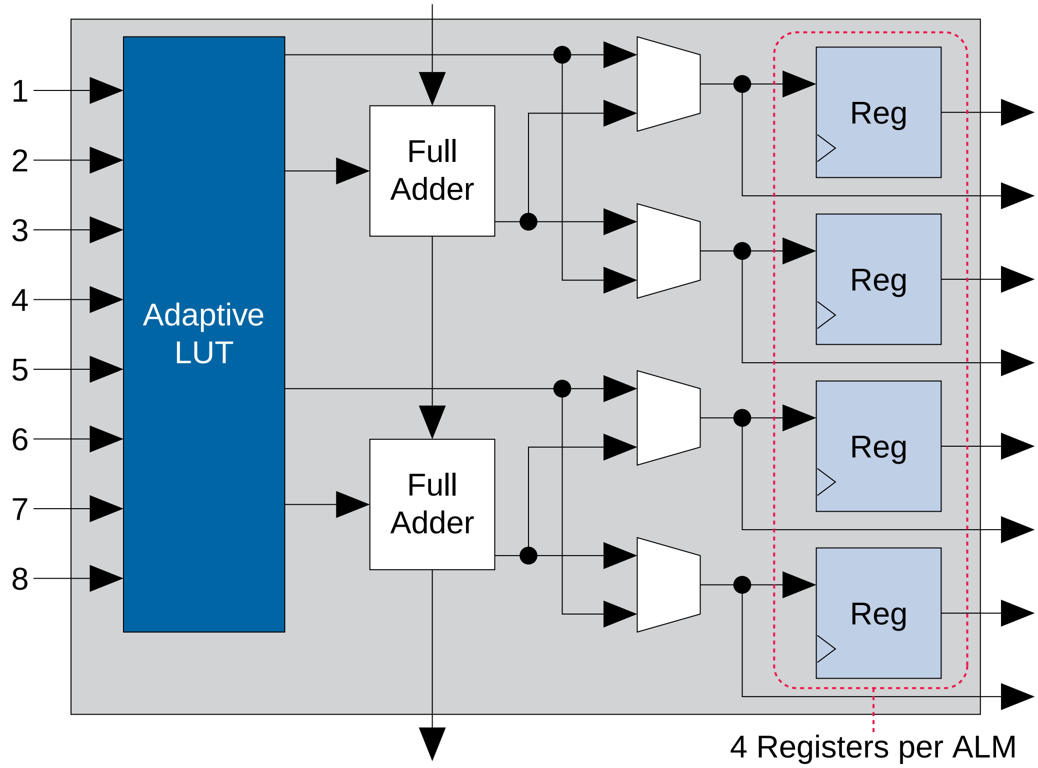


Figure 9. Intel Stratix 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

1.14. Core Clocking

Core clocking in Intel Stratix 10 devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Figure 10. DSP Block: Standard Precision Fixed Point Mode

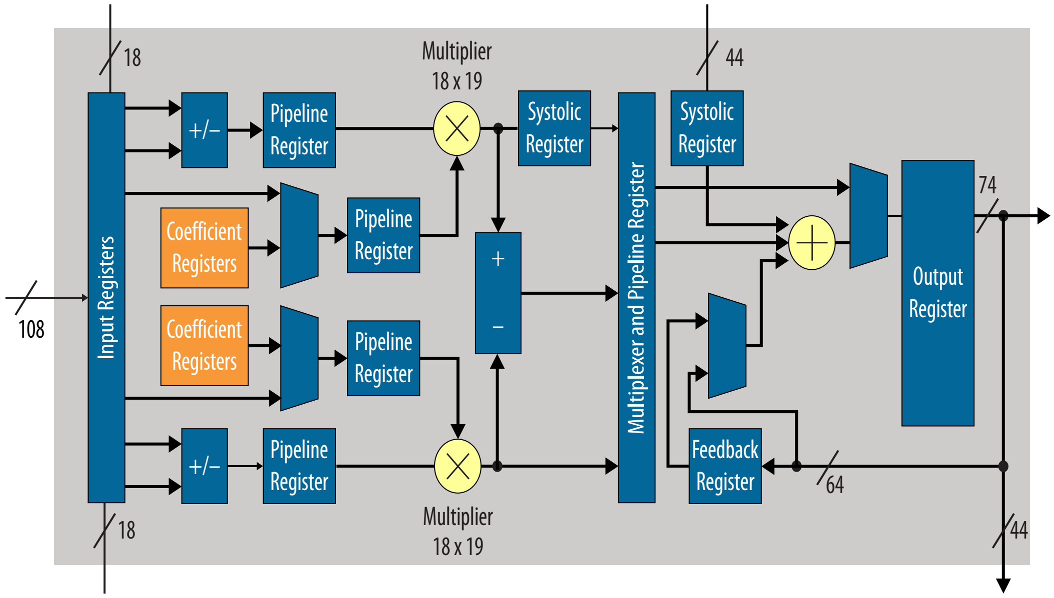


Figure 11. DSP Block: High Precision Fixed Point Mode

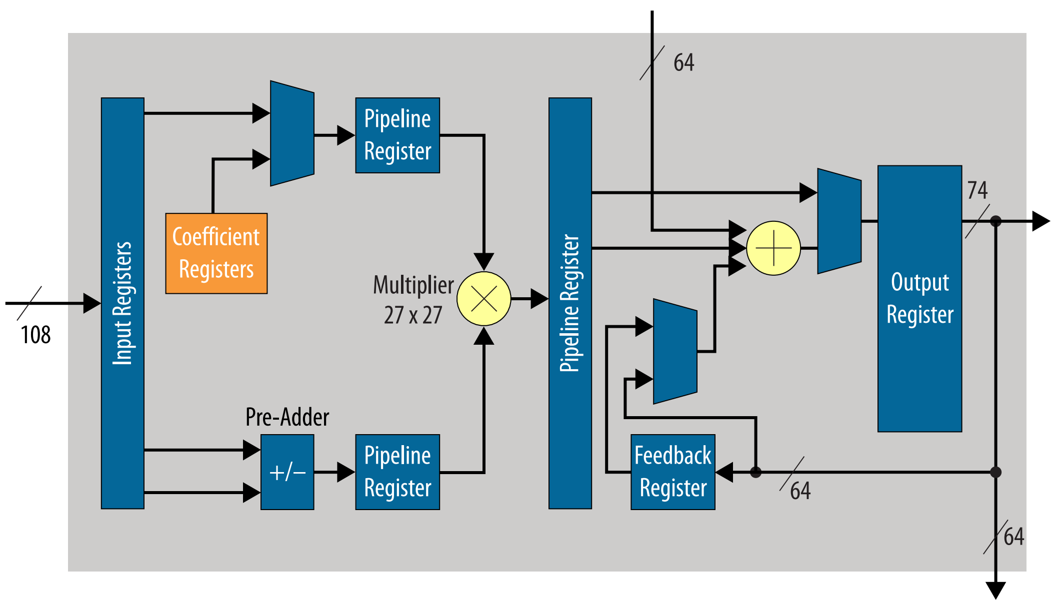
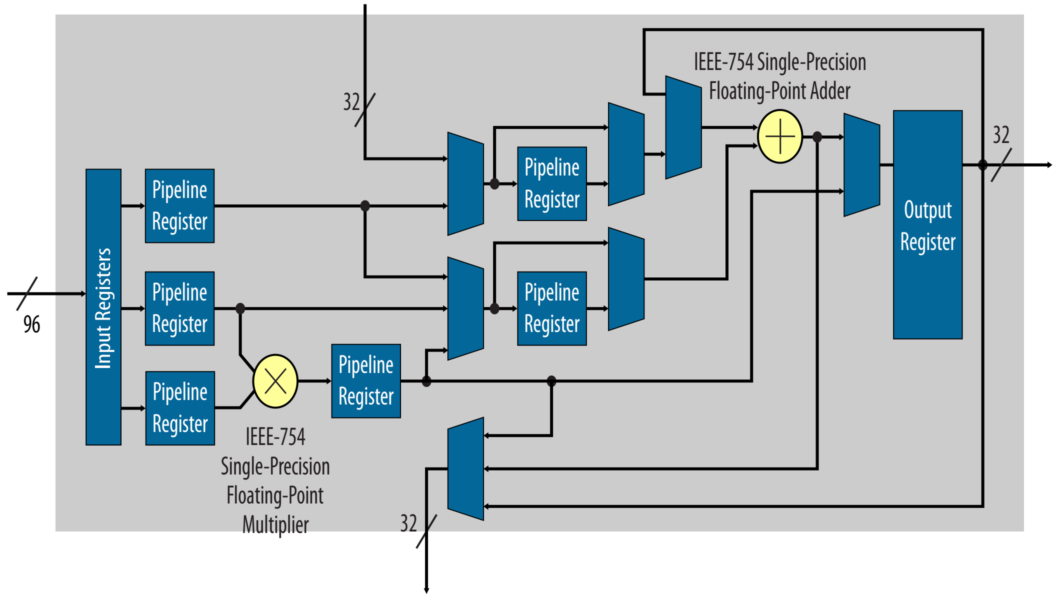


Figure 12. DSP Block: Single Precision Floating Point Mode



Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

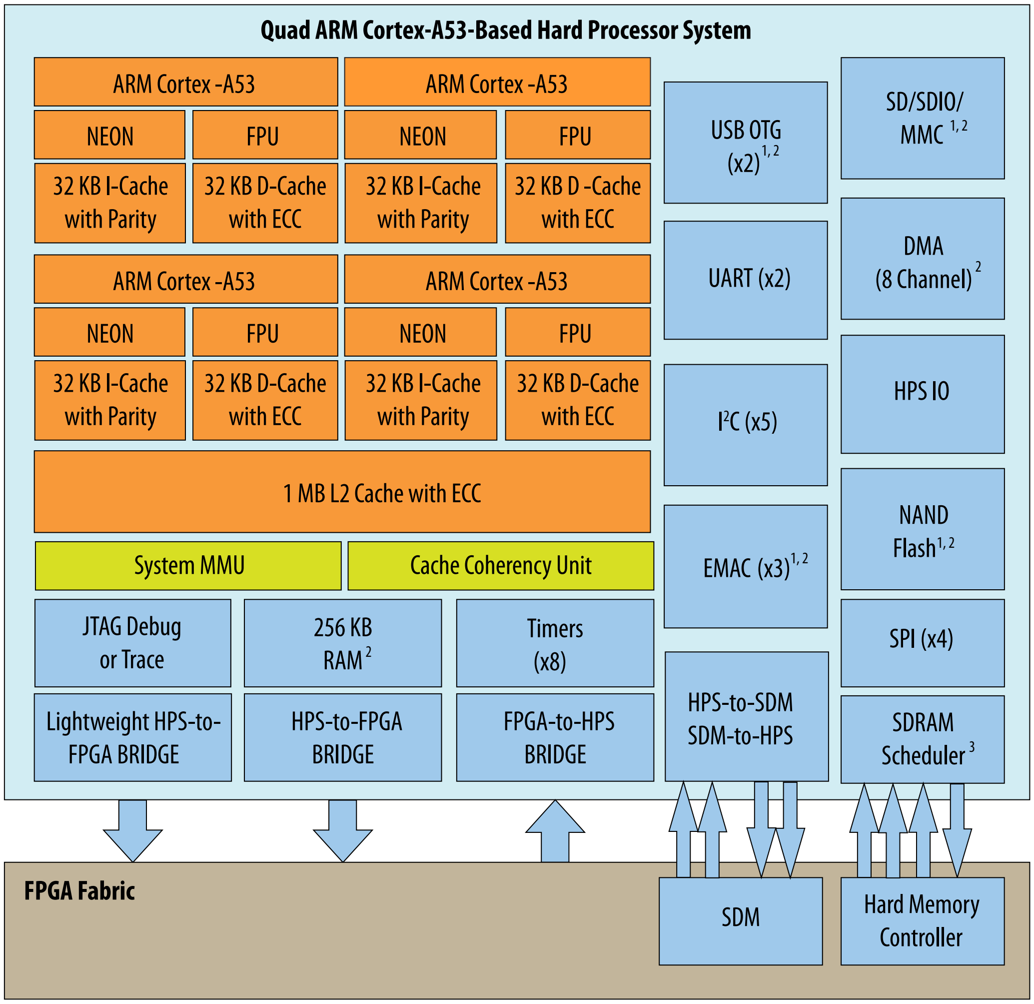
In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 12. Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point
Single Precision floating point	1 Single Precision floating point adder, 1 Single Precision floating point multiplier	Floating point

Figure 13. HPS Block Diagram



Notes:
1. Integrated direct memory access (DMA)
2. Integrated error correction code (ECC)
3. Multiport front-end interface to hard memory controller

1.18.1. Key Features of the Intel Stratix 10 HPS

Table 14. Key Features of the Intel Stratix 10 GX/SX HPS

Feature	Description
Quad-core ARM Cortex-A53 MPCore processor unit	• 2.3 MIPS/MHz instruction efficiency • CPU frequency up to 1.5 GHz • At 1.5 GHz total performance of 13,800 MIPS • ARMv8-A architecture • Runs 64-bit and 32-bit ARM instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Jazelle® RCT execution architecture with 8-bit Java bytecodes

continued...

Feature	Description
	• Superscalar, variable length, out-of-order pipeline with dynamic branch prediction • Improved ARM NEON™ media processing engine • Single- and double-precision floating-point unit • CoreSight™ debug and trace technology
System Memory Management Unit	• Enables a unified memory model and extends hardware virtualization into peripherals implemented in the FPGA fabric
Cache Coherency unit	• Changes in shared data stored in cache are propagated throughout the system providing bi-directional coherency for co-processing elements.
Cache	• L1 Cache — 32 KB of instruction cache w/ parity check — 32 KB of L1 data cache w /ECC — Parity checking • L2 Cache — 1MB shared — 8-way set associative — SEU Protection with parity on TAG ram and ECC on data RAM — Cache lockdown support
On-Chip Memory	• 256 KB of scratch on-chip RAM
External SDRAM and Flash Memory Interfaces for HPS	• Hard memory controller with support for DDR4, DDR3, LPDDR3 — 40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC) — Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies — Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters — Software Configurable Priority Scheduling on individual SDRAM bursts — Fully programmable timing parameter support for all JEDEC-specified timing parameters — Multiport front-end (MPFE) scheduler interface to the hard memory controller, which supports the AXI® Quality of Service (QoS) for interface to the FPGA fabric • NAND flash controller — ONFI 1.0 — Integrated descriptor based with DMA — Programmable hardware ECC support — Support for 8- and 16-bit Flash devices • Secure Digital SD/SDIO/MMC controller — eMMC 4.5 — Integrated descriptor based DMA — CE-ATA digital commands supported — 50 MHz operating frequency • Direct memory access (DMA) controller — 8-channel — Supports up to 32 peripheral handshake interface

continued...

1.19. Power Management

Intel Stratix 10 devices leverage the advanced Intel 14-nm Tri-Gate process technology, the all new HyperFlex core architecture to enable Hyper-Folding, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

With the new HyperFlex core architecture, designs can run 2X faster than previous generation FPGAs. With 2X performance and same required throughput, architects can cut the data path width in half to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

The optional power reduction techniques in Intel Stratix 10 devices include:

- **Available Low Static Power Devices**—Intel Stratix 10 devices are available with a fixed core voltage that provides lower static power than the SmartVID standard power devices, while maintaining device performance

Furthermore, Intel Stratix 10 devices feature Intel’s industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

1.20. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.

The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be

The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 14-nm Tri-Gate process technology used for Intel Stratix 10 devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

1.26. Document Revision History for the Intel Stratix 10 GX/SX Device Overview

Document Version	Changes
2018.08.08	Made the following changes: • Changed the specs for QDRII+ and QDRII+ Xtreme and added specs for QDRIV in the "External Memory Interface Performance" table. • Updated description of the power options in the "Sample Ordering COde and Available Options for Intel Stratix 10 Devices" figure. • Changed the description of the technology and power management features in the "Intel Stratix 10 FPGA and SoC Common Device Features" table. • Changed the description of SmartVID in the "Power Management" section. • Changed the direction arrow from the coefficient registers block in the "DSP Block: High Precision Fixed Point Mode" figure.
2017.10.30	Made the following changes: • Removed the embedded eSRAM feature globally. • Removed the Low Power (VID) and Military operating temperature options, and package code 53 from the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure. • Changed the Maximum transceiver data rate (chip-to-chip) specification for L-Tile devices in the "Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices" table.
2016.10.31	Made the following changes: • Changed the number of available transceivers to 96, globally. • Changed the single-precision floating point performance to 10 TeraFLOPS, globally. • Changed the maximum datarate to 28.3 Gbps, globally. • Changed some of the features listed in the "Stratix 10 GX/SX Device Overview" section. • Changed descriptions for the GX and SX devices in the "Stratix 10 Family Variants" section. • Changed the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure.

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Document Version	Changes
	• Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table. • Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table: — Transceiver hard IP — Internal memory blocks — Core clock networks — Packaging • Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section. • Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section. • Removed footnotes from the "Transceiver PCS Features" table. • Changed the HMC description in the "External Memory and General Purpose I/O" section. • Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section. • Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table. • Changed the description in the "Internal Embedded Memory" section. • Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table. • Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section. • Updated the "Key Features of the Stratix 10 HPS" table. • Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table. • Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table.
2015.12.04	Initial release.