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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Quad ARM® Cortex®-A53 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 2500K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 2397-BBGA, FCBGA |
| Supplier Device Package | 2397-FBGA, FC (50x50) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/1sx250lu2f50i2vg |

# Contents

# 1. Intel® Stratix® 10 GX/SX Device Overview

Intel's 14-nm Intel® Stratix® 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

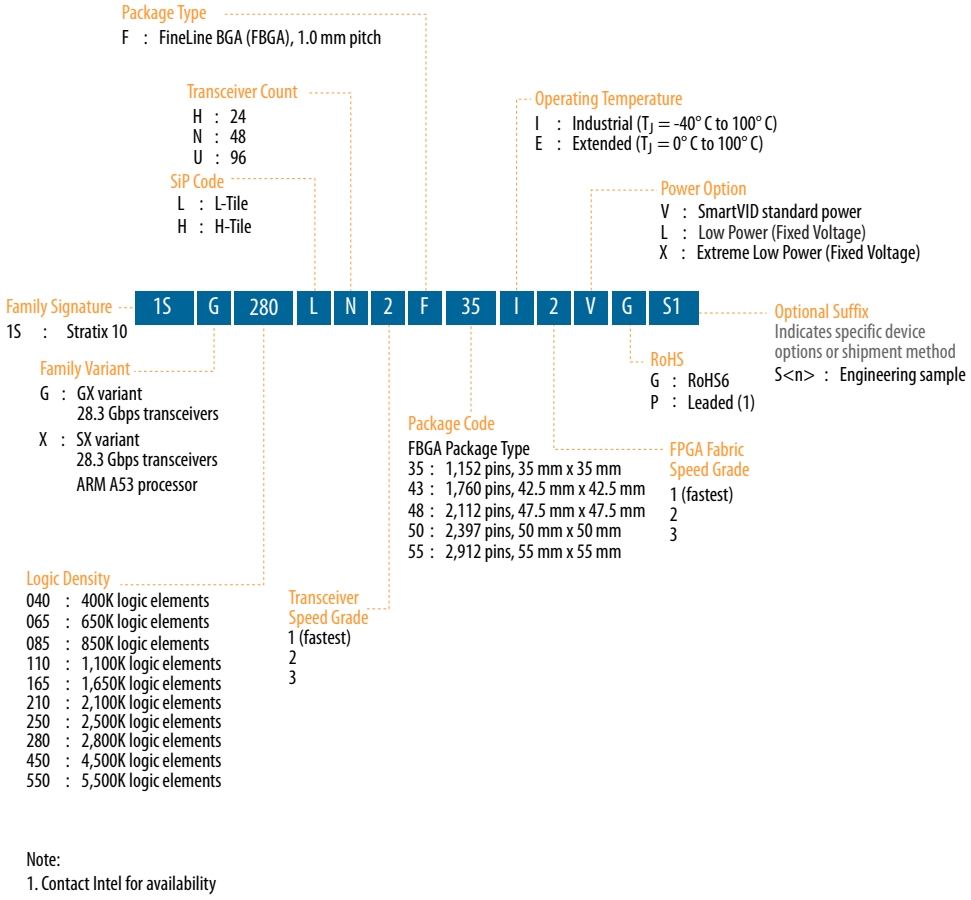
- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.

### 1.1.1. Available Options

**Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices**




## 1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

**Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices**

| Feature | Stratix V FPGAs | Intel Stratix 10 FPGAs and SoCs |
|---|---|---|
| **Process technology** | 28-nm TSMC (planar transistor) | 14 nm Intel Tri-Gate (FinFET) |
| **Hard processor core** | None | Quad-core 64-bit ARM Cortex-A53 (SoC only) |
| **Core architecture** | Conventional core architecture with conventional interconnect | HyperFlex core architecture with Hyper-Registers in the interconnect |
| **Core performance** | 500 MHz | 1 GHz |
| **Power dissipation** | 1x | As low as 0.3x |

*continued...*

| Feature | Stratix V FPGAs | Intel Stratix 10 FPGAs and SoCs |
|---|---|---|
| **Logic density** | 952 KLE (monolithic) | 5,500 KLE (monolithic) |
| **Embedded memory (M20K)** | 52 Mbits | 229 Mbits |
| **18x19 multipliers** | 3,926<br>*Note:* Multiplier is 18x18 in Stratix V devices. | 11,520<br>*Note:* Multiplier is 18x19 in Intel Stratix 10 devices. |
| **Floating point DSP capability** | Up to 1 TFLOP, requires soft floating point adder and multiplier | Up to 10 TFLOPS, hard IEEE 754 compliant single precision floating point adder and multiplier |
| **Maximum transceivers** | 66 | 96 |
| **Maximum transceiver data rate (chip-to-chip)** | 28.05 Gbps | 28.3 Gbps L-Tile<br>28.3 Gbps H-Tile |
| **Maximum transceiver data rate (backplane)** | 12.5 Gbps | 12.5 Gbps L-Tile<br>28.3 Gbps H-Tile |
| **Hard memory controller** | None | DDR4 @ 1333 MHz/2666 Mbps<br>DDR3 @ 1067 MHz/2133 Mbps |
| **Hard protocol IP** | PCIe Gen3 x8 (up to 4 instances) | PCIe Gen3 x16 (up to 4 instances)<br>SR-IOV (4 physical functions / 2k virtual functions) on H-Tile devices<br>10GBASE-KR/40GBASE-KR4 FEC |
| **Core clocking and PLLs** | Global, quadrant and regional clocks supported by fractional-synthesis fPLLs | Programmable clock tree synthesis supported by fractional synthesis fPLLs and integer IO PLLs |
| **Register state readback and writeback** | Not available | Non-destructive register state readback and writeback for ASIC prototyping and other applications |

These innovations result in the following improvements:

- **Improved Core Logic Performance**: The HyperFlex core architecture combined with Intel's 14-nm Tri-Gate technology allows Intel Stratix 10 devices to achieve 2X the core performance compared to the previous generation
- **Lower Power**: Intel Stratix 10 devices use up to 70% lower power compared to the previous generation, enabled by 14-nm Intel Tri-Gate technology, the HyperFlex core architecture, and optional power saving features built into the architecture
- **Higher Density**: Intel Stratix 10 devices offer over five times the level of integration, with up to 5,500K logic elements (LEs) in a monolithic fabric, over 229 Mbits of embedded memory blocks (M20K), and 11,520 18x19 multipliers
- **Embedded Processing**: Intel Stratix 10 SoCs feature a Quad-Core 64-bit ARM Cortex-A53 processor optimized for power efficiency and software compatible with previous generation Arria and Cyclone SoC devices
- **Improved Transceiver Performance**: With up to 96 transceiver channels implemented in heterogeneous 3D SiP transceiver tiles, Intel Stratix 10 GX and SX devices support data rates up to 28.3 Gbps chip-to-chip and 28.3 Gbps across the backplane with signal conditioning circuits capable of equalizing over 30 dB of system loss
- **Improved DSP Performance**: The variable precision DSP block in Intel Stratix 10 devices features hard fixed and floating point capability, with up to 10 TeraFLOPS IEEE754 single-precision floating point performance

- **Additional Hard IP**: Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking**: Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs**: The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

## 1.3. FPGA and SoC Features Summary

**Table 2. Intel Stratix 10 FPGA and SoC Common Device Features**

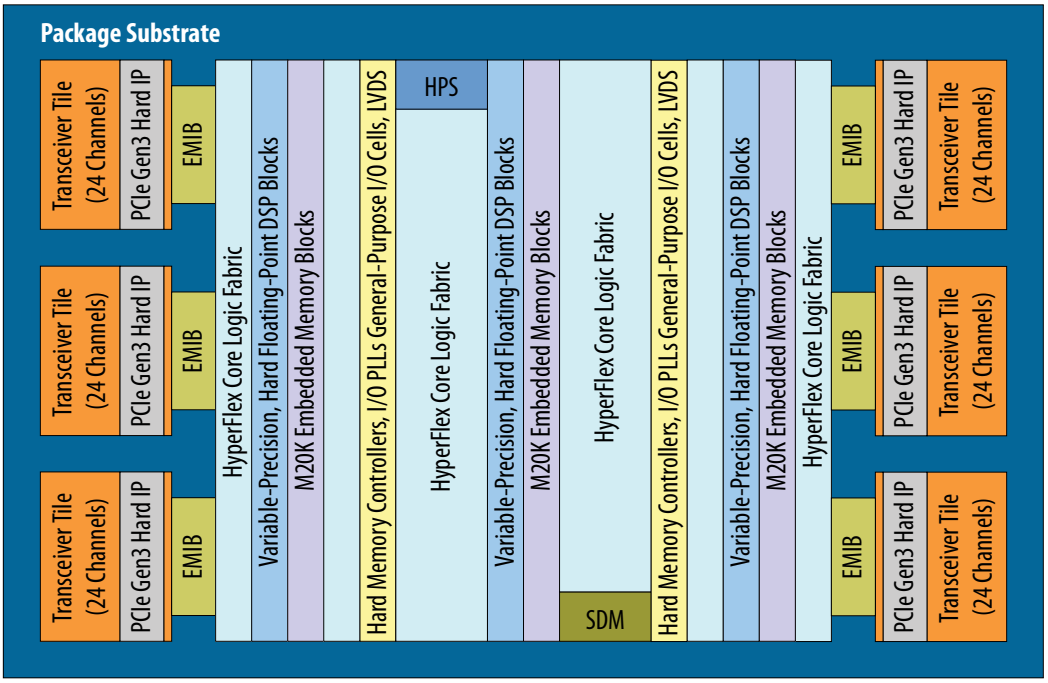
| Feature | Description |
|---|---|
| Technology | • 14-nm Intel Tri-Gate (FinFET) process technology<br>• SmartVID controlled core voltage, standard power devices<br>• 0.85-V fixed core voltage, low static power devices available |
| Low power serial transceivers | • Up to 96 total transceivers available<br>• Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices<br>• Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices<br>• Extended range down to 125 Mbps with oversampling<br>• ATX transmit PLLs with user-configurable fractional synthesis capability<br>• XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support<br>• Adaptive linear and decision feedback equalization<br>• Transmit pre-emphasis and de-emphasis<br>• Dynamic partial reconfiguration of individual transceiver channels<br>• On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring) |
| General purpose I/Os | • Up to 1640 total GPIO available<br>• 1.6 Gbps LVDS—every pair can be configured as an input or output<br>• 1333 MHz/2666 Mbps DDR4 external memory interface<br>• 1067 MHz/2133 Mbps DDR3 external memory interface<br>• 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing<br>• On-chip termination (OCT) |
| Embedded hard IP | • PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port<br>• DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller)<br>• Multiple hard IP instantiations in each device<br>• Single Root I/O Virtualization (SR-IOV) |
| Transceiver hard IP | • 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)<br>• 10G Ethernet PCS<br>• PCI Express PIPE interface<br>• Interlaken PCS<br>• Gigabit Ethernet PCS<br>• Deterministic latency support for Common Public Radio Interface (CPRI) PCS<br>• Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS<br>• 8B/10B, 64B/66B, 64B/67B encoders and decoders<br>• Custom mode support for proprietary protocols |

*continued...*

| SoC Subsystem | Feature | Description |
|---|---|---|
| | NAND flash controller | • 1 ONFI 1.0, 8- and 16-bit support |
| | General-purpose I/O (GPIO) | • Maximum of 48 software programmable GPIO |
| | Timers | • 4 general-purpose timers<br>• 4 watchdog timers |
| **Secure Device Manager** | Security | • Secure boot<br>• Advanced Encryption Standard (AES) and authentication (SHA/ECDSA) |
| **External Memory Interface** | External Memory Interface | • Hard Memory Controller with DDR4 and DDR3, and LPDDR3 |

## 1.4. Intel Stratix 10 Block Diagram

**Figure 2. Intel Stratix 10 FPGA and SoC Architecture Block Diagram**




HPS: Quad ARM Cortex-A53 Hard Processor System
SDM: Secure Device Manager
EMIB: Embedded Multi-Die Interconnect Bridge

## 1.5. Intel Stratix 10 FPGA and SoC Family Plan

(1) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

**Table 4. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—FPGA Core (part 1)**

| Intel Stratix 10 GX/SX Device Name | Logic Elements (KLE) | M20K Blocks | M20K Mbits | MLAB Counts | MLAB Mbits | 18x19 Multipliers (1) |
|---|---|---|---|---|---|---|
| GX 400/ SX 400 | 378 | 1,537 | 30 | 3,204 | 2 | 1,296 |
| GX 650/ SX 650 | 612 | 2,489 | 49 | 5,184 | 3 | 2,304 |
| GX 850/ SX 850 | 841 | 3,477 | 68 | 7,124 | 4 | 4,032 |
| GX 1100/ SX 1100 | 1,092 | 4,401 | 86 | 9,540 | 6 | 5,040 |
| GX 1650/ SX 1650 | 1,624 | 5,851 | 114 | 13,764 | 8 | 6,290 |
| GX 2100/ SX 2100 | 2,005 | 6,501 | 127 | 17,316 | 11 | 7,488 |
| GX 2500/ SX 2500 | 2,422 | 9,963 | 195 | 20,529 | 13 | 10,022 |
| GX 2800/ SX 2800 | 2,753 | 11,721 | 229 | 23,796 | 15 | 11,520 |
| GX 4500/ SX 4500 | 4,463 | 7,033 | 137 | 37,821 | 23 | 3,960 |
| GX 5500/ SX 5500 | 5,510 | 7,033 | 137 | 47,700 | 29 | 3,960 |

**Table 5. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—Interconnects, PLLs and Hard IP (part 2)**

| Intel Stratix 10 GX/SX Device Name | Interconnects | | PLLs | | Hard IP |
|---|---|---|---|---|---|
| | Maximum GPIOs | Maximum XCVR | fPLLs | I/O PLLs | PCIe Hard IP Blocks |
| GX 400/ SX 400 | 392 | 24 | 8 | 8 | 1 |
| GX 650/ SX 650 | 400 | 48 | 16 | 8 | 2 |
| GX 850/ SX 850 | 736 | 48 | 16 | 15 | 2 |
| GX 1100/ SX 1100 | 736 | 48 | 16 | 15 | 2 |
| GX 1650/ SX 1650 | 704 | 96 | 32 | 14 | 4 |
| GX 2100/ SX 2100 | 704 | 96 | 32 | 14 | 4 |
| GX 2500/ SX 2500 | 1160 | 96 | 32 | 24 | 4 |

*continued...*

| Intel Stratix 10 GX/SX Device Name | F1152 HF35 (35x35 mm²) | F1760 NF43 (42.5x42.5 mm²) | F1760 NF43 (42.5x42.5 mm²) |
|---|---|---|---|
| SX 2800 | | | |
| GX 4500/ SX 4500 | | | |
| GX 5500/ SX 5500 | | | |

**Table 7. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 2**

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers (2) (3) (4) (5) (6) (7)

| Intel Stratix 10 GX/SX Device Name | F2112 NF48 (47.5x47.5 mm²) | F2397 UF50 (50x50 mm²) | F2912 HF55 (55x55 mm²) |
|---|---|---|---|
| GX 400/ SX 400 | | | |
| GX 650/ SX 650 | | | |
| GX 850/ SX 850 | 736, 16, 360, 48 | | |
| GX 1100/ SX 1100 | 736, 16, 360, 48 | | |
| GX 1650/ SX 1650 | | 704, 32, 336, 96 | |
| GX 2100/ SX 2100 | | 704, 32, 336, 96 | |
| GX 2500/ SX 2500 | | 704, 32, 336, 96 | 1160, 8, 576, 24 |
| GX 2800/ SX 2800 | | 704, 32, 336, 96 | 1160, 8, 576, 24 |
| GX 4500/ SX 4500 | | | 1640, 8, 816, 24 |
| GX 5500/ SX 5500 | | | 1640, 8, 816, 24 |

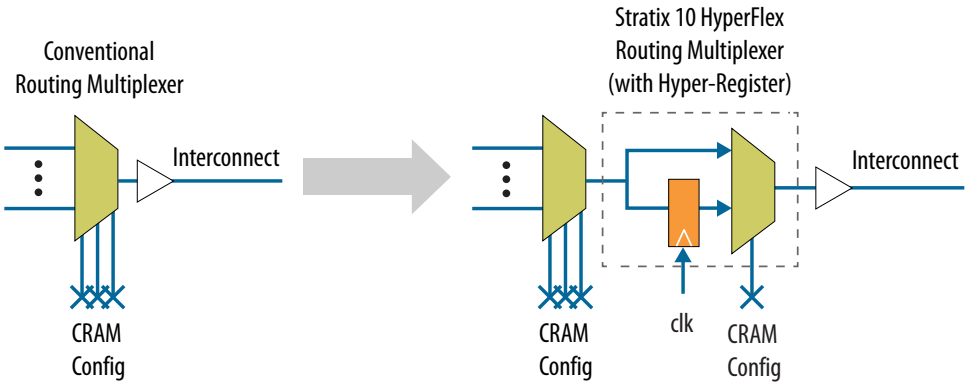
## 1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

**Figure 3. Bypassable Hyper-Register**

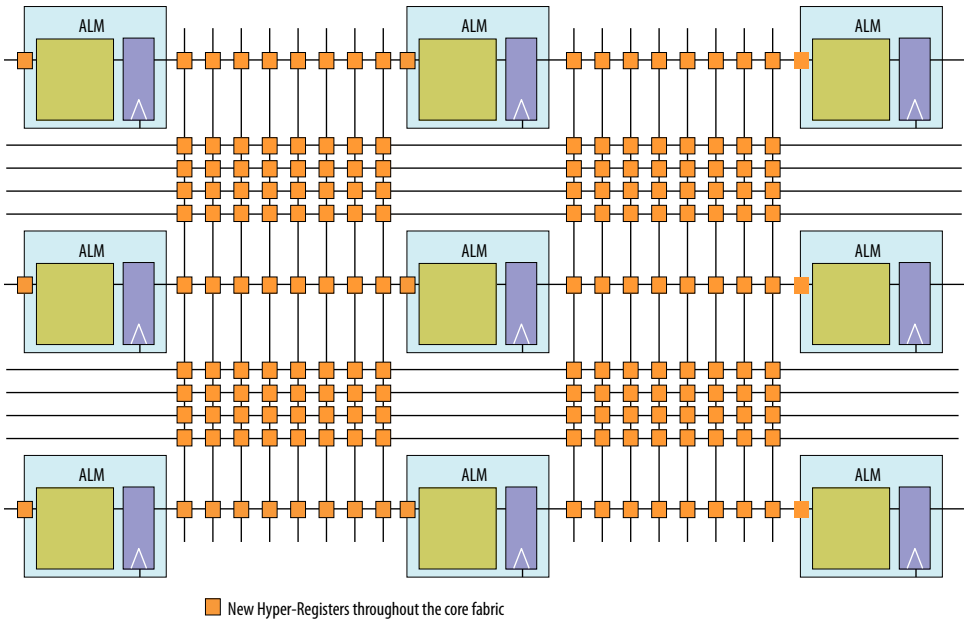



The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

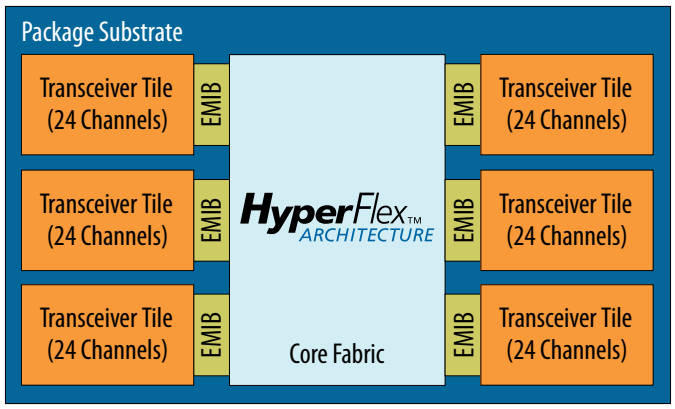
**Figure 4. HyperFlex Core Architecture**




## 1.7. Heterogeneous 3D SiP Transceiver Tiles

Intel Stratix 10 FPGAs and SoCs feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles, each containing 24 full-duplex transceiver channels. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

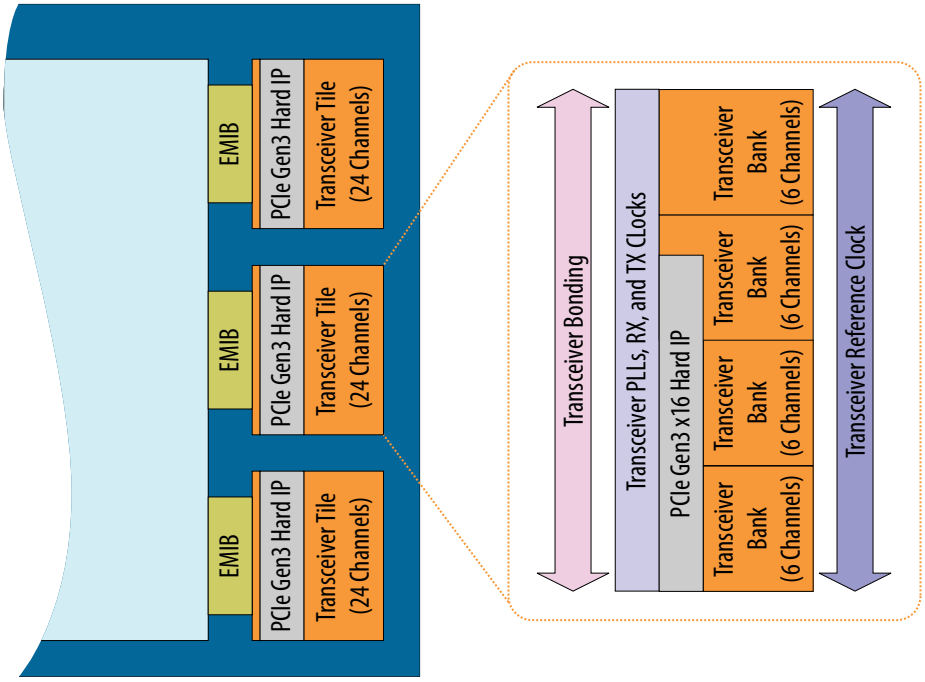
**Figure 5. Monolithic Core Fabric and Heterogeneous 3D SiP Transceiver Tiles**



Each transceiver tile contains:

- 24 full-duplex transceiver channels (PMA and PCS)
- Reference clock distribution network
- Transmit PLLs
- High-speed clocking and bonding networks
- One instance of PCI Express hard IP

**Figure 6. Heterogeneous 3D SiP Transceiver Tile Architecture**




## 1.8. Intel Stratix 10 Transceivers

Intel Stratix 10 devices offer up to 96 total full-duplex transceiver channels. These channels provide continuous data rates from 1 Gbps to 28.3 Gbps for chip-to-chip, chip-to-module, and backplane applications. In each device,two thirds of the transceivers can be configured up to the maximum data rate of 28.3 Gbps to drive 100G interfaces and C form-factor pluggable CFP2/CFP4 optical modules. For longer-reach backplane driving applications, advanced adaptive equalization circuits are used to equalize over 30 dB of system loss.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

| PCS Protocol Support | Data Rate (Gbps) | Transmitter Data Path | Receiver Data Path |
|---|---|---|---|
| Enhanced PCS | 2.5 to 17.4 | FIFO, channel bonding, bit-slipper, and gear box | FIFO, block sync, bit-slipper, and gear box |
| 10GBASE-R | 10.3125 | FIFO, 64B/66B encoder, scrambler, FEC, and gear box | FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box |
| Interlaken | 4.9 to 17.4 | FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box | FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box |
| SFI-S/SFI-5.2 | 11.3 | FIFO, channel bonding, bit-slipper, and gear box | FIFO, bit-slipper, and gear box |
| IEEE 1588 | 1.25 to 10.3125 | FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box | FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box |
| SDI | up to 12.5 | FIFO and gear box | FIFO, bit-slipper, and gear box |
| GigE | 1.25 | Same as Standard PCS plus GigE state machine | Same as Standard PCS plus GigE state machine |
| PCS Direct | up to 28.3 | Custom | Custom |

**Related Information**

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

## 1.9. PCI Express Gen1/Gen2/Gen3 Hard IP

Intel Stratix 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, increased functionality, and designer productivity.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers. It also supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8/x16 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic (autonomous mode). This feature allows the PCI Express link to power up and complete link training in less than 100 ms, while the rest of the device is still in the process of being configured. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

The PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the device via protocol (CvP) across the PCI Express bus at Gen1/Gen2/Gen3 rates.

## 1.10. Interlaken PCS Hard IP

Intel Stratix 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Intel Stratix 10 devices.

Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

**Table 10. External Memory Interface Performance**

The listed speeds are for the 1-rank case.

| Interface | Controller Type | Performance |
|---|---|---|
| DDR4 | Hard | 2666 Mbps |
| DDR3 | Hard | 2133 Mbps |
| QDRII+ | Soft | 1,100 Mtps |
| QDRII+ Xtreme | Soft | 1,266 Mtps |
| QDRIV | Soft | 2,133 Mtps |
| RLDRAM III | Soft | 2400 Mbps |
| RLDRAM II | Soft | 533 Mbps |

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

## 1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

**Figure 10. DSP Block: Standard Precision Fixed Point Mode**

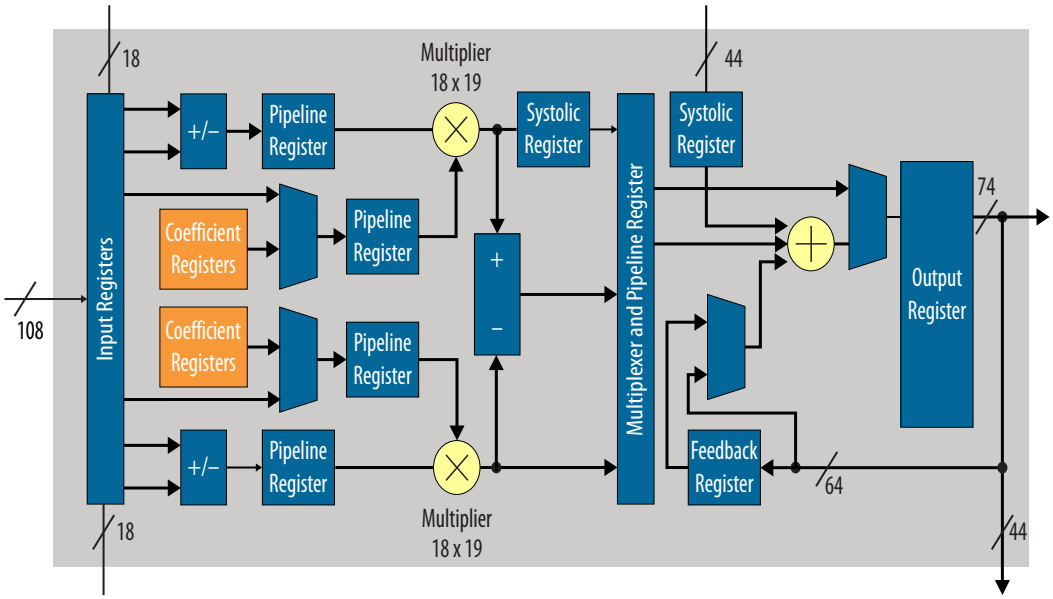



**Figure 11. DSP Block: High Precision Fixed Point Mode**

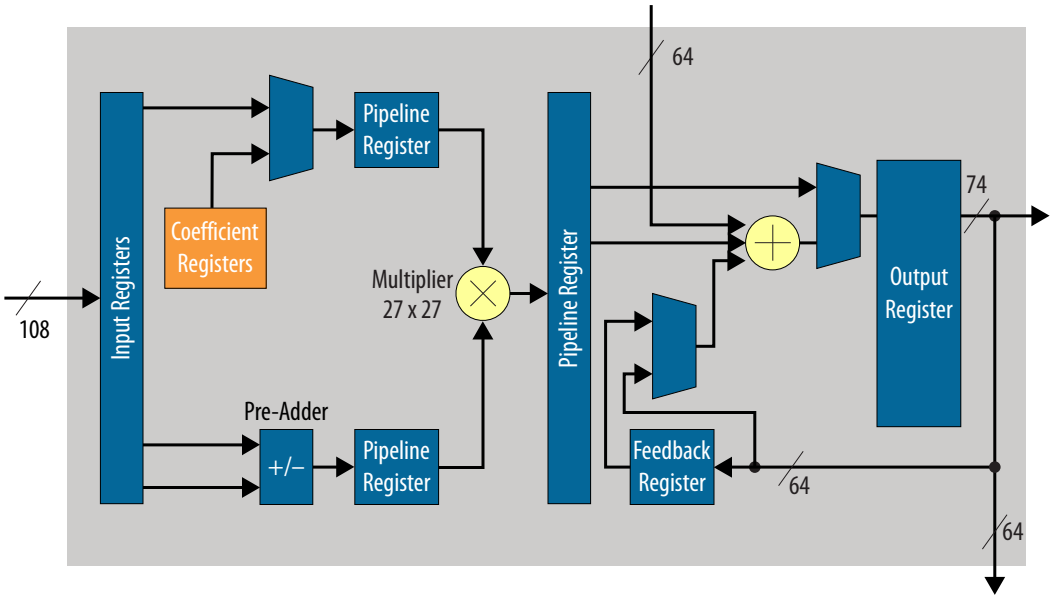
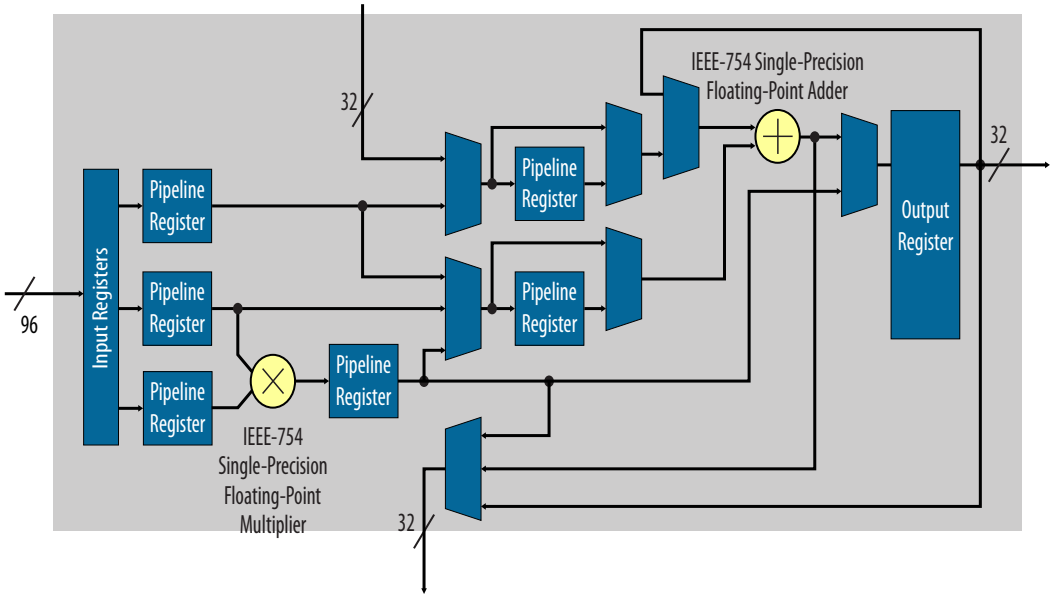


**Figure 12. DSP Block: Single Precision Floating Point Mode**




Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

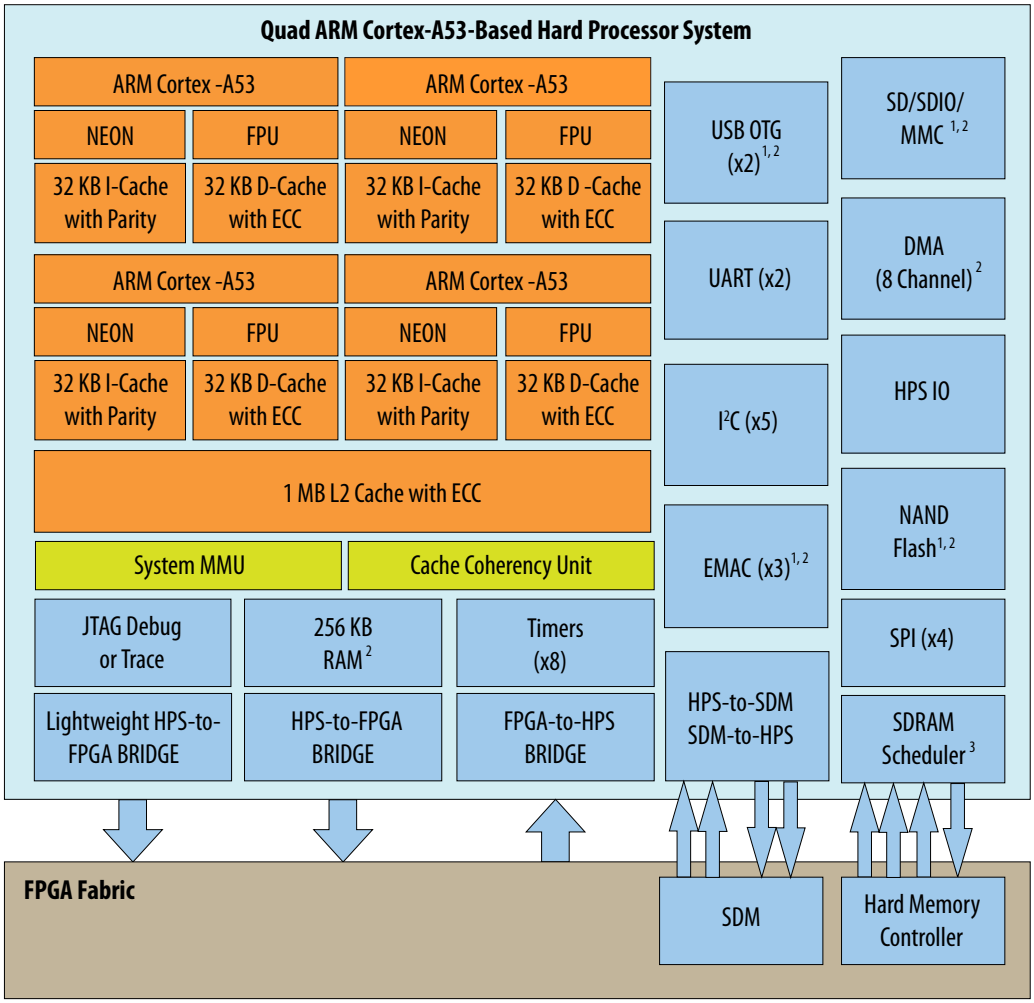
In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

**Table 12. Variable Precision DSP Block Configurations**

| Multiplier Size | DSP Block Resources | Expected Usage |
|---|---|---|
| 18x19 bits | 1/2 of Variable Precision DSP Block | Medium precision fixed point |
| 27x27 bits | 1 Variable Precision DSP Block | High precision fixed point |
| 19x36 bits | 1 Variable Precision DSP Block with external adder | Fixed point FFTs |
| 36x36 bits | 2 Variable Precision DSP Blocks with external adder | Very high precision fixed point |
| 54x54 bits | 4 Variable Precision DSP Blocks with external adder | Double Precision floating point |
| Single Precision floating point | 1 Single Precision floating point adder, 1 Single Precision floating point multiplier | Floating point |

**Figure 13. HPS Block Diagram**




Notes:
1. Integrated direct memory access (DMA)
2. Integrated error correction code (ECC)
3. Multiport front-end interface to hard memory controller

## 1.18.1. Key Features of the Intel Stratix 10 HPS

**Table 14. Key Features of the Intel Stratix 10 GX/SX HPS**

| Feature | Description |
|---|---|
| Quad-core ARM Cortex-A53 MPCore processor unit | • 2.3 MIPS/MHz instruction efficiency<br>• CPU frequency up to 1.5 GHz<br>• At 1.5 GHz total performance of 13,800 MIPS<br>• ARMv8-A architecture<br>• Runs 64-bit and 32-bit ARM instructions<br>• 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint<br>• Jazelle® RCT execution architecture with 8-bit Java bytecodes |

*continued...*

| Feature | Description |
|---|---|
| Communication Interface Controllers | • Three 10/100/1000 Ethernet media access controls (MAC) with integrated DMA<br>— Supports RGMII and RMII external PHY Interfaces<br>— Option to support other PHY interfaces through FPGA logic<br>• GMII<br>• MII<br>• RMII (requires MII to RMII adapter)<br>• RGMII (requires GMII to RGMII adapter)<br>• SGMII (requires GMII to SGMII adapter)<br>— Supports IEEE 1588-2002 and IEEE 1588-2008 standards for precision networked clock synchronization<br>— Supports IEEE 802.1Q VLAN tag detection for reception frames<br>— Supports Ethernet AVB standard<br>• Two USB On-the-Go (OTG) controllers with DMA<br>— Dual-Role Device (device and host functions)<br>• High-speed (480 Mbps)<br>• Full-speed (12 Mbps)<br>• Low-speed (1.5 Mbps)<br>• Supports USB 1.1 (full-speed and low-speed)<br>— Integrated descriptor-based scatter-gather DMA<br>— Support for external ULPI PHY<br>— Up to 16 bidirectional endpoints, including control endpoint<br>— Up to 16 host channels<br>— Supports generic root hub<br>— Configurable to OTG 1.3 and OTG 2.0 modes<br>• Five $I^2C$ controllers (three can be used by EMAC for MIO to external PHY)<br>— Support both 100Kbps and 400Kbps modes<br>— Support both 7-bit and 10-bit addressing modes<br>— Support Master and Slave operating mode<br>• Two UART 16550 compatible<br>— Programmable baud rate up to 115.2Kbaud<br>• Four serial peripheral interfaces (SPI) (2 Master, 2 Slaves)<br>— Full and Half duplex |
| Timers and I/O | • Timers<br>— 4 general-purpose timers<br>— 4 watchdog timers<br>• 48 HPS direct I/O allow HPS peripherals to connect directly to I/O<br>• Up to three IO48 banks may be assigned to HPS for HPS DDR access |
| Interconnect to Logic Core | • FPGA-to-HPS Bridge<br>— Allows IP bus masters in the FPGA fabric to access to HPS bus slaves<br>— Configurable 32-, 64-, or 128-bit AMBA AXI interface<br>• HPS-to-FPGA Bridge<br>— Allows HPS bus masters to access bus slaves in FPGA fabric<br>— Configurable 32-, 64-, or 128-bit AMBA AXI interface allows high-bandwidth HPS master transactions to FPGA fabric<br>• HPS-to-SDM and SDM-to-HPS Bridges<br>— Allows the HPS to reach the SDM block and the SDM to bootstrap the HPS<br>• Light Weight HPS-to-FPGA Bridge<br>— Light weight 32-bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in FPGA fabric<br>• FPGA-to-HPS SDRAM Bridge<br>— Up to three AMBA AXI interfaces supporting 32, 64, or 128-bit data paths |

The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

## 1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

## 1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be

The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 14-nm Tri-Gate process technology used for Intel Stratix 10 devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

## 1.26. Document Revision History for the Intel Stratix 10 GX/SX Device Overview

| Document Version | Changes |
|---|---|
| 2018.08.08 | Made the following changes:<br>• Changed the specs for QDRII+ and QDRII+ Xtreme and added specs for QDRIV in the "External Memory Interface Performance" table.<br>• Updated description of the power options in the "Sample Ordering COde and Available Options for Intel Stratix 10 Devices" figure.<br>• Changed the description of the technology and power management features in the "Intel Stratix 10 FPGA and SoC Common Device Features" table.<br>• Changed the description of SmartVID in the "Power Management" section.<br>• Changed the direction arrow from the coefficient registers block in the "DSP Block: High Precision Fixed Point Mode" figure. |
| 2017.10.30 | Made the following changes:<br>• Removed the embedded eSRAM feature globally.<br>• Removed the Low Power (VID) and Military operating temperature options, and package code 53 from the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure.<br>• Changed the Maximum transceiver data rate (chip-to-chip) specification for L-Tile devices in the "Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices" table. |
| 2016.10.31 | Made the following changes:<br>• Changed the number of available transceivers to 96, globally.<br>• Changed the single-precision floating point performance to 10 TeraFLOPS, globally.<br>• Changed the maximum datarate to 28.3 Gbps, globally.<br>• Changed some of the features listed in the "Stratix 10 GX/SX Device Overview" section.<br>• Changed descriptions for the GX and SX devices in the "Stratix 10 Family Variants" section.<br>• Changed the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure. |

*continued...*