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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2500K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2397-BBGA, FCBGA
Supplier Device Package	2397-FBGA, FC (50x50)
Purchase URL	https://www.e-xfl.com/product-detail/intel/1sx250lu3f50e2lg

- Dedicated secure device manager (SDM) for:
  - Enhanced device configuration and security
  - AES-256, SHA-256/384 and ECDSA-256/384 encrypt/decrypt accelerators and authentication
  - Multi-factor authentication
  - Physically Unclonable Function (PUF) service and software programmable device configuration capability
- Comprehensive set of advanced power saving features delivering up to 70% lower power compared to previous generation high-performance FPGAs
- Non-destructive register state readback and writeback, to support ASIC prototyping and other applications

With these capabilities, Intel Stratix 10 FPGAs and SoCs are ideally suited for the most demanding applications in diverse markets such as:

- **Compute and Storage**—for custom servers, cloud computing and data center acceleration
- **Networking**—for Terabit, 400G and multi-100G bridging, aggregation, packet processing and traffic management
- **Optical Transport Networks**—for OTU4, 2xOTU4, 4xOTU4
- **Broadcast**—for high-end studio distribution, headend encoding/decoding, edge quadrature amplitude modulation (QAM)
- **Military**—for radar, electronic warfare, and secure communications
- **Medical**—for diagnostic scanners and diagnostic imaging
- **Test and Measurement**—for protocol and application testers
- **Wireless**—for next-generation 5G networks
- **ASIC Prototyping**—for designs that require the largest monolithic FPGA fabric with the highest I/O count

1.1. Intel Stratix 10 Family Variants

Intel Stratix 10 devices are available in FPGA (GX) and SoC (SX) variants.

- **Intel Stratix 10 GX** devices deliver up to 1 GHz core fabric performance and contain up to 5.5 million LEs in a monolithic fabric. They also feature up to 96 general purpose transceivers on separate transceiver tiles, and 2666 Mbps DDR4 external memory interface performance. The transceivers are capable of up to 28.3 Gbps short reach and across the backplane. These devices are optimized for FPGA applications that require the highest transceiver bandwidth and core fabric performance, with the power efficiency of Intel's industry-leading 14-nm Tri-Gate process technology.
- **Intel Stratix 10 SX** devices have a feature set that is identical to Intel Stratix 10 GX devices, with the addition of an embedded quad-core 64-bit ARM Cortex A53 hard processor system.

Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Logic density	952 KLE (monolithic)	5,500 KLE (monolithic)
Embedded memory (M20K)	52 Mbits	229 Mbits
18x19 multipliers	3,926 *Note:* Multiplier is 18x18 in Stratix V devices.	11,520 *Note:* Multiplier is 18x19 in Intel Stratix 10 devices.
Floating point DSP capability	Up to 1 TFLOP, requires soft floating point adder and multiplier	Up to 10 TFLOPS, hard IEEE 754 compliant single precision floating point adder and multiplier
Maximum transceivers	66	96
Maximum transceiver data rate (chip-to-chip)	28.05 Gbps	28.3 Gbps L-Tile 28.3 Gbps H-Tile
Maximum transceiver data rate (backplane)	12.5 Gbps	12.5 Gbps L-Tile 28.3 Gbps H-Tile
Hard memory controller	None	DDR4 @ 1333 MHz/2666 Mbps DDR3 @ 1067 MHz/2133 Mbps
Hard protocol IP	PCIe Gen3 x8 (up to 4 instances)	PCIe Gen3 x16 (up to 4 instances) SR-IOV (4 physical functions / 2k virtual functions) on H-Tile devices 10GBASE-KR/40GBASE-KR4 FEC
Core clocking and PLLs	Global, quadrant and regional clocks supported by fractional-synthesis fPLLs	Programmable clock tree synthesis supported by fractional synthesis fPLLs and integer IO PLLs
Register state readback and writeback	Not available	Non-destructive register state readback and writeback for ASIC prototyping and other applications

These innovations result in the following improvements:

- **Improved Core Logic Performance**: The HyperFlex core architecture combined with Intel's 14-nm Tri-Gate technology allows Intel Stratix 10 devices to achieve 2X the core performance compared to the previous generation
- **Lower Power**: Intel Stratix 10 devices use up to 70% lower power compared to the previous generation, enabled by 14-nm Intel Tri-Gate technology, the HyperFlex core architecture, and optional power saving features built into the architecture
- **Higher Density**: Intel Stratix 10 devices offer over five times the level of integration, with up to 5,500K logic elements (LEs) in a monolithic fabric, over 229 Mbits of embedded memory blocks (M20K), and 11,520 18x19 multipliers
- **Embedded Processing**: Intel Stratix 10 SoCs feature a Quad-Core 64-bit ARM Cortex-A53 processor optimized for power efficiency and software compatible with previous generation Arria and Cyclone SoC devices
- **Improved Transceiver Performance**: With up to 96 transceiver channels implemented in heterogeneous 3D SiP transceiver tiles, Intel Stratix 10 GX and SX devices support data rates up to 28.3 Gbps chip-to-chip and 28.3 Gbps across the backplane with signal conditioning circuits capable of equalizing over 30 dB of system loss
- **Improved DSP Performance**: The variable precision DSP block in Intel Stratix 10 devices features hard fixed and floating point capability, with up to 10 TeraFLOPS IEEE754 single-precision floating point performance

- **Additional Hard IP**: Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking**: Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs**: The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

1.3. FPGA and SoC Features Summary

Table 2. Intel Stratix 10 FPGA and SoC Common Device Features

Feature	Description
Technology	• 14-nm Intel Tri-Gate (FinFET) process technology • SmartVID controlled core voltage, standard power devices • 0.85-V fixed core voltage, low static power devices available
Low power serial transceivers	• Up to 96 total transceivers available • Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices • Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)
General purpose I/Os	• Up to 1640 total GPIO available • 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port • DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller) • Multiple hard IP instantiations in each device • Single Root I/O Virtualization (SR-IOV)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols

continued...

Feature	Description
Power management	• SmartVID controlled core voltage, standard power devices • 0.85-V fixed core voltage, low static power devices available • Intel Quartus® Prime Pro Edition integrated power analysis
High performance monolithic core fabric	• HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks • Monolithic fabric minimizes compile times and increases logic utilization • Enhanced adaptive logic module (ALM) • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture with programmable clock tree synthesis • Fine-grained partial reconfiguration
Internal memory blocks	• M20K—20-Kbit with hard ECC support • MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	• IEEE 754-compliant hard single-precision floating point capability • Supports signal processing with precision ranging from 18x19 up to 54x54 • Native 27x27 and 18x19 multiply modes • 64-bit accumulator and cascade for systolic FIRs • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • Additional pipeline register increases performance and reduces power
Phase locked loops (PLL)	• Fractional synthesis PLLs (fPLL) support both fractional and integer modes • Fractional mode with third-order delta-sigma modulation • Precision frequency synthesis • Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering
Core clock networks	• 1 GHz fabric clocking • 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface • 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface • Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks • Clocks only synthesized where needed, to minimize dynamic power

continued...

Feature	Description
Configuration	• Dedicated Secure Device Manager • Software programmable device configuration • Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication • Physically Unclonable Function (PUF) service
Packaging	• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology • Multiple devices with identical package footprints allows seamless migration across different device densities • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Software and tools	• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • Fast Forward compiler to allow HyperFlex architecture performance exploration • Transceiver toolkit • Platform designer integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Table 3. Intel Stratix 10 SoC Specific Device Features

SoC Subsystem	Feature	Description
Hard Processor System	Multi-processor unit (MPU) core	• Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology • Scalar floating-point unit supporting single and double precision • ARM NEON media processing engine for each processor
	System Controllers	• System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
	Layer 1 Cache	• 32 KB L1 instruction cache with parity • 32 KB L1 data cache with ECC
	Layer 2 Cache	• 1 MB Shared L2 Cache with ECC
	On-Chip Memory	• 256 KB On-Chip RAM
	Direct memory access (DMA) controller	• 8-Channel DMA
	Ethernet media access controller (EMAC)	• Three 10/100/1000 EMAC with integrated DMA
	USB On-The-Go controller (OTG)	• 2 USB OTG with integrated DMA
	UART controller	• 2 UART 16550 compatible
	Serial Peripheral Interface (SPI) controller	• 4 SPI
	I^2C controller	• 5 I^2C controllers
	SD/SDIO/MMC controller	• 1 eMMC version 4.5 with DMA and CE-ATA support • SD, including eSD, version 3.0 • SDIO, including eSDIO, version 3.0 • CE-ATA - version 1.1

continued...

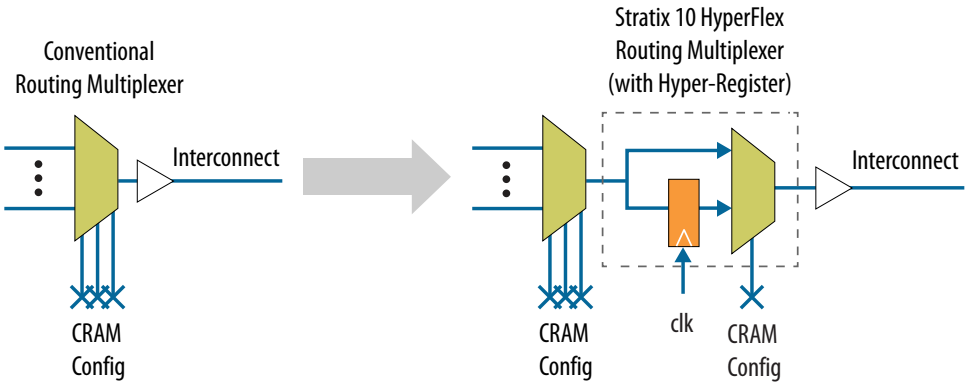
1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 3. Bypassable Hyper-Register

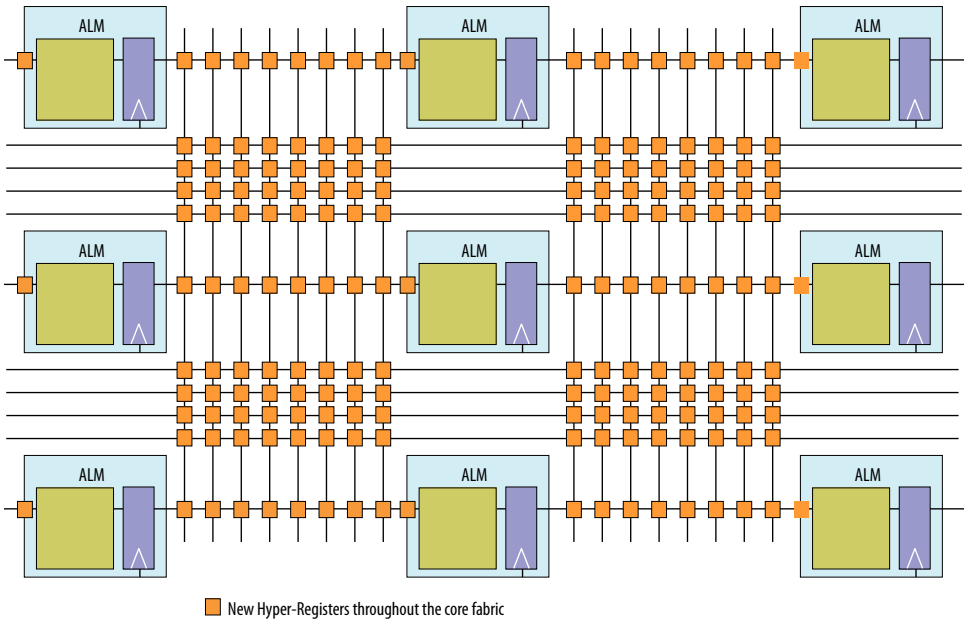


The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

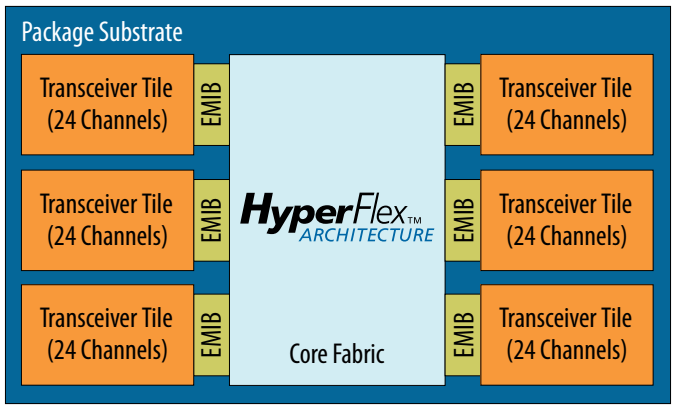
Figure 4. HyperFlex Core Architecture



1.7. Heterogeneous 3D SiP Transceiver Tiles

Intel Stratix 10 FPGAs and SoCs feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles, each containing 24 full-duplex transceiver channels. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

Figure 5. Monolithic Core Fabric and Heterogeneous 3D SiP Transceiver Tiles



Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

1.8.1. PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

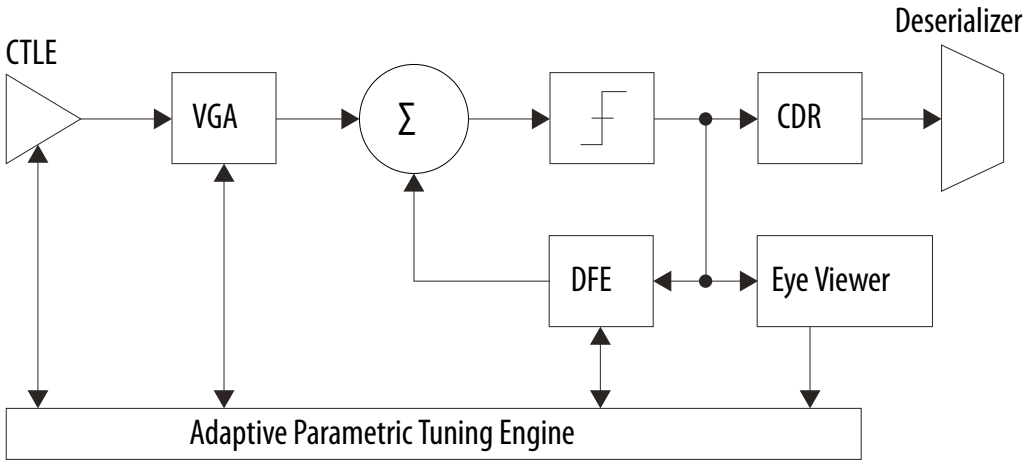
Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- **ATX PLL**—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.
- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.
- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- **Variable Gain Amplifier (VGA)**—to optimize the receiver's dynamic range
- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation
- **Decision Feedback Equalizer (DFE)**—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections
- **On-Die Instrumentation (ODI)**—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing

Figure 7. Intel Stratix 10 Receiver Block Features



All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

Table 8. Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps [8] to 28.3 Gbps (Intel Stratix 10 GX/SX devices)
Backplane Support	

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 12.5	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.3	Custom	Custom

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

1.9. PCI Express Gen1/Gen2/Gen3 Hard IP

Intel Stratix 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, increased functionality, and designer productivity.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers. It also supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8/x16 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic (autonomous mode). This feature allows the PCI Express link to power up and complete link training in less than 100 ms, while the rest of the device is still in the process of being configured. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

The PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the device via protocol (CvP) across the PCI Express bus at Gen1/Gen2/Gen3 rates.

1.10. Interlaken PCS Hard IP

Intel Stratix 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Intel Stratix 10 devices.

1.11. 10G Ethernet Hard IP

Intel Stratix 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

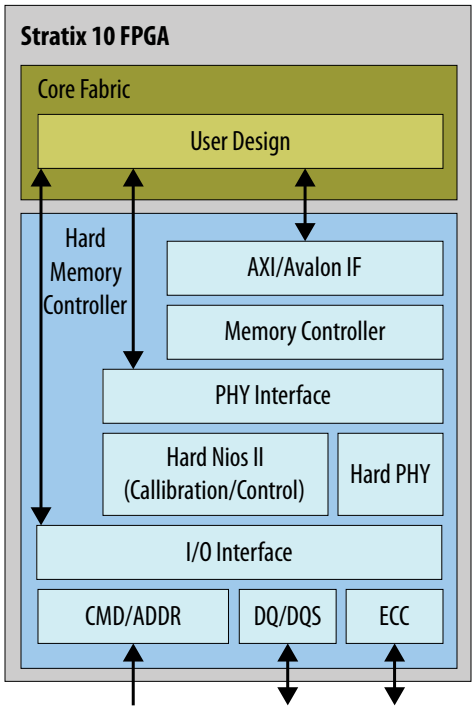
The integrated serial transceivers simplify multi-port 10GbE systems compared to 10 GbE Attachment Unit Interface (XAUI) interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated transceivers incorporate signal conditioning circuits, which enable direct connection to standard 10G XFP and SFP+ pluggable optical modules. The transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

1.12. External Memory and General Purpose I/O

Intel Stratix 10 devices offer substantial external memory bandwidth, with up to ten 72-bit wide DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth is provided along with the ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. The external memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers.

Figure 8. Hard Memory Controller



Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 10. External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

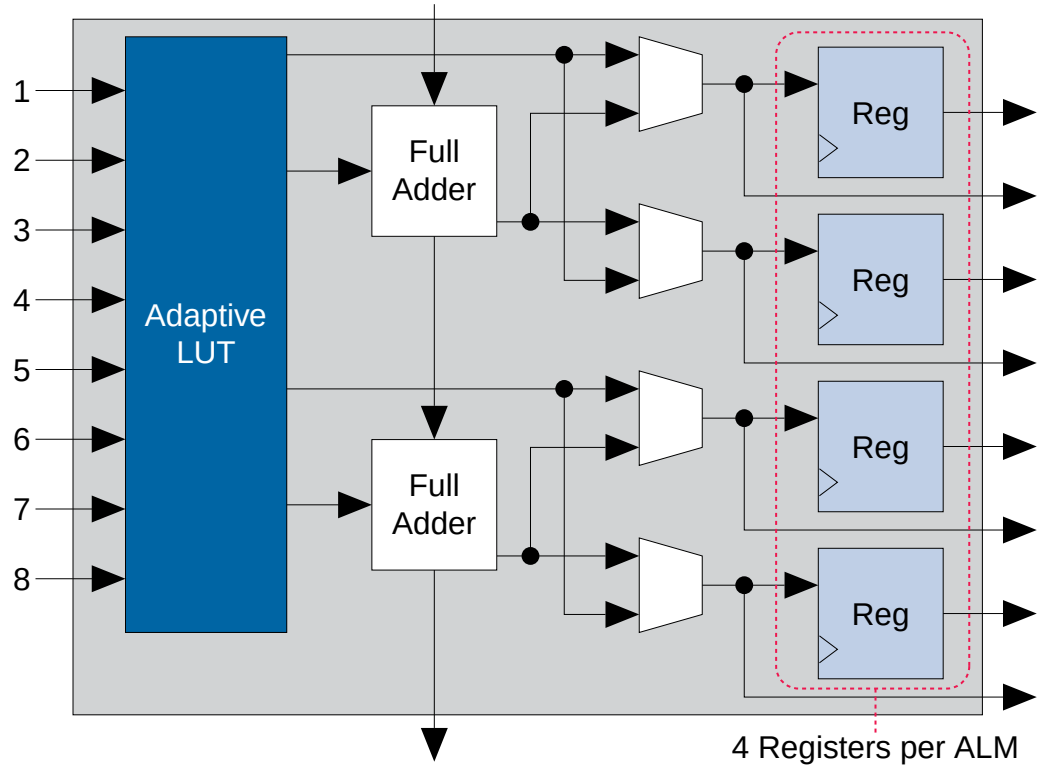
Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 9. Intel Stratix 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

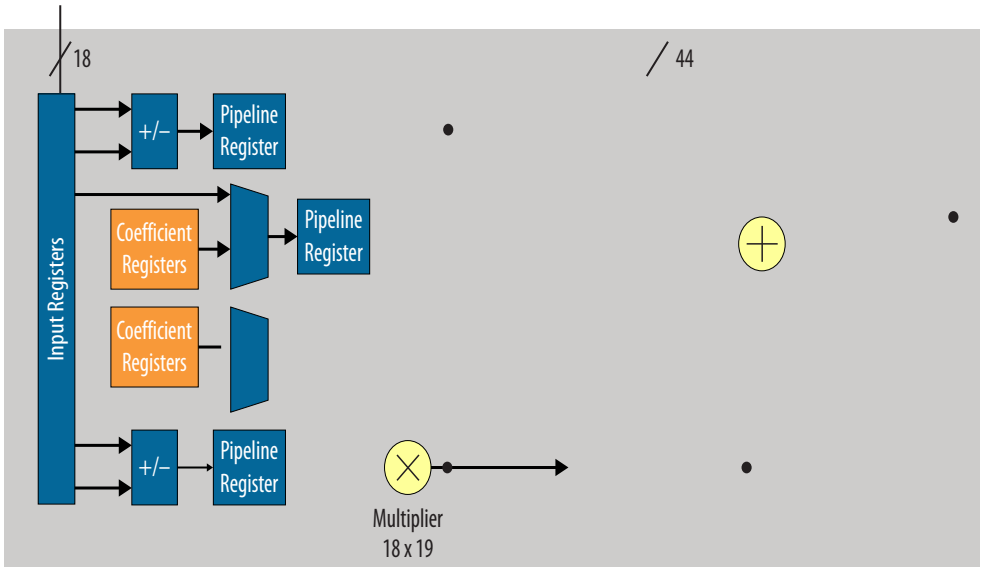



Figure 10. DSP Block: Standard Precision Fixed Point Mode