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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2500K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2397-BBGA, FCBGA
Supplier Device Package	2397-FBGA, FC (50x50)
Purchase URL	https://www.e-xfl.com/product-detail/intel/1sx250lu3f50e3vg



Contents

1. Intel® Stratix® 10 GX/SX Device Overview.....	3
1.1. Intel Stratix 10 Family Variants.....	4
1.1.1. Available Options.....	6
1.2. Innovations in Intel Stratix 10 FPGAs and SoCs.....	6
1.3. FPGA and SoC Features Summary.....	8
1.4. Intel Stratix 10 Block Diagram.....	11
1.5. Intel Stratix 10 FPGA and SoC Family Plan.....	11
1.6. HyperFlex Core Architecture.....	15
1.7. Heterogeneous 3D SiP Transceiver Tiles.....	16
1.8. Intel Stratix 10 Transceivers.....	17
1.8.1. PMA Features.....	18
1.8.2. PCS Features.....	20
1.9. PCI Express Gen1/Gen2/Gen3 Hard IP.....	21
1.10. Interlaken PCS Hard IP.....	21
1.11. 10G Ethernet Hard IP.....	22
1.12. External Memory and General Purpose I/O.....	22
1.13. Adaptive Logic Module (ALM).....	23
1.14. Core Clocking.....	24
1.15. Fractional Synthesis PLLs and I/O PLLs.....	25
1.16. Internal Embedded Memory.....	25
1.17. Variable Precision DSP Block.....	25
1.18. Hard Processor System (HPS).....	28
1.18.1. Key Features of the Intel Stratix 10 HPS.....	29
1.19. Power Management.....	32
1.20. Device Configuration and Secure Device Manager (SDM).....	32
1.21. Device Security.....	34
1.22. Configuration via Protocol Using PCI Express.....	34
1.23. Partial and Dynamic Reconfiguration.....	35
1.24. Fast Forward Compile.....	35
1.25. Single Event Upset (SEU) Error Detection and Correction.....	35
1.26. Document Revision History for the Intel Stratix 10 GX/SX Device Overview.....	36



Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

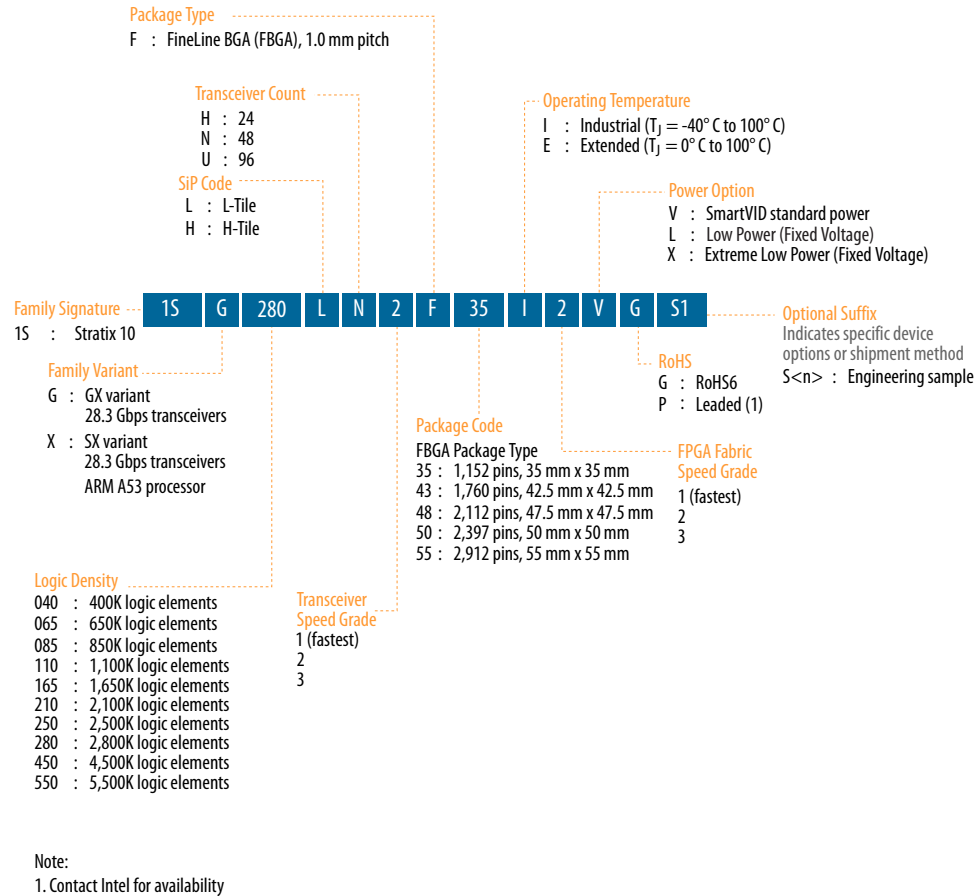
To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.



1.1.1. Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices



1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices

Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Process technology	28-nm TSMC (planar transistor)	14 nm Intel Tri-Gate (FinFET)
Hard processor core	None	Quad-core 64-bit ARM Cortex-A53 (SoC only)
Core architecture	Conventional core architecture with conventional interconnect	HyperFlex core architecture with Hyper-Registers in the interconnect
Core performance	500 MHz	1 GHz
Power dissipation	1x	As low as 0.3x
continued...		



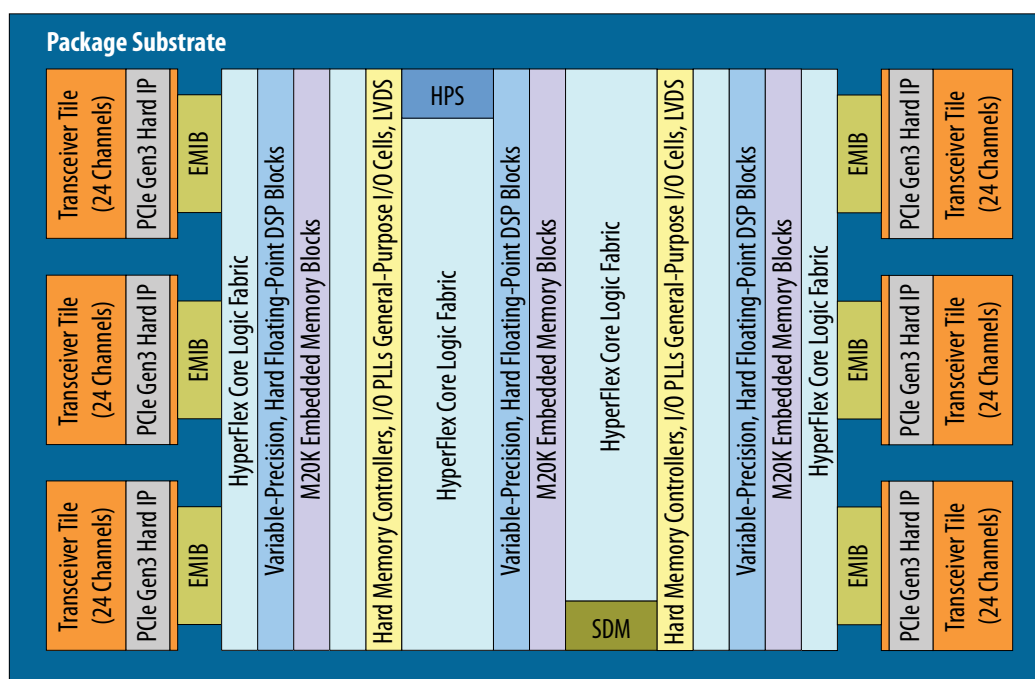
Feature	Description
Power management	<ul style="list-style-type: none"> SmartVID controlled core voltage, standard power devices 0.85-V fixed core voltage, low static power devices available Intel Quartus® Prime Pro Edition integrated power analysis
High performance monolithic core fabric	<ul style="list-style-type: none"> HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks Monolithic fabric minimizes compile times and increases logic utilization Enhanced adaptive logic module (ALM) Improved multi-track routing architecture reduces congestion and improves compile times Hierarchical core clocking architecture with programmable clock tree synthesis Fine-grained partial reconfiguration
Internal memory blocks	<ul style="list-style-type: none"> M20K—20-Kbit with hard ECC support MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	<ul style="list-style-type: none"> IEEE 754-compliant hard single-precision floating point capability Supports signal processing with precision ranging from 18x19 up to 54x54 Native 27x27 and 18x19 multiply modes 64-bit accumulator and cascade for systolic FIRs Internal coefficient memory banks Pre-adder/subtractor improves efficiency Additional pipeline register increases performance and reduces power
Phase locked loops (PLL)	<ul style="list-style-type: none"> Fractional synthesis PLLs (fPLL) support both fractional and integer modes Fractional mode with third-order delta-sigma modulation Precision frequency synthesis Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering
Core clock networks	<ul style="list-style-type: none"> 1 GHz fabric clocking 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks Clocks only synthesized where needed, to minimize dynamic power
continued...	



SoC Subsystem	Feature	Description
	NAND flash controller	<ul style="list-style-type: none"> 1 ONFI 1.0, 8- and 16-bit support
	General-purpose I/O (GPIO)	<ul style="list-style-type: none"> Maximum of 48 software programmable GPIO
	Timers	<ul style="list-style-type: none"> 4 general-purpose timers 4 watchdog timers
Secure Device Manager	Security	<ul style="list-style-type: none"> Secure boot Advanced Encryption Standard (AES) and authentication (SHA/ECDSA)
External Memory Interface	External Memory Interface	<ul style="list-style-type: none"> Hard Memory Controller with DDR4 and DDR3, and LPDDR3

1.4. Intel Stratix 10 Block Diagram

Figure 2. Intel Stratix 10 FPGA and SoC Architecture Block Diagram



HPS: Quad ARM Cortex-A53 Hard Processor System

SDM: Secure Device Manager

EMIB: Embedded Multi-Die Interconnect Bridge

1.5. Intel Stratix 10 FPGA and SoC Family Plan

⁽¹⁾ The number of 27x27 multipliers is one-half the number of 18x19 multipliers.



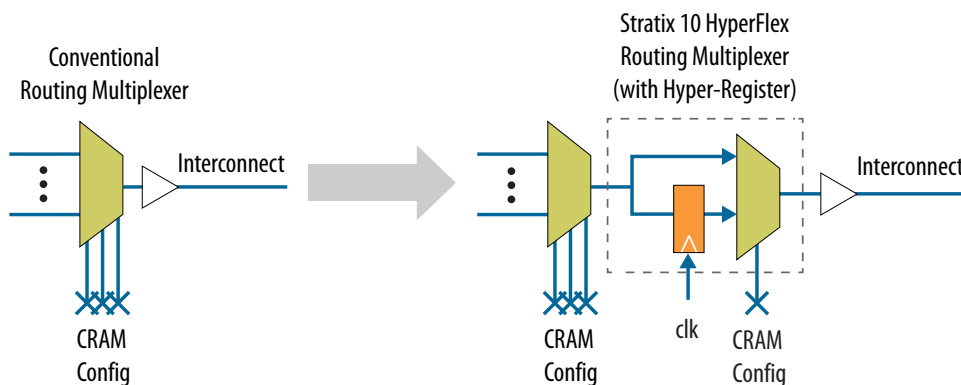
1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 3. Bypassable Hyper-Register



The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.



Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

1.8.1. PMA Features

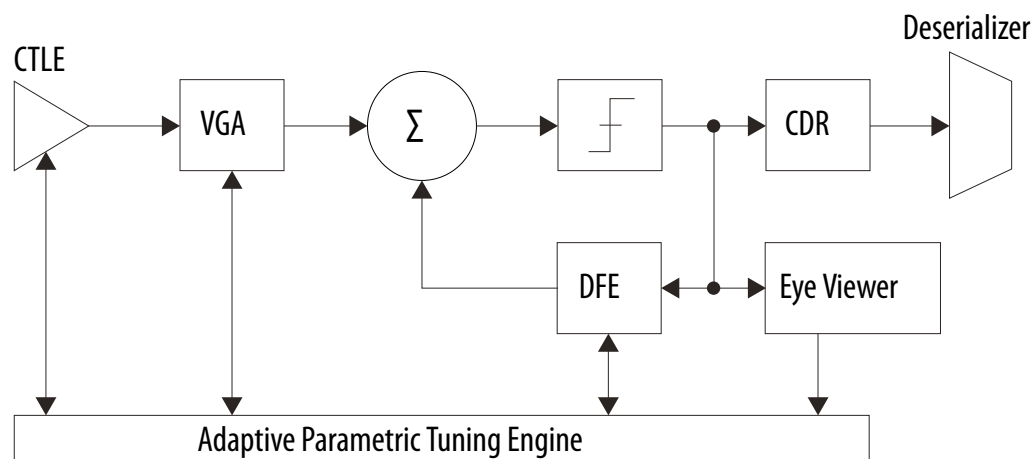
PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- **ATX PLL**—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.
- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.
- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- **Variable Gain Amplifier (VGA)**—to optimize the receiver's dynamic range
- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation
- **Decision Feedback Equalizer (DFE)**—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections
- **On-Die Instrumentation (ODI)**—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing

**Figure 7. Intel Stratix 10 Receiver Block Features**

All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

Table 8. Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps ⁽⁸⁾ to 28.3 Gbps (Intel Stratix 10 GX/SX devices)
Backplane Support	Drive backplanes at data rates up to 28.3 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, QSFPDD, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	15 fixed tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Advanced Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols, with optional fractional frequency synthesis capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost

continued...

⁽⁸⁾ Stratix 10 transceivers can support data rates below 1 Gbps with over sampling.



Feature	Capability
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation—Eye Viewer and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (Eye Viewer). Also inject jitter from transmitter to test link margin in system.
Dynamic Reconfiguration	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility.
Multiple PCS-PMA and PCS-Core to FPGA fabric interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

1.8.2. PCS Features

Intel Stratix 10 PMA channels interface with core logic through configurable and bypassable PCS interface layers.

The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. This feature provides the flexibility to implement a wide range of applications with 8, 10, 16, 20, 32, 40, or 64-bit interface width between each transceiver and the core logic.

The PCS also contains hard IP to support a variety of standard and proprietary protocols across a wide range of data rates and encoding schemes. The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports 64B/66B and 64B/67B encoded applications up to 17.4 Gbps. The enhanced PCS mode also includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit. For highly customized implementations, a PCS Direct mode provides an interface up to 64 bits wide to allow for custom encoding and support for data rates up to 28.3 Gbps.

For more information about the PCS-Core interface or the double rate transfer mode, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*, and the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.

Table 9. Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	1 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x2, x4, x8, x16	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core
PCI Express Gen3 x1, x2, x4, x8, x16	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit-slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
continued...			



Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 10. External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

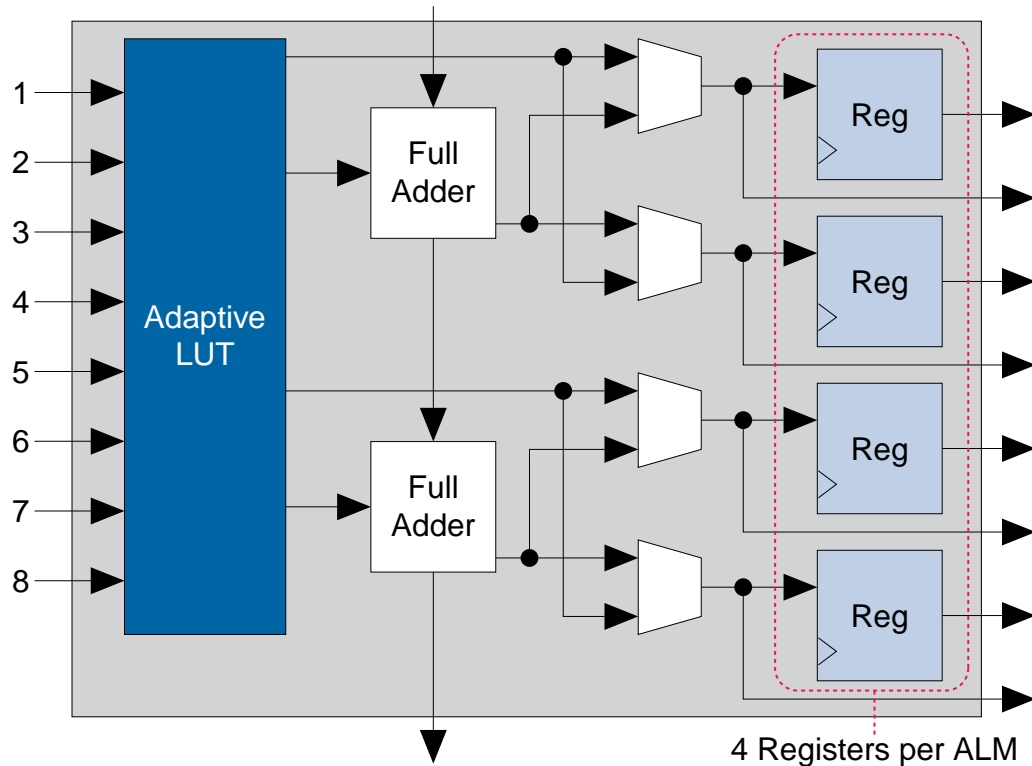
Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

Figure 9. Intel Stratix 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

1.14. Core Clocking

Core clocking in Intel Stratix 10 devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.



The core clock network in Intel Stratix 10 devices supports the new HyperFlex core architecture at clock rates up to 1 GHz. It also supports the hard memory controllers up to 2666 Mbps with a quarter rate transfer to the core. The core clock network is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

1.15. Fractional Synthesis PLLs and I/O PLLs

Intel Stratix 10 devices have up to 32 fractional synthesis PLLs (fPLL) available for use with transceivers or in the core fabric.

The fPLLs are located in the 3D SiP transceiver H-tiles, eight per tile, adjacent to the transceiver channels. The fPLLs can be used to reduce both the number of oscillators required on the board and the number of clock pins required, by synthesizing multiple clock frequencies from a single reference clock source. In addition to synthesizing reference clock frequencies for the transceiver transmit PLLs, the fPLLs can also be used directly for transmit clocking. Each fPLL can be independently configured for conventional integer mode, or enhanced fractional synthesis mode with third-order delta-sigma modulation.

In addition to the fPLLs, Intel Stratix 10 devices contain up to 34 integer I/O PLLs (IOPLLs) available for general purpose use in the core fabric and for simplifying the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are located in each bank of 48 general purpose I/O, 1 per I/O bank, adjacent to the hard memory controllers and LVDS SerDes in each I/O bank. This makes it easier to close timing because the IOPLLs are tightly coupled with the I/Os that need to use them. The IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay clock buffering.

1.16. Internal Embedded Memory

Intel Stratix 10 devices contain two types of embedded memory blocks: M20K (20-Kbit) and MLAB (640-bit).

The M20K and MLAB blocks are familiar block sizes carried over from previous Intel device families. The MLAB blocks are ideal for wide and shallow memories, while the M20K blocks are intended to support larger memory configurations and include hard ECC. Both M20K and MLAB embedded memory blocks can be configured as a single-port or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are highly flexible and support a number of memory configurations as shown in [Table 11](#) on page 25.

Table 11. Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation) 32 x 20	2K x 10 (or x8) 1K x 20 (or x16) 512 x 40 (or x32)

1.17. Variable Precision DSP Block

The Intel Stratix 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE-754 compliant floating point capability.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Figure 10. DSP Block: Standard Precision Fixed Point Mode

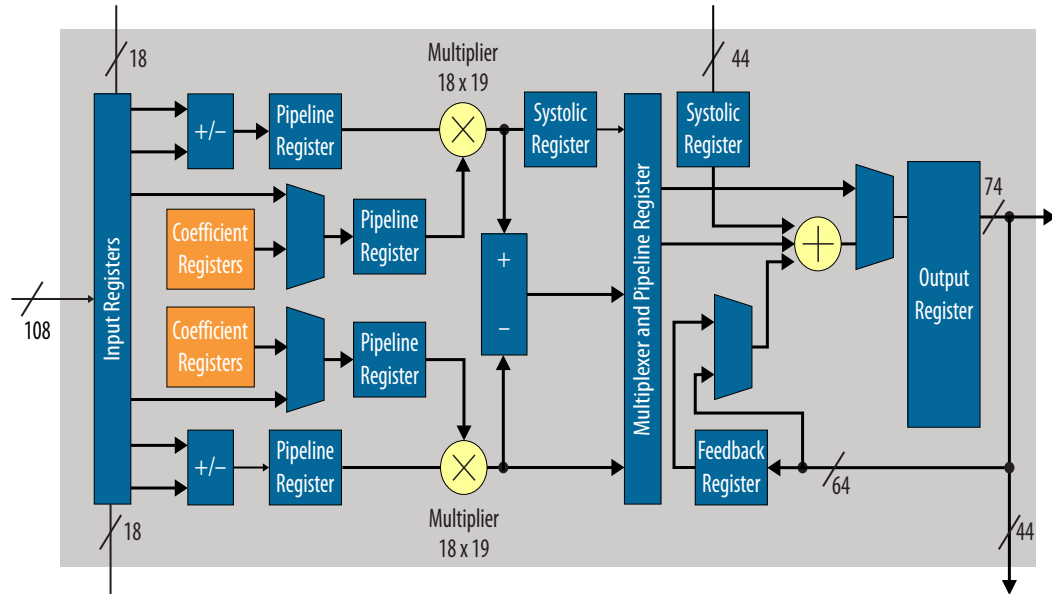
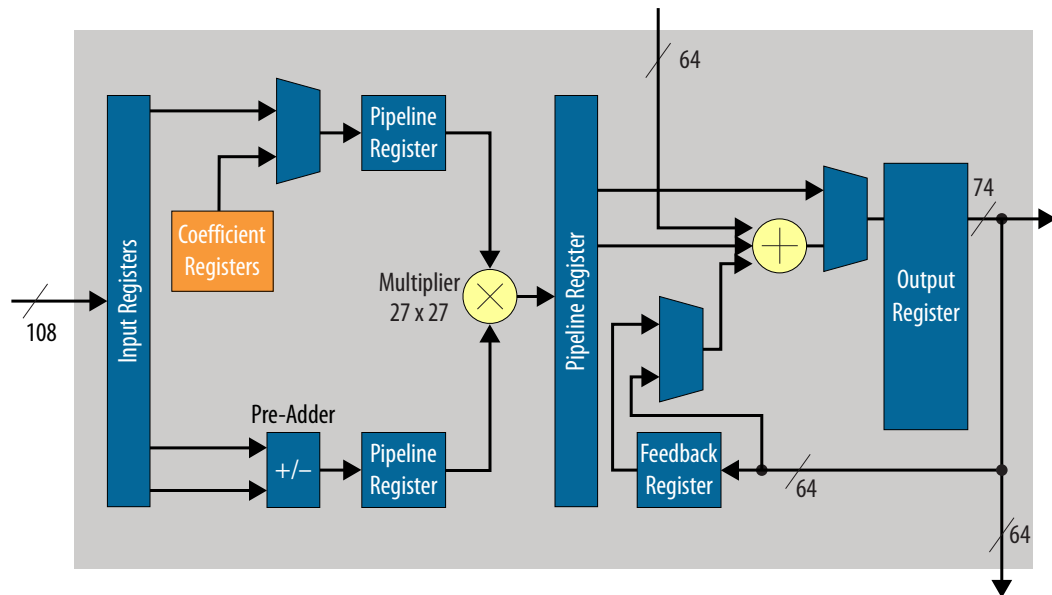


Figure 11. DSP Block: High Precision Fixed Point Mode





Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Table 13. Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFT
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT

For FFT applications with high dynamic range requirements, the Intel FFT IP Core offers an option of single precision floating point implementation with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

- Hard 18-bit and 25-bit pre-adders
- Hard floating point multipliers and adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Intel Quartus Prime software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. With the Variable Precision DSP block architecture and hard floating point multipliers and adders, Intel Stratix 10 devices can efficiently support many different precision levels up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

1.18. Hard Processor System (HPS)

The Intel Stratix 10 SoC Hard Processor System (HPS) is Intel's industry leading third generation HPS. Leveraging the performance of Intel's 14-nm Tri-Gate technology, Intel Stratix 10 SoC devices more than double the performance of previous generation SoCs with an integrated quad-core 64-bit ARM Cortex-A53. The HPS also enables system-wide hardware virtualization capabilities by adding a system memory management unit. These architecture improvements ensure that Intel Stratix 10 SoCs will meet the requirements of current and future embedded markets, including wireless and wireline communications, data center acceleration, and numerous military applications.



Feature	Description
	<ul style="list-style-type: none"> Superscalar, variable length, out-of-order pipeline with dynamic branch prediction Improved ARM NEON™ media processing engine Single- and double-precision floating-point unit CoreSight™ debug and trace technology
System Memory Management Unit	<ul style="list-style-type: none"> Enables a unified memory model and extends hardware virtualization into peripherals implemented in the FPGA fabric
Cache Coherency unit	<ul style="list-style-type: none"> Changes in shared data stored in cache are propagated throughout the system providing bi-directional coherency for co-processing elements.
Cache	<ul style="list-style-type: none"> L1 Cache <ul style="list-style-type: none"> 32 KB of instruction cache w/ parity check 32 KB of L1 data cache w /ECC Parity checking L2 Cache <ul style="list-style-type: none"> 1MB shared 8-way set associative SEU Protection with parity on TAG ram and ECC on data RAM Cache lockdown support
On-Chip Memory	<ul style="list-style-type: none"> 256 KB of scratch on-chip RAM
External SDRAM and Flash Memory Interfaces for HPS	<ul style="list-style-type: none"> Hard memory controller with support for DDR4, DDR3, LPDDR3 <ul style="list-style-type: none"> 40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC) Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters Software Configurable Priority Scheduling on individual SDRAM bursts Fully programmable timing parameter support for all JEDEC-specified timing parameters Multiport front-end (MPFE) scheduler interface to the hard memory controller, which supports the AXI® Quality of Service (QoS) for interface to the FPGA fabric NAND flash controller <ul style="list-style-type: none"> ONFI 1.0 Integrated descriptor based with DMA Programmable hardware ECC support Support for 8- and 16-bit Flash devices Secure Digital SD/SDIO/MMC controller <ul style="list-style-type: none"> eMMC 4.5 Integrated descriptor based DMA CE-ATA digital commands supported 50 MHz operating frequency Direct memory access (DMA) controller <ul style="list-style-type: none"> 8-channel Supports up to 32 peripheral handshake interface

continued...



1.19. Power Management

Intel Stratix 10 devices leverage the advanced Intel 14-nm Tri-Gate process technology, the all new HyperFlex core architecture to enable Hyper-Folding, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

With the new HyperFlex core architecture, designs can run 2X faster than previous generation FPGAs. With 2X performance and same required throughput, architects can cut the data path width in half to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

The optional power reduction techniques in Intel Stratix 10 devices include:

- **Available Low Static Power Devices**—Intel Stratix 10 devices are available with a fixed core voltage that provides lower static power than the SmartVID standard power devices, while maintaining device performance

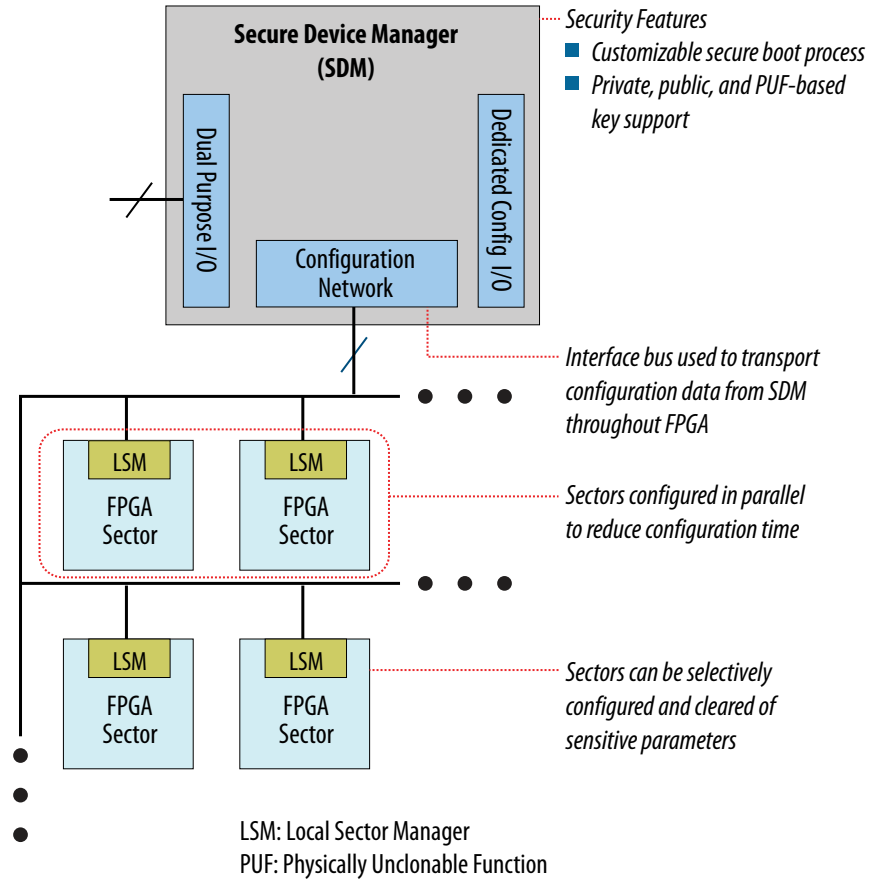
Furthermore, Intel Stratix 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

1.20. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.



Figure 14. SDM Block Diagram



During configuration, Intel Stratix 10 devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.



powered up and active within the 100 ms time allowed by the PCI Express specification. Intel Stratix 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

1.23. Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Intel Quartus Prime design software

Dynamic reconfiguration in Intel Stratix 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multiprotocol or multi-rate support. Both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

1.24. Fast Forward Compile

The innovative Fast Forward Compile feature in the Intel Quartus Prime software identifies performance bottlenecks in your design and provides detailed, step-by-step performance improvement recommendations that you can then implement. The Compiler reports estimates of the maximum operating frequency that can be achieved by applying the recommendations. As part of the new Hyper-Aware design flow, Fast Forward Compile maximizes the performance of your Intel Stratix 10 design and achieves rapid timing closure.

Previously, this type of optimization required multiple time-consuming design iterations, including full design re-compilation to determine the effectiveness of the changes. Fast Forward Compile enables you to make better decisions about where to focus your optimization efforts, and how to increase your design performance and throughput. This technique removes much of the guesswork of performance exploration, resulting in fewer design iterations and as much as 2X core performance gains for Intel Stratix 10 designs.

1.25. Single Event Upset (SEU) Error Detection and Correction

Intel Stratix 10 FPGAs and SoCs offer robust SEU error detection and correction circuitry. The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running parity checker circuit with integrated ECC that automatically corrects one or two bit errors and detects higher order multibit errors.



The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 14-nm Tri-Gate process technology used for Intel Stratix 10 devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

1.26. Document Revision History for the Intel Stratix 10 GX/SX Device Overview

Document Version	Changes
2018.08.08	Made the following changes: <ul style="list-style-type: none">• Changed the specs for QDRII+ and QDRII+ Xtreme and added specs for QDRIV in the "External Memory Interface Performance" table.• Updated description of the power options in the "Sample Ordering COde and Available Options for Intel Stratix 10 Devices" figure.• Changed the description of the technology and power management features in the "Intel Stratix 10 FPGA and SoC Common Device Features" table.• Changed the description of SmartVID in the "Power Management" section.• Changed the direction arrow from the coefficient registers block in the "DSP Block: High Precision Fixed Point Mode" figure.
2017.10.30	Made the following changes: <ul style="list-style-type: none">• Removed the embedded eSRAM feature globally.• Removed the Low Power (VID) and Military operating temperature options, and package code 53 from the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure.• Changed the Maximum transceiver data rate (chip-to-chip) specification for L-Tile devices in the "Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices" table.
2016.10.31	Made the following changes: <ul style="list-style-type: none">• Changed the number of available transceivers to 96, globally.• Changed the single-precision floating point performance to 10 TeraFLOPS, globally.• Changed the maximum datarate to 28.3 Gbps, globally.• Changed some of the features listed in the "Stratix 10 GX/SX Device Overview" section.• Changed descriptions for the GX and SX devices in the "Stratix 10 Family Variants" section.• Changed the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure.
continued...	



Document Version	Changes
	<ul style="list-style-type: none"> • Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table. • Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table: <ul style="list-style-type: none"> — Transceiver hard IP — Internal memory blocks — Core clock networks — Packaging • Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section. • Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section. • Removed footnotes from the "Transceiver PCS Features" table. • Changed the HMC description in the "External Memory and General Purpose I/O" section. • Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section. • Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table. • Changed the description in the "Internal Embedded Memory" section. • Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table. • Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section. • Updated the "Key Features of the Stratix 10 HPS" table. • Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table. • Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table.
2015.12.04	Initial release.