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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2500K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	2397-BBGA, FCBGA
Supplier Device Package	2397-FBGA, FC (50x50)
Purchase URL	https://www.e-xfl.com/product-detail/intel/1sx250lu3f50i1vg

Contents

Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.

- **Additional Hard IP**: Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking**: Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs**: The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

1.3. FPGA and SoC Features Summary

Table 2. Intel Stratix 10 FPGA and SoC Common Device Features

Feature	Description
Technology	• 14-nm Intel Tri-Gate (FinFET) process technology • SmartVID controlled core voltage, standard power devices • 0.85-V fixed core voltage, low static power devices available
Low power serial transceivers	• Up to 96 total transceivers available • Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices • Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)
General purpose I/Os	• Up to 1640 total GPIO available • 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port • DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller) • Multiple hard IP instantiations in each device • Single Root I/O Virtualization (SR-IOV)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols

continued...

Feature	Description
Power management	• SmartVID controlled core voltage, standard power devices • 0.85-V fixed core voltage, low static power devices available • Intel Quartus® Prime Pro Edition integrated power analysis
High performance monolithic core fabric	• HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks • Monolithic fabric minimizes compile times and increases logic utilization • Enhanced adaptive logic module (ALM) • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture with programmable clock tree synthesis • Fine-grained partial reconfiguration
Internal memory blocks	• M20K—20-Kbit with hard ECC support • MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	• IEEE 754-compliant hard single-precision floating point capability • Supports signal processing with precision ranging from 18x19 up to 54x54 • Native 27x27 and 18x19 multiply modes • 64-bit accumulator and cascade for systolic FIRs • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • Additional pipeline register increases performance and reduces power
Phase locked loops (PLL)	• Fractional synthesis PLLs (fPLL) support both fractional and integer modes • Fractional mode with third-order delta-sigma modulation • Precision frequency synthesis • Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering
Core clock networks	• 1 GHz fabric clocking • 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface • 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface • Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks • Clocks only synthesized where needed, to minimize dynamic power

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Feature	Description
Configuration	• Dedicated Secure Device Manager • Software programmable device configuration • Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication • Physically Unclonable Function (PUF) service
Packaging	• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology • Multiple devices with identical package footprints allows seamless migration across different device densities • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Software and tools	• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • Fast Forward compiler to allow HyperFlex architecture performance exploration • Transceiver toolkit • Platform designer integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Table 3. Intel Stratix 10 SoC Specific Device Features

SoC Subsystem	Feature	Description
Hard Processor System	Multi-processor unit (MPU) core	• Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology • Scalar floating-point unit supporting single and double precision • ARM NEON media processing engine for each processor
	System Controllers	• System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
	Layer 1 Cache	• 32 KB L1 instruction cache with parity • 32 KB L1 data cache with ECC
	Layer 2 Cache	• 1 MB Shared L2 Cache with ECC
	On-Chip Memory	• 256 KB On-Chip RAM
	Direct memory access (DMA) controller	• 8-Channel DMA
	Ethernet media access controller (EMAC)	• Three 10/100/1000 EMAC with integrated DMA
	USB On-The-Go controller (OTG)	• 2 USB OTG with integrated DMA
	UART controller	• 2 UART 16550 compatible
	Serial Peripheral Interface (SPI) controller	• 4 SPI
	I^2C controller	• 5 I^2C controllers
	SD/SDIO/MMC controller	• 1 eMMC version 4.5 with DMA and CE-ATA support • SD, including eSD, version 3.0 • SDIO, including eSDIO, version 3.0 • CE-ATA - version 1.1

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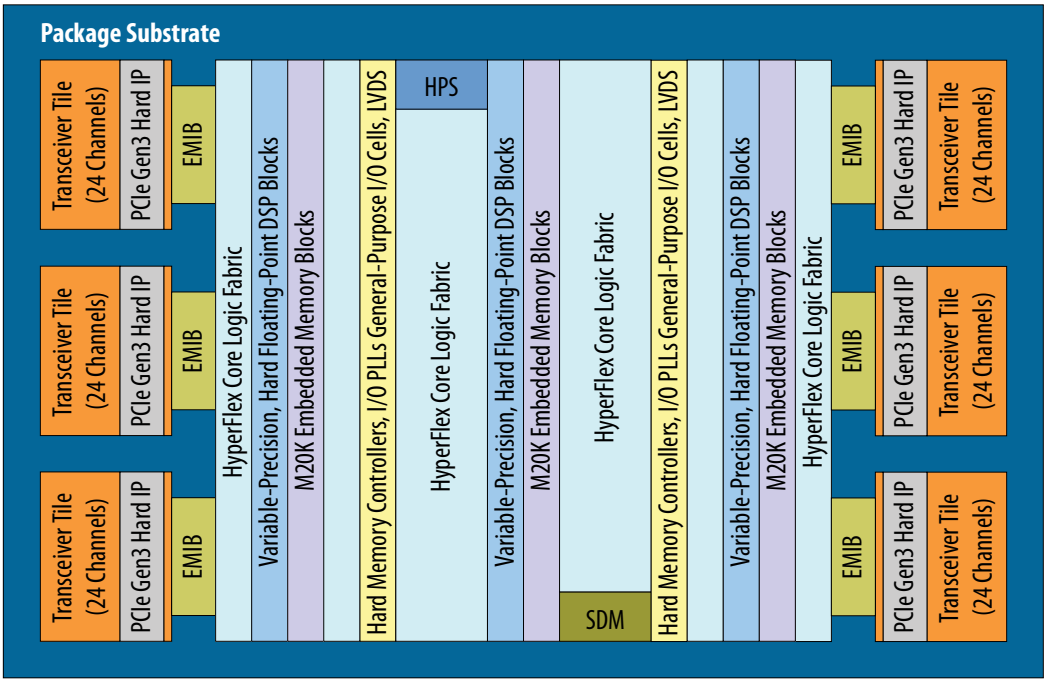
SoC Subsystem	Feature	Description
	NAND flash controller	• 1 ONFI 1.0, 8- and 16-bit support
	General-purpose I/O (GPIO)	• Maximum of 48 software programmable GPIO
	Timers	• 4 general-purpose timers • 4 watchdog timers
Secure Device Manager	Security	• Secure boot • Advanced Encryption Standard (AES) and authentication (SHA/ECDSA)
External Memory Interface	External Memory Interface	• Hard Memory Controller with DDR4 and DDR3, and LPDDR3

1.4. Intel Stratix 10 Block Diagram

Figure 2. Intel Stratix 10 FPGA and SoC Architecture Block Diagram



HPS: Quad ARM Cortex-A53 Hard Processor System
SDM: Secure Device Manager
EMIB: Embedded Multi-Die Interconnect Bridge

1.5. Intel Stratix 10 FPGA and SoC Family Plan

(1) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

Intel Stratix 10 GX/SX Device Name	Interconnects		PLLs		Hard IP
	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 2800/ SX 2800	1160	96	32	24	4
GX 4500/ SX 4500	1640	24	8	34	1
GX 5500/ SX 5500	1640	24	8	34	1

Table 6. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 1

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers (2) (3) (4) (5) (6) (7)

Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm²)	F1760 NF43 (42.5x42.5 mm²)	F1760 NF43 (42.5x42.5 mm²)
GX 400/ SX 400	392, 8, 192, 24		
GX 650/ SX 650	392, 8, 192, 24	400, 16, 192, 48	
GX 850/ SX 850			688, 16, 336, 48
GX 1100/ SX 1100			688, 16, 336, 48
GX 1650/ SX 1650			688, 16, 336, 48
GX 2100/ SX 2100			688, 16, 336, 48
GX 2500/ SX 2500			688, 16, 336, 48
GX 2800/			688, 16, 336, 48

continued...

(2) All packages are ball grid arrays with 1.0 mm pitch.

(3) High-Voltage I/O pins are used for 3 V and 2.5 V interfacing.

(4) Each LVDS pair can be configured as either a differential input or a differential output.

(5) High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.

(6) Each package column offers pin migration (common circuit board footprint) for all devices in the column.

(7) Intel Stratix 10 GX devices are pin migratable with Intel Stratix 10 SX devices in the same package.

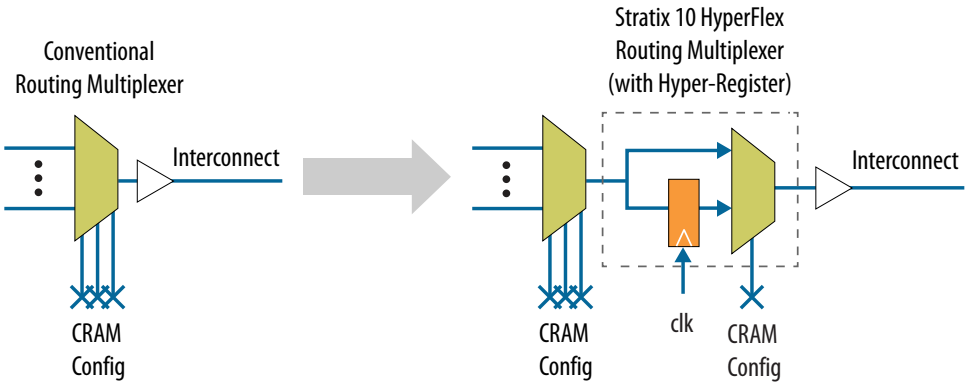
1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 3. Bypassable Hyper-Register



The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

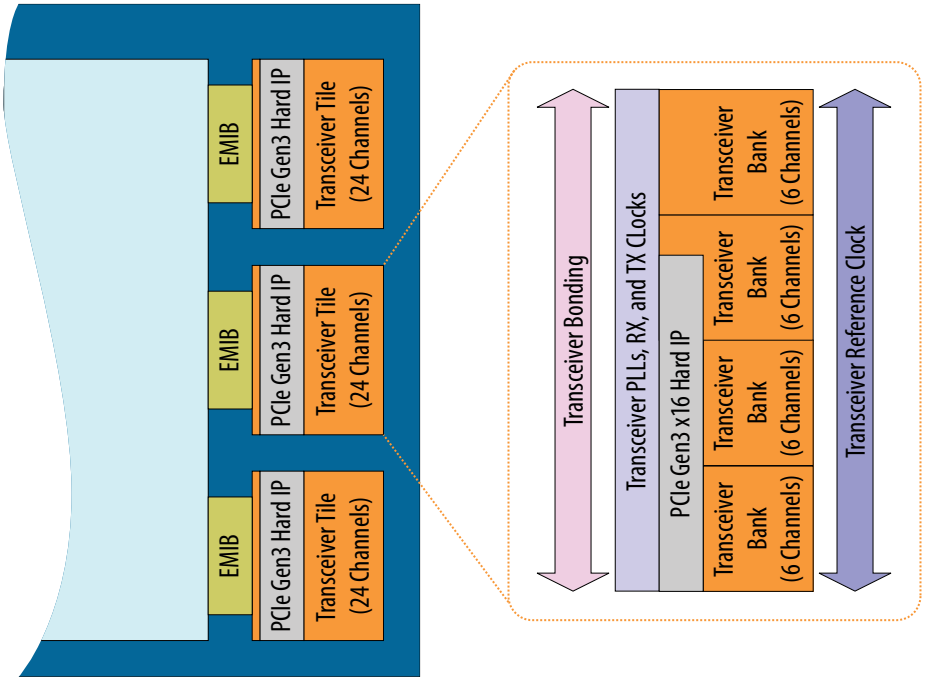
- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

Each transceiver tile contains:

- 24 full-duplex transceiver channels (PMA and PCS)
- Reference clock distribution network
- Transmit PLLs
- High-speed clocking and bonding networks
- One instance of PCI Express hard IP

Figure 6. Heterogeneous 3D SiP Transceiver Tile Architecture



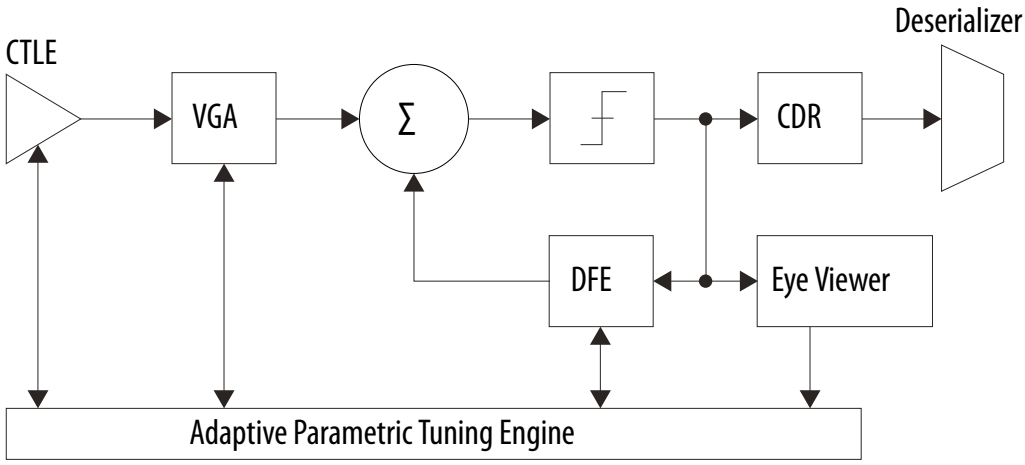
1.8. Intel Stratix 10 Transceivers

Intel Stratix 10 devices offer up to 96 total full-duplex transceiver channels. These channels provide continuous data rates from 1 Gbps to 28.3 Gbps for chip-to-chip, chip-to-module, and backplane applications. In each device,two thirds of the transceivers can be configured up to the maximum data rate of 28.3 Gbps to drive 100G interfaces and C form-factor pluggable CFP2/CFP4 optical modules. For longer-reach backplane driving applications, advanced adaptive equalization circuits are used to equalize over 30 dB of system loss.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

Figure 7. Intel Stratix 10 Receiver Block Features



All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

Table 8. Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps [8] to 28.3 Gbps (Intel Stratix 10 GX/SX devices)
Backplane Support	Drive backplanes at data rates up to 28.3 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, QSFPDD, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	15 fixed tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Advanced Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols, with optional fractional frequency synthesis capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost

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(8) Stratix 10 transceivers can support data rates below 1 Gbps with over sampling.

Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 10. External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

The core clock network in Intel Stratix 10 devices supports the new HyperFlex core architecture at clock rates up to 1 GHz. It also supports the hard memory controllers up to 2666 Mbps with a quarter rate transfer to the core. The core clock network is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

1.15. Fractional Synthesis PLLs and I/O PLLs

Intel Stratix 10 devices have up to 32 fractional synthesis PLLs (fPLL) available for use with transceivers or in the core fabric.

The fPLLs are located in the 3D SiP transceiver H-tiles, eight per tile, adjacent to the transceiver channels. The fPLLs can be used to reduce both the number of oscillators required on the board and the number of clock pins required, by synthesizing multiple clock frequencies from a single reference clock source. In addition to synthesizing reference clock frequencies for the transceiver transmit PLLs, the fPLLs can also be used directly for transmit clocking. Each fPLL can be independently configured for conventional integer mode, or enhanced fractional synthesis mode with third-order delta-sigma modulation.

In addition to the fPLLs, Intel Stratix 10 devices contain up to 34 integer I/O PLLs (IOPLLs) available for general purpose use in the core fabric and for simplifying the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are located in each bank of 48 general purpose I/O, 1 per I/O bank, adjacent to the hard memory controllers and LVDS SerDes in each I/O bank. This makes it easier to close timing because the IOPLLs are tightly coupled with the I/Os that need to use them. The IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay clock buffering.

1.16. Internal Embedded Memory

Intel Stratix 10 devices contain two types of embedded memory blocks: M20K (20-Kbit) and MLAB (640-bit).

The M20K and MLAB blocks are familiar block sizes carried over from previous Intel device families. The MLAB blocks are ideal for wide and shallow memories, while the M20K blocks are intended to support larger memory configurations and include hard ECC. Both M20K and MLAB embedded memory blocks can be configured as a single-port or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are highly flexible and support a number of memory configurations as shown in Table 11 on page 25.

Table 11. Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation) 32 x 20	2K x 10 (or x8) 1K x 20 (or x16) 512 x 40 (or x32)

1.17. Variable Precision DSP Block

The Intel Stratix 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE-754 compliant floating point capability.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Figure 10. DSP Block: Standard Precision Fixed Point Mode

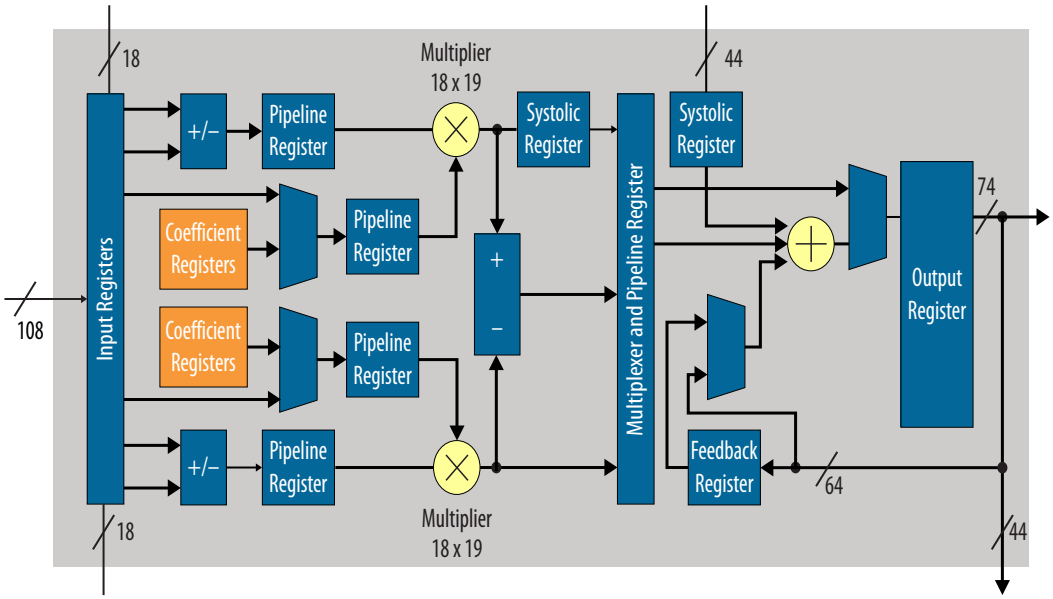


Figure 11. DSP Block: High Precision Fixed Point Mode

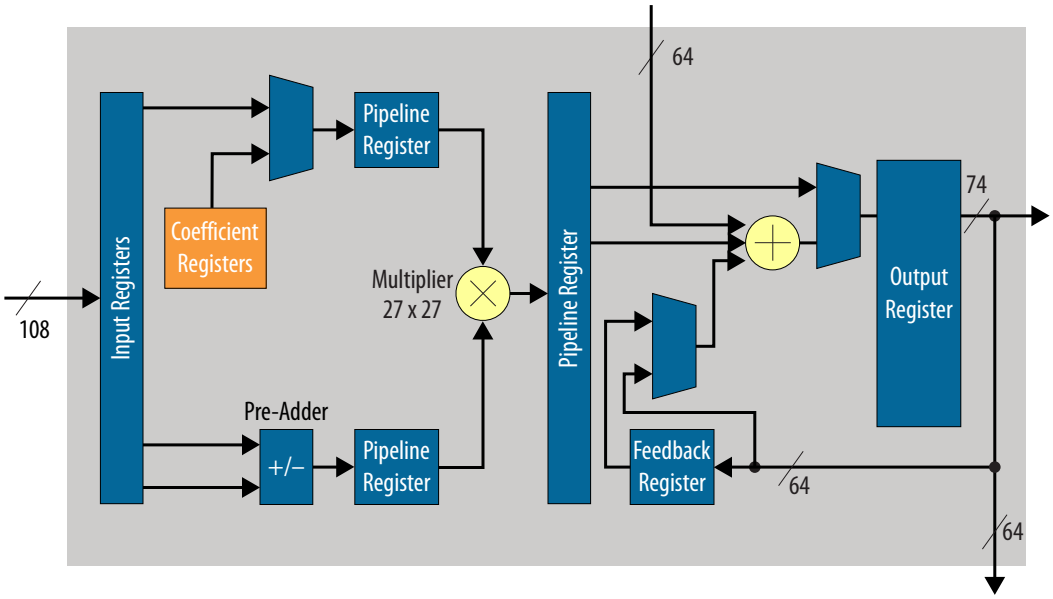
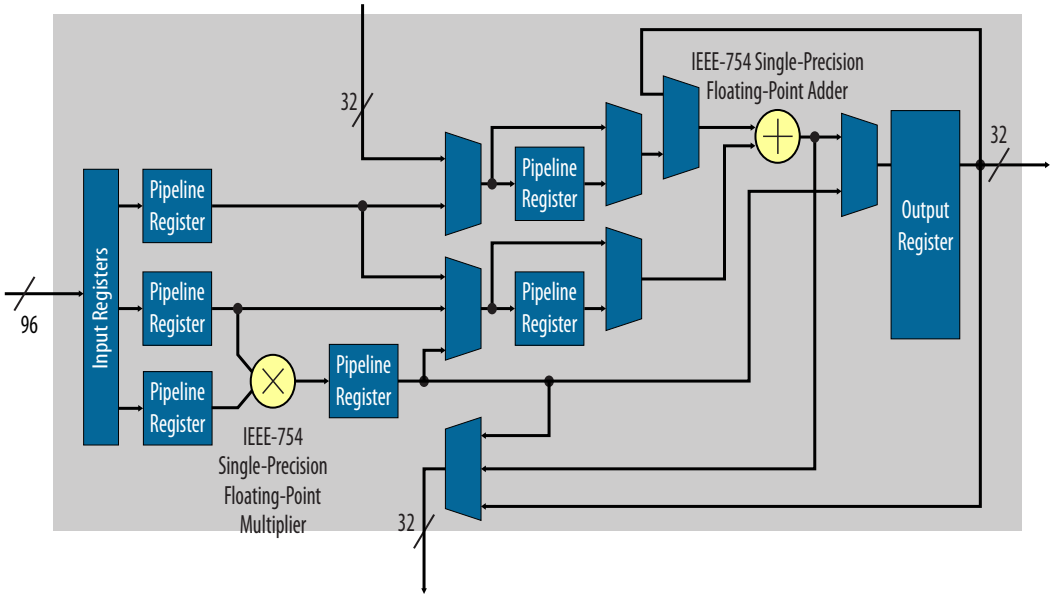


Figure 12. DSP Block: Single Precision Floating Point Mode



Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 12. Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point
Single Precision floating point	1 Single Precision floating point adder, 1 Single Precision floating point multiplier	Floating point

Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Table 13. Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFT
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT

For FFT applications with high dynamic range requirements, the Intel FFT IP Core offers an option of single precision floating point implementation with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

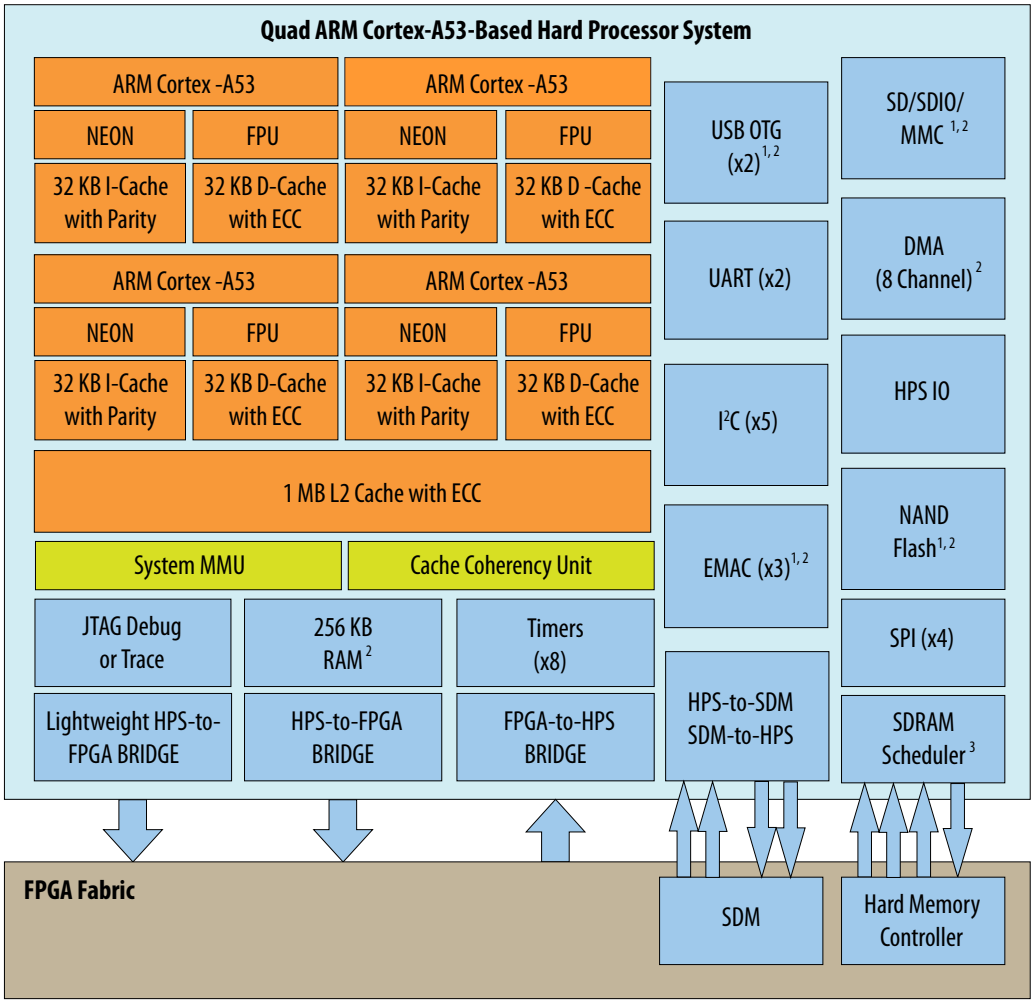
- Hard 18-bit and 25-bit pre-adders
- Hard floating point multipliers and adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Intel Quartus Prime software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. With the Variable Precision DSP block architecture and hard floating point multipliers and adders, Intel Stratix 10 devices can efficiently support many different precision levels up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

1.18. Hard Processor System (HPS)

The Intel Stratix 10 SoC Hard Processor System (HPS) is Intel's industry leading third generation HPS. Leveraging the performance of Intel's 14-nm Tri-Gate technology, Intel Stratix 10 SoC devices more than double the performance of previous generation SoCs with an integrated quad-core 64-bit ARM Cortex-A53. The HPS also enables system-wide hardware virtualization capabilities by adding a system memory management unit. These architecture improvements ensure that Intel Stratix 10 SoCs will meet the requirements of current and future embedded markets, including wireless and wireline communications, data center acceleration, and numerous military applications.

Figure 13. HPS Block Diagram



Notes:
1. Integrated direct memory access (DMA)
2. Integrated error correction code (ECC)
3. Multiport front-end interface to hard memory controller

1.18.1. Key Features of the Intel Stratix 10 HPS

Table 14. Key Features of the Intel Stratix 10 GX/SX HPS

Feature	Description
Quad-core ARM Cortex-A53 MPCore processor unit	• 2.3 MIPS/MHz instruction efficiency • CPU frequency up to 1.5 GHz • At 1.5 GHz total performance of 13,800 MIPS • ARMv8-A architecture • Runs 64-bit and 32-bit ARM instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Jazelle® RCT execution architecture with 8-bit Java bytecodes

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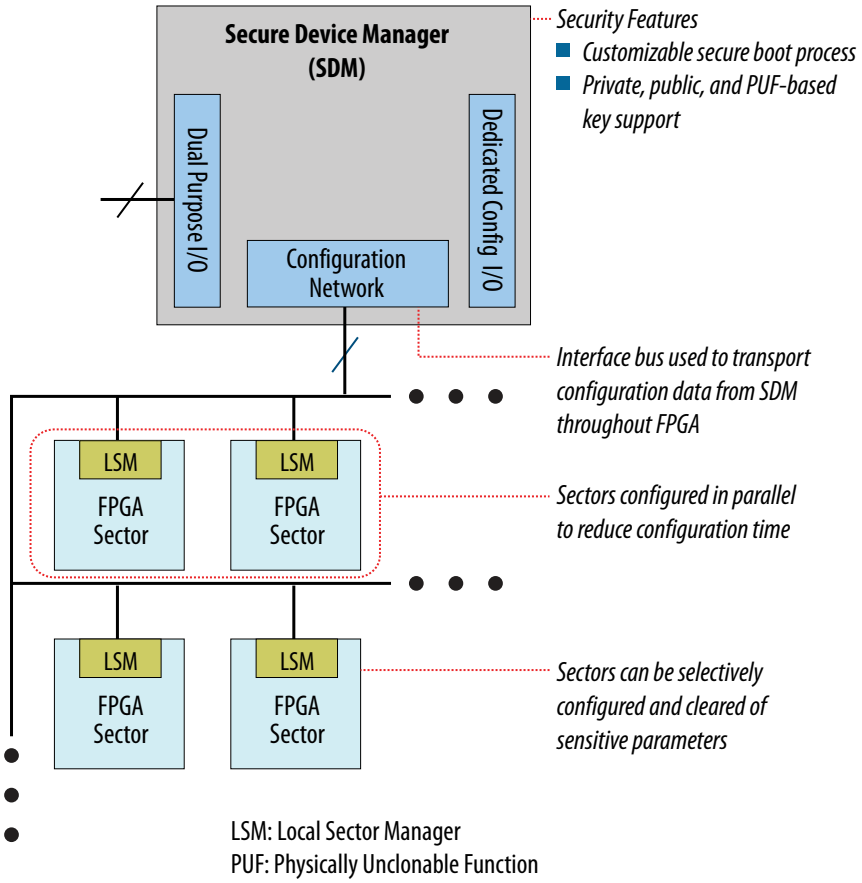
Figure 14. SDM Block Diagram



During configuration, Intel Stratix 10 devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.

The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be

powered up and active within the 100 ms time allowed by the PCI Express specification. Intel Stratix 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

1.23. Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Intel Quartus Prime design software

Dynamic reconfiguration in Intel Stratix 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multiprotocol or multi-rate support. Both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

1.24. Fast Forward Compile

The innovative Fast Forward Compile feature in the Intel Quartus Prime software identifies performance bottlenecks in your design and provides detailed, step-by-step performance improvement recommendations that you can then implement. The Compiler reports estimates of the maximum operating frequency that can be achieved by applying the recommendations. As part of the new Hyper-Aware design flow, Fast Forward Compile maximizes the performance of your Intel Stratix 10 design and achieves rapid timing closure.

Previously, this type of optimization required multiple time-consuming design iterations, including full design re-compilation to determine the effectiveness of the changes. Fast Forward Compile enables you to make better decisions about where to focus your optimization efforts, and how to increase your design performance and throughput. This technique removes much of the guesswork of performance exploration, resulting in fewer design iterations and as much as 2X core performance gains for Intel Stratix 10 designs.

1.25. Single Event Upset (SEU) Error Detection and Correction

Intel Stratix 10 FPGAs and SoCs offer robust SEU error detection and correction circuitry. The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running parity checker circuit with integrated ECC that automatically corrects one or two bit errors and detects higher order multibit errors.

Document Version	Changes
	• Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table. • Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table: — Transceiver hard IP — Internal memory blocks — Core clock networks — Packaging • Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section. • Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section. • Removed footnotes from the "Transceiver PCS Features" table. • Changed the HMC description in the "External Memory and General Purpose I/O" section. • Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section. • Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table. • Changed the description in the "Internal Embedded Memory" section. • Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table. • Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section. • Updated the "Key Features of the Stratix 10 HPS" table. • Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table. • Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table.
2015.12.04	Initial release.