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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

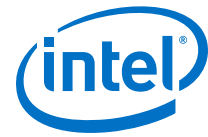
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2500K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	2397-BBGA, FCBGA
Supplier Device Package	2397-FBGA, FC (50x50)
Purchase URL	https://www.e-xfl.com/product-detail/intel/1sx250lu3f50i2lg



1. Intel® Stratix® 10 GX/SX Device Overview

Intel's 14-nm Intel® Stratix® 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

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Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

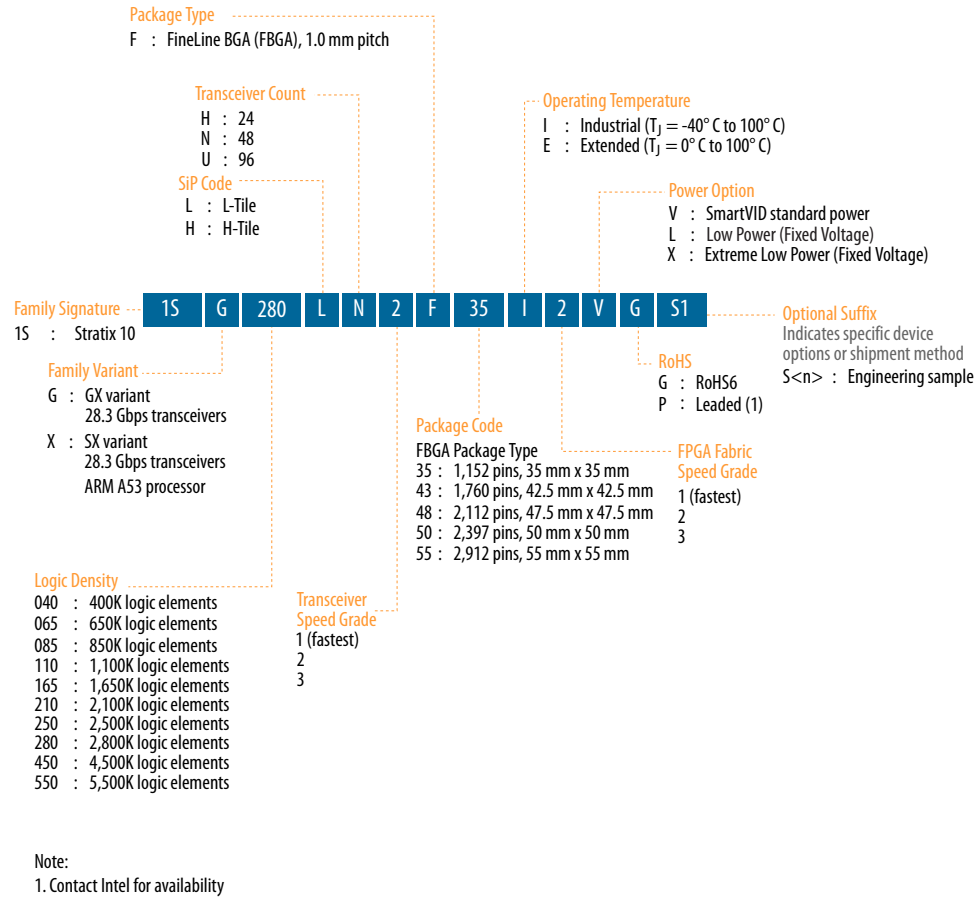
To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.



1.1.1. Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices



1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices

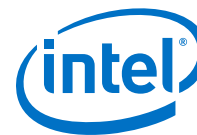
Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Process technology	28-nm TSMC (planar transistor)	14 nm Intel Tri-Gate (FinFET)
Hard processor core	None	Quad-core 64-bit ARM Cortex-A53 (SoC only)
Core architecture	Conventional core architecture with conventional interconnect	HyperFlex core architecture with Hyper-Registers in the interconnect
Core performance	500 MHz	1 GHz
Power dissipation	1x	As low as 0.3x
continued...		



Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Logic density	952 KLE (monolithic)	5,500 KLE (monolithic)
Embedded memory (M20K)	52 Mbits	229 Mbits
18x19 multipliers	3,926 <i>Note:</i> Multiplier is 18x18 in Stratix V devices.	11,520 <i>Note:</i> Multiplier is 18x19 in Intel Stratix 10 devices.
Floating point DSP capability	Up to 1 TFLOP, requires soft floating point adder and multiplier	Up to 10 TFLOPS, hard IEEE 754 compliant single precision floating point adder and multiplier
Maximum transceivers	66	96
Maximum transceiver data rate (chip-to-chip)	28.05 Gbps	28.3 Gbps L-Tile 28.3 Gbps H-Tile
Maximum transceiver data rate (backplane)	12.5 Gbps	12.5 Gbps L-Tile 28.3 Gbps H-Tile
Hard memory controller	None	DDR4 @ 1333 MHz/2666 Mbps DDR3 @ 1067 MHz/2133 Mbps
Hard protocol IP	PCIe Gen3 x8 (up to 4 instances)	PCIe Gen3 x16 (up to 4 instances) SR-IOV (4 physical functions / 2k virtual functions) on H-Tile devices 10GBASE-KR/40GBASE-KR4 FEC
Core clocking and PLLs	Global, quadrant and regional clocks supported by fractional-synthesis fPLLs	Programmable clock tree synthesis supported by fractional synthesis fPLLs and integer IO PLLs
Register state readback and writeback	Not available	Non-destructive register state readback and writeback for ASIC prototyping and other applications

These innovations result in the following improvements:

- **Improved Core Logic Performance:** The HyperFlex core architecture combined with Intel's 14-nm Tri-Gate technology allows Intel Stratix 10 devices to achieve 2X the core performance compared to the previous generation
- **Lower Power:** Intel Stratix 10 devices use up to 70% lower power compared to the previous generation, enabled by 14-nm Intel Tri-Gate technology, the HyperFlex core architecture, and optional power saving features built into the architecture
- **Higher Density:** Intel Stratix 10 devices offer over five times the level of integration, with up to 5,500K logic elements (LEs) in a monolithic fabric, over 229 Mbits of embedded memory blocks (M20K), and 11,520 18x19 multipliers
- **Embedded Processing:** Intel Stratix 10 SoCs feature a Quad-Core 64-bit ARM Cortex-A53 processor optimized for power efficiency and software compatible with previous generation Arria and Cyclone SoC devices
- **Improved Transceiver Performance:** With up to 96 transceiver channels implemented in heterogeneous 3D SiP transceiver tiles, Intel Stratix 10 GX and SX devices support data rates up to 28.3 Gbps chip-to-chip and 28.3 Gbps across the backplane with signal conditioning circuits capable of equalizing over 30 dB of system loss
- **Improved DSP Performance:** The variable precision DSP block in Intel Stratix 10 devices features hard fixed and floating point capability, with up to 10 TeraFLOPS IEEE754 single-precision floating point performance



Feature	Description
Power management	<ul style="list-style-type: none"> SmartVID controlled core voltage, standard power devices 0.85-V fixed core voltage, low static power devices available Intel Quartus® Prime Pro Edition integrated power analysis
High performance monolithic core fabric	<ul style="list-style-type: none"> HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks Monolithic fabric minimizes compile times and increases logic utilization Enhanced adaptive logic module (ALM) Improved multi-track routing architecture reduces congestion and improves compile times Hierarchical core clocking architecture with programmable clock tree synthesis Fine-grained partial reconfiguration
Internal memory blocks	<ul style="list-style-type: none"> M20K—20-Kbit with hard ECC support MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	<ul style="list-style-type: none"> IEEE 754-compliant hard single-precision floating point capability Supports signal processing with precision ranging from 18x19 up to 54x54 Native 27x27 and 18x19 multiply modes 64-bit accumulator and cascade for systolic FIRs Internal coefficient memory banks Pre-adder/subtractor improves efficiency Additional pipeline register increases performance and reduces power
Phase locked loops (PLL)	<ul style="list-style-type: none"> Fractional synthesis PLLs (fPLL) support both fractional and integer modes Fractional mode with third-order delta-sigma modulation Precision frequency synthesis Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering
Core clock networks	<ul style="list-style-type: none"> 1 GHz fabric clocking 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks Clocks only synthesized where needed, to minimize dynamic power
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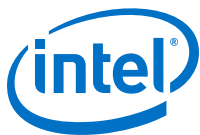


Intel Stratix 10 GX/SX Device Name	Interconnects		PLLs		Hard IP
	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 2800/ SX 2800	1160	96	32	24	4
GX 4500/ SX 4500	1640	24	8	34	1
GX 5500/ SX 5500	1640	24	8	34	1

Table 6. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 1Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers ⁽²⁾ ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾ ⁽⁶⁾ ⁽⁷⁾

Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm ²)	F1760 NF43 (42.5x42.5 mm ²)	F1760 NF43 (42.5x42.5 mm ²)
GX 400/ SX 400	392, 8, 192, 24		
GX 650/ SX 650	392, 8, 192, 24	400, 16, 192, 48	
GX 850/ SX 850			688, 16, 336, 48
GX 1100/ SX 1100			688, 16, 336, 48
GX 1650/ SX 1650			688, 16, 336, 48
GX 2100/ SX 2100			688, 16, 336, 48
GX 2500/ SX 2500			688, 16, 336, 48
GX 2800/ SX 2800			688, 16, 336, 48
continued...			

⁽²⁾ All packages are ball grid arrays with 1.0 mm pitch.⁽³⁾ High-Voltage I/O pins are used for 3 V and 2.5 V interfacing.⁽⁴⁾ Each LVDS pair can be configured as either a differential input or a differential output.⁽⁵⁾ High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.⁽⁶⁾ Each package column offers pin migration (common circuit board footprint) for all devices in the column.⁽⁷⁾ Intel Stratix 10 GX devices are pin migratable with Intel Stratix 10 SX devices in the same package.

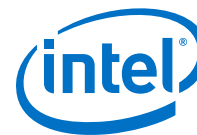


Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm ²)	F1760 NF43 (42.5x42.5 mm ²)	F1760 NF43 (42.5x42.5 mm ²)
SX 2800			
GX 4500/ SX 4500			
GX 5500/ SX 5500			

Table 7. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 2

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers ⁽²⁾ ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾ ⁽⁶⁾ ⁽⁷⁾

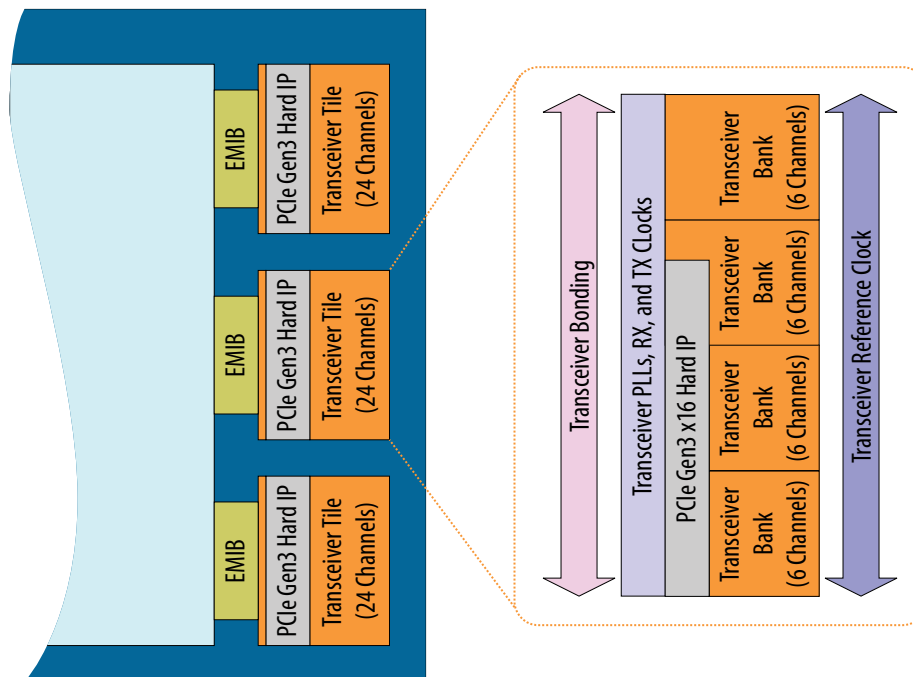
Intel Stratix 10 GX/SX Device Name	F2112 NF48 (47.5x47.5 mm ²)	F2397 UF50 (50x50 mm ²)	F2912 HF55 (55x55 mm ²)
GX 400/ SX 400			
GX 650/ SX 650			
GX 850/ SX 850	736, 16, 360, 48		
GX 1100/ SX 1100	736, 16, 360, 48		
GX 1650/ SX 1650		704, 32, 336, 96	
GX 2100/ SX 2100		704, 32, 336, 96	
GX 2500/ SX 2500		704, 32, 336, 96	1160, 8, 576, 24
GX 2800/ SX 2800		704, 32, 336, 96	1160, 8, 576, 24
GX 4500/ SX 4500			1640, 8, 816, 24
GX 5500/ SX 5500			1640, 8, 816, 24



Each transceiver tile contains:

- 24 full-duplex transceiver channels (PMA and PCS)
- Reference clock distribution network
- Transmit PLLs
- High-speed clocking and bonding networks
- One instance of PCI Express hard IP

Figure 6. Heterogeneous 3D SiP Transceiver Tile Architecture

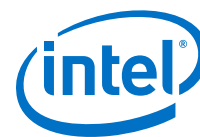
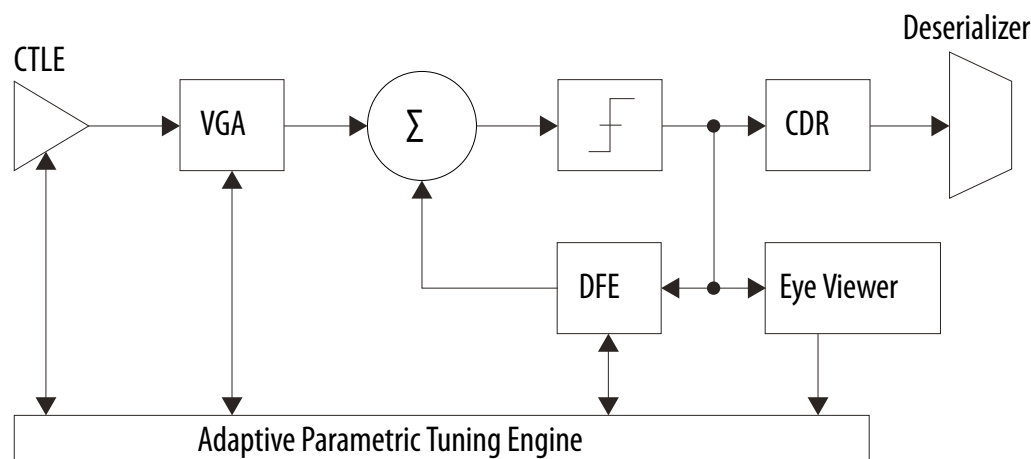


1.8. Intel Stratix 10 Transceivers

Intel Stratix 10 devices offer up to 96 total full-duplex transceiver channels. These channels provide continuous data rates from 1 Gbps to 28.3 Gbps for chip-to-chip, chip-to-module, and backplane applications. In each device, two thirds of the transceivers can be configured up to the maximum data rate of 28.3 Gbps to drive 100G interfaces and C form-factor pluggable CFP2/CFP4 optical modules. For longer-reach backplane driving applications, advanced adaptive equalization circuits are used to equalize over 30 dB of system loss.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

**Figure 7. Intel Stratix 10 Receiver Block Features**

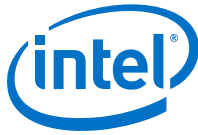
All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

Table 8. Transceiver PMA Features

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps ⁽⁸⁾ to 28.3 Gbps (Intel Stratix 10 GX/SX devices)
Backplane Support	Drive backplanes at data rates up to 28.3 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, QSFPDD, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	15 fixed tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Advanced Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols, with optional fractional frequency synthesis capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost

continued...

⁽⁸⁾ Stratix 10 transceivers can support data rates below 1 Gbps with over sampling.



Feature	Capability
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation—Eye Viewer and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (Eye Viewer). Also inject jitter from transmitter to test link margin in system.
Dynamic Reconfiguration	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility.
Multiple PCS-PMA and PCS-Core to FPGA fabric interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

1.8.2. PCS Features

Intel Stratix 10 PMA channels interface with core logic through configurable and bypassable PCS interface layers.

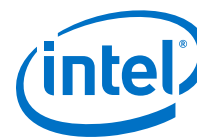
The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. This feature provides the flexibility to implement a wide range of applications with 8, 10, 16, 20, 32, 40, or 64-bit interface width between each transceiver and the core logic.

The PCS also contains hard IP to support a variety of standard and proprietary protocols across a wide range of data rates and encoding schemes. The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports 64B/66B and 64B/67B encoded applications up to 17.4 Gbps. The enhanced PCS mode also includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit. For highly customized implementations, a PCS Direct mode provides an interface up to 64 bits wide to allow for custom encoding and support for data rates up to 28.3 Gbps.

For more information about the PCS-Core interface or the double rate transfer mode, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*, and the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.

Table 9. Transceiver PCS Features

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	1 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x2, x4, x8, x16	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core
PCI Express Gen3 x1, x2, x4, x8, x16	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit-slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
continued...			



PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 12.5	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.3	Custom	Custom

Related Information

[Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide](#)

1.9. PCI Express Gen1/Gen2/Gen3 Hard IP

Intel Stratix 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, increased functionality, and designer productivity.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers. It also supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8/x16 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic (autonomous mode). This feature allows the PCI Express link to power up and complete link training in less than 100 ms, while the rest of the device is still in the process of being configured. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

The PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the device via protocol (CvP) across the PCI Express bus at Gen1/Gen2/Gen3 rates.

1.10. Interlaken PCS Hard IP

Intel Stratix 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Intel Stratix 10 devices.

1.11. 10G Ethernet Hard IP

Intel Stratix 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

The integrated serial transceivers simplify multi-port 10GbE systems compared to 10 GbE Attachment Unit Interface (XAUI) interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated transceivers incorporate signal conditioning circuits, which enable direct connection to standard 10G XFP and SFP+ pluggable optical modules. The transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

1.12. External Memory and General Purpose I/O

Intel Stratix 10 devices offer substantial external memory bandwidth, with up to ten 72-bit wide DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth is provided along with the ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. The external memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers.

Figure 8. Hard Memory Controller

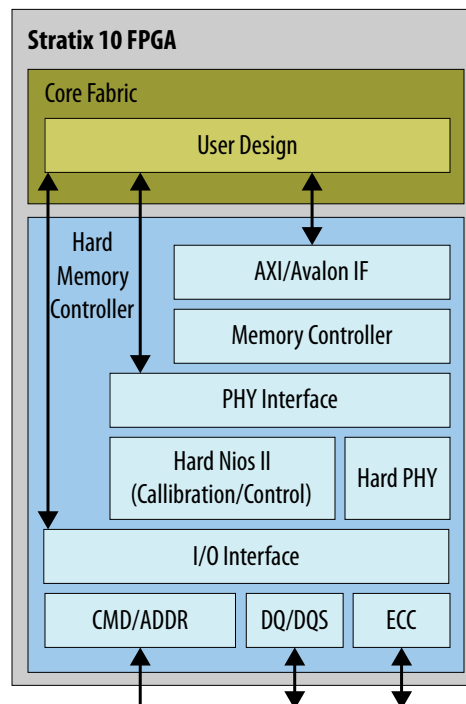
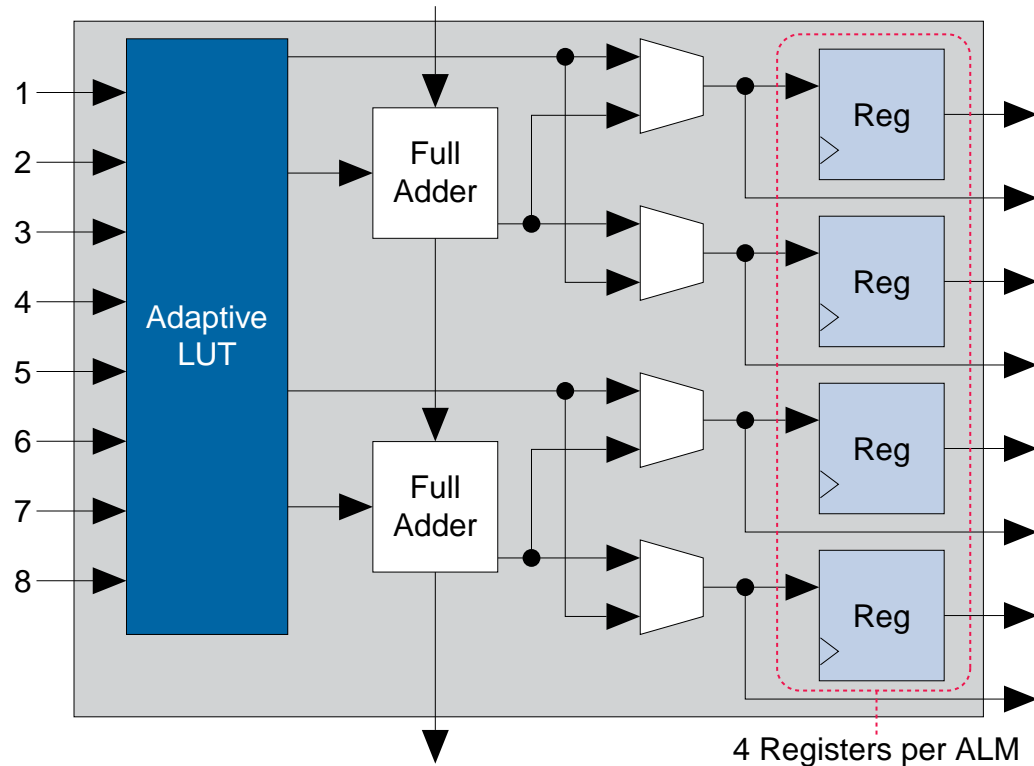


Figure 9. Intel Stratix 10 FPGA and SoC ALM Block Diagram



Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

1.14. Core Clocking

Core clocking in Intel Stratix 10 devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.



The core clock network in Intel Stratix 10 devices supports the new HyperFlex core architecture at clock rates up to 1 GHz. It also supports the hard memory controllers up to 2666 Mbps with a quarter rate transfer to the core. The core clock network is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

1.15. Fractional Synthesis PLLs and I/O PLLs

Intel Stratix 10 devices have up to 32 fractional synthesis PLLs (fPLL) available for use with transceivers or in the core fabric.

The fPLLs are located in the 3D SiP transceiver H-tiles, eight per tile, adjacent to the transceiver channels. The fPLLs can be used to reduce both the number of oscillators required on the board and the number of clock pins required, by synthesizing multiple clock frequencies from a single reference clock source. In addition to synthesizing reference clock frequencies for the transceiver transmit PLLs, the fPLLs can also be used directly for transmit clocking. Each fPLL can be independently configured for conventional integer mode, or enhanced fractional synthesis mode with third-order delta-sigma modulation.

In addition to the fPLLs, Intel Stratix 10 devices contain up to 34 integer I/O PLLs (IOPLLs) available for general purpose use in the core fabric and for simplifying the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are located in each bank of 48 general purpose I/O, 1 per I/O bank, adjacent to the hard memory controllers and LVDS SerDes in each I/O bank. This makes it easier to close timing because the IOPLLs are tightly coupled with the I/Os that need to use them. The IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay clock buffering.

1.16. Internal Embedded Memory

Intel Stratix 10 devices contain two types of embedded memory blocks: M20K (20-Kbit) and MLAB (640-bit).

The M20K and MLAB blocks are familiar block sizes carried over from previous Intel device families. The MLAB blocks are ideal for wide and shallow memories, while the M20K blocks are intended to support larger memory configurations and include hard ECC. Both M20K and MLAB embedded memory blocks can be configured as a single-port or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are highly flexible and support a number of memory configurations as shown in [Table 11](#) on page 25.

Table 11. Internal Embedded Memory Block Configurations

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation) 32 x 20	2K x 10 (or x8) 1K x 20 (or x16) 512 x 40 (or x32)

1.17. Variable Precision DSP Block

The Intel Stratix 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE-754 compliant floating point capability.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

Figure 10. DSP Block: Standard Precision Fixed Point Mode

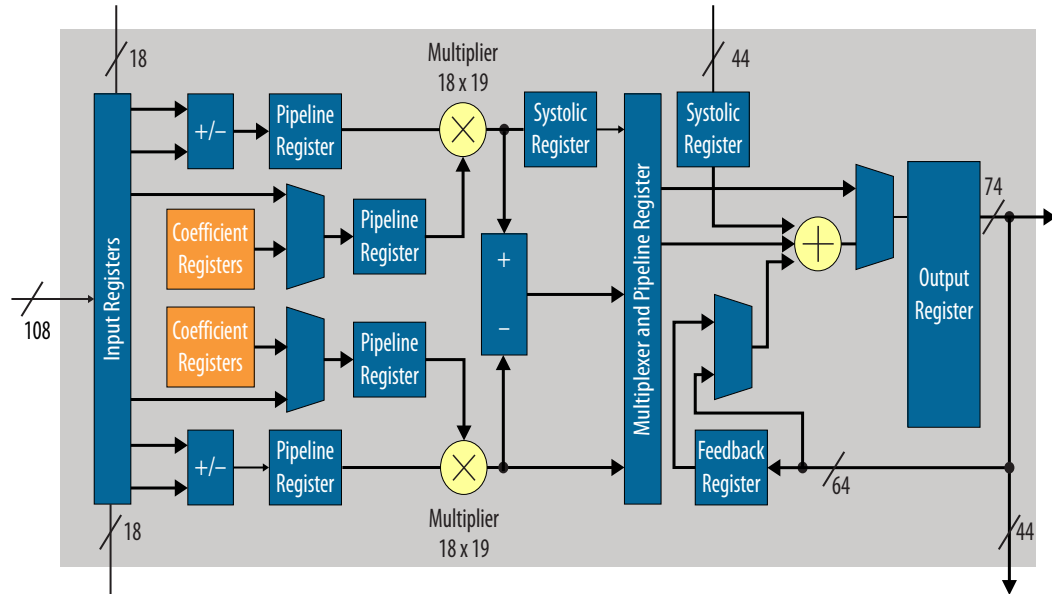
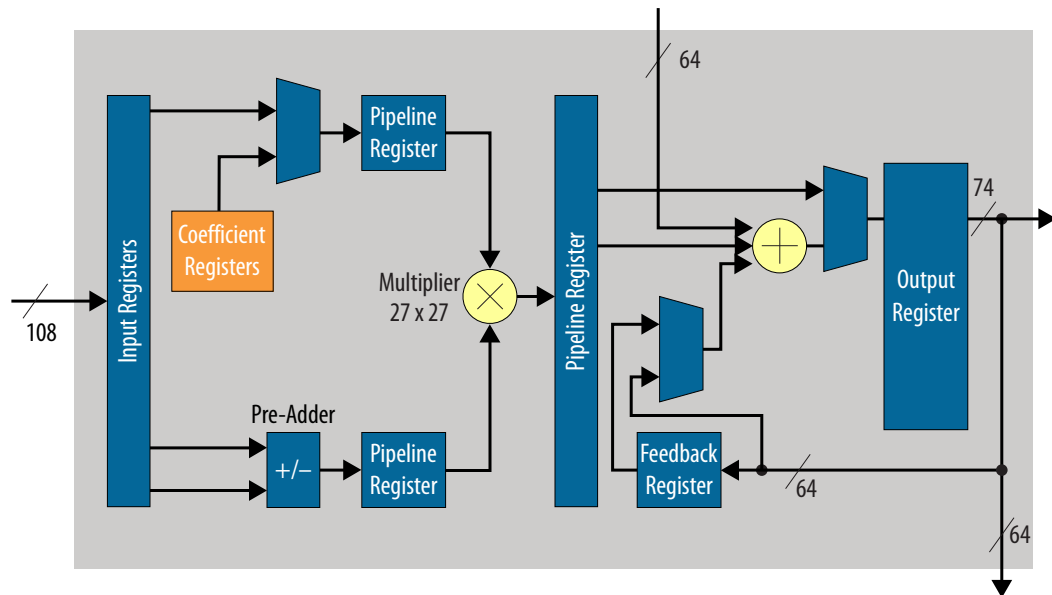
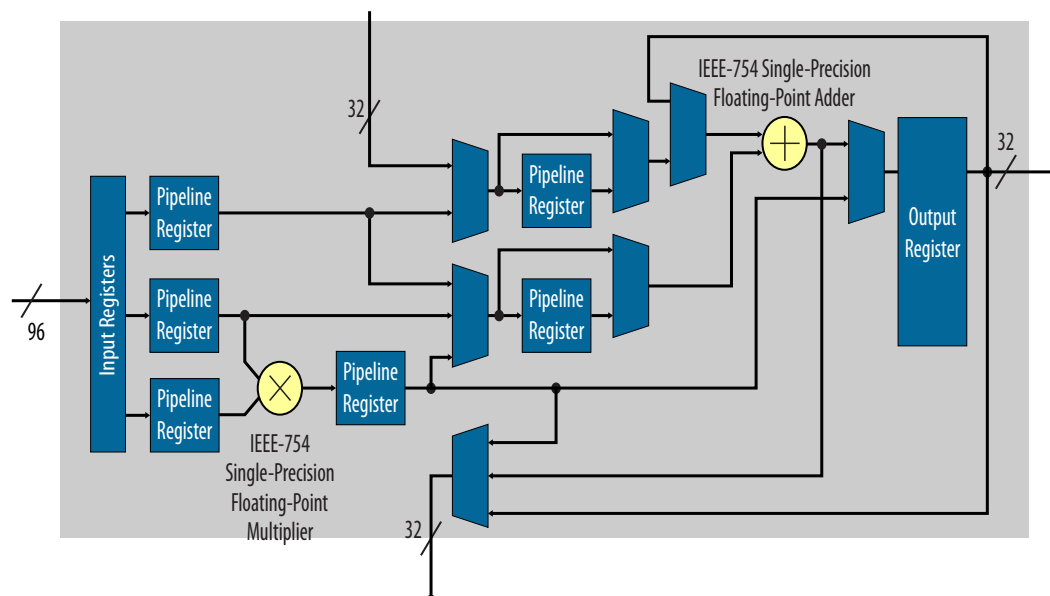


Figure 11. DSP Block: High Precision Fixed Point Mode



**Figure 12. DSP Block: Single Precision Floating Point Mode**

Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

Table 12. Variable Precision DSP Block Configurations

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point
Single Precision floating point	1 Single Precision floating point adder, 1 Single Precision floating point multiplier	Floating point



Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

Table 13. Complex Multiplication With Variable Precision DSP Block

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFT
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT

For FFT applications with high dynamic range requirements, the Intel FFT IP Core offers an option of single precision floating point implementation with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

- Hard 18-bit and 25-bit pre-adders
- Hard floating point multipliers and adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Intel Quartus Prime software for most modes

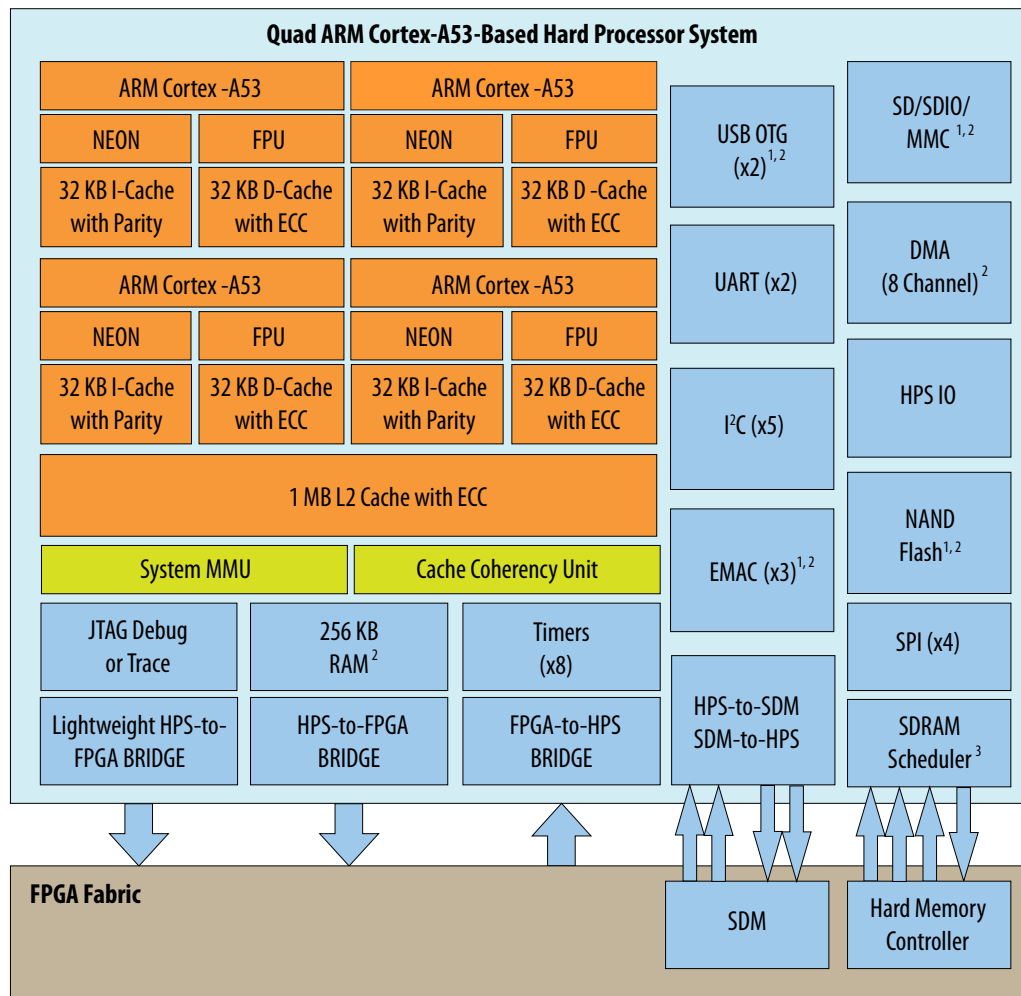
The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. With the Variable Precision DSP block architecture and hard floating point multipliers and adders, Intel Stratix 10 devices can efficiently support many different precision levels up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

1.18. Hard Processor System (HPS)

The Intel Stratix 10 SoC Hard Processor System (HPS) is Intel's industry leading third generation HPS. Leveraging the performance of Intel's 14-nm Tri-Gate technology, Intel Stratix 10 SoC devices more than double the performance of previous generation SoCs with an integrated quad-core 64-bit ARM Cortex-A53. The HPS also enables system-wide hardware virtualization capabilities by adding a system memory management unit. These architecture improvements ensure that Intel Stratix 10 SoCs will meet the requirements of current and future embedded markets, including wireless and wireline communications, data center acceleration, and numerous military applications.



Figure 13. HPS Block Diagram



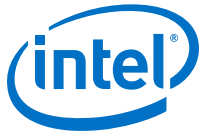
- Notes:
1. Integrated direct memory access (DMA)
 2. Integrated error correction code (ECC)
 3. Multiport front-end interface to hard memory controller

1.18.1. Key Features of the Intel Stratix 10 HPS

Table 14. Key Features of the Intel Stratix 10 GX/SX HPS

Feature	Description
Quad-core ARM Cortex-A53 MPCore processor unit	<ul style="list-style-type: none"> • 2.3 MIPS/MHz instruction efficiency • CPU frequency up to 1.5 GHz • At 1.5 GHz total performance of 13,800 MIPS • ARMv8-A architecture • Runs 64-bit and 32-bit ARM instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Jazelle® RCT execution architecture with 8-bit Java bytecodes

continued...



1.19. Power Management

Intel Stratix 10 devices leverage the advanced Intel 14-nm Tri-Gate process technology, the all new HyperFlex core architecture to enable Hyper-Folding, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

With the new HyperFlex core architecture, designs can run 2X faster than previous generation FPGAs. With 2X performance and same required throughput, architects can cut the data path width in half to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

The optional power reduction techniques in Intel Stratix 10 devices include:

- **Available Low Static Power Devices**—Intel Stratix 10 devices are available with a fixed core voltage that provides lower static power than the SmartVID standard power devices, while maintaining device performance

Furthermore, Intel Stratix 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

1.20. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.



The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be