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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

### Details

| | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Quad ARM® Cortex®-A53 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 2800K Logic Elements |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 1760-BBGA, FCBGA |
| Supplier Device Package | 1760-FBGA, FC (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/1sx280ln2f43e2vgs1 |

# Contents

- Dedicated secure device manager (SDM) for:
    - Enhanced device configuration and security
    - AES-256, SHA-256/384 and ECDSA-256/384 encrypt/decrypt accelerators and authentication
    - Multi-factor authentication
    - Physically Unclonable Function (PUF) service and software programmable device configuration capability
- Comprehensive set of advanced power saving features delivering up to 70% lower power compared to previous generation high-performance FPGAs
- Non-destructive register state readback and writeback, to support ASIC prototyping and other applications

With these capabilities, Intel Stratix 10 FPGAs and SoCs are ideally suited for the most demanding applications in diverse markets such as:

- **Compute and Storage**—for custom servers, cloud computing and data center acceleration
- **Networking**—for Terabit, 400G and multi-100G bridging, aggregation, packet processing and traffic management
- **Optical Transport Networks**—for OTU4, 2xOTU4, 4xOTU4
- **Broadcast**—for high-end studio distribution, headend encoding/decoding, edge quadrature amplitude modulation (QAM)
- **Military**—for radar, electronic warfare, and secure communications
- **Medical**—for diagnostic scanners and diagnostic imaging
- **Test and Measurement**—for protocol and application testers
- **Wireless**—for next-generation 5G networks
- **ASIC Prototyping**—for designs that require the largest monolithic FPGA fabric with the highest I/O count

## 1.1. Intel Stratix 10 Family Variants

Intel Stratix 10 devices are available in FPGA (GX) and SoC (SX) variants.

- **Intel Stratix 10 GX** devices deliver up to 1 GHz core fabric performance and contain up to 5.5 million LEs in a monolithic fabric. They also feature up to 96 general purpose transceivers on separate transceiver tiles, and 2666 Mbps DDR4 external memory interface performance. The transceivers are capable of up to 28.3 Gbps short reach and across the backplane. These devices are optimized for FPGA applications that require the highest transceiver bandwidth and core fabric performance, with the power efficiency of Intel's industry-leading 14-nm Tri-Gate process technology.
- **Intel Stratix 10 SX** devices have a feature set that is identical to Intel Stratix 10 GX devices, with the addition of an embedded quad-core 64-bit ARM Cortex A53 hard processor system.

Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

• M20K (20 kbit) embedded memory blocks

• Variable precision DSP blocks with hard IEEE 754 compliant floating-point units

• Fractional synthesis and integer PLLs

• Hard memory controllers and PHY for external memory interfaces

• General purpose IO cells

To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.

## 1.1.1. Available Options

**Figure 1.** Sample Ordering Code and Available Options for Intel Stratix 10 Devices



Package Type
F : FineLine BGA (FBGA), 1.0 mm pitch

Transceiver Count
H : 24
N : 48
U : 96

SiP Code
L : L-Tile
H : H-Tile

Operating Temperature
I : Industrial (T_J = -40° C to 100° C)
E : Extended (T_J = 0° C to 100° C)

Power Option
V : SmartVID standard power
L : Low Power (Fixed Voltage)
X : Extreme Low Power (Fixed Voltage)

Family Signature
1S : Stratix 10

`1S  G  280  L  N  2  F  35  I  2  V  G  S1`

Optional Suffix
Indicates specific device
options or shipment method
S<n> : Engineering sample

Family Variant
G : GX variant
28.3 Gbps transceivers
X : SX variant
28.3 Gbps transceivers
ARM A53 processor

RoHS
G : RoHS6
P : Leaded (1)

Package Code
FBGA Package Type
35 : 1,152 pins, 35 mm x 35 mm
43 : 1,760 pins, 42.5 mm x 42.5 mm
48 : 2,112 pins, 47.5 mm x 47.5 mm
50 : 2,397 pins, 50 mm x 50 mm
55 : 2,912 pins, 55 mm x 55 mm

FPGA Fabric
Speed Grade
1 (fastest)
2
3

Logic Density
040 : 400K logic elements
065 : 650K logic elements
085 : 850K logic elements
110 : 1,100K logic elements
165 : 1,650K logic elements
210 : 2,100K logic elements
250 : 2,500K logic elements
280 : 2,800K logic elements
450 : 4,500K logic elements
550 : 5,500K logic elements

Transceiver
Speed Grade
1 (fastest)
2
3

Note:
1. Contact Intel for availability

## 1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

**Table 1.** Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices

| Feature | Stratix V FPGAs | Intel Stratix 10 FPGAs and SoCs |
|---|---|---|
| Process technology | 28-nm TSMC (planar transistor) | 14 nm Intel Tri-Gate (FinFET) |
| Hard processor core | None | Quad-core 64-bit ARM Cortex-A53 (SoC only) |
| Core architecture | Conventional core architecture with conventional interconnect | HyperFlex core architecture with Hyper-Registers in the interconnect |
| Core performance | 500 MHz | 1 GHz |
| Power dissipation | 1x | As low as 0.3x |
| | | *continued...* |

| Feature | Stratix V FPGAs | Intel Stratix 10 FPGAs and SoCs |
|---|---|---|
| Logic density | 952 KLE (monolithic) | 5,500 KLE (monolithic) |
| Embedded memory (M20K) | 52 Mbits | 229 Mbits |
| 18x19 multipliers | 3,926 <br> *Note:* Multiplier is 18x18 in Stratix V devices. | 11,520 <br> *Note:* Multiplier is 18x19 in Intel Stratix 10 devices. |
| Floating point DSP capability | Up to 1 TFLOP, requires soft floating point adder and multiplier | Up to 10 TFLOPS, hard IEEE 754 compliant single precision floating point adder and multiplier |
| Maximum transceivers | 66 | 96 |
| Maximum transceiver data rate (chip-to-chip) | 28.05 Gbps | 28.3 Gbps L-Tile <br> 28.3 Gbps H-Tile |
| Maximum transceiver data rate (backplane) | 12.5 Gbps | 12.5 Gbps L-Tile <br> 28.3 Gbps H-Tile |
| Hard memory controller | None | DDR4 @ 1333 MHz/2666 Mbps <br> DDR3 @ 1067 MHz/2133 Mbps |
| Hard protocol IP | PCIe Gen3 x8 (up to 4 instances) | PCIe Gen3 x16 (up to 4 instances) <br> SR-IOV (4 physical functions / 2k virtual functions) on H-Tile devices <br> 10GBASE-KR/40GBASE-KR4 FEC |
| Core clocking and PLLs | Global, quadrant and regional clocks supported by fractional-synthesis fPLLs | Programmable clock tree synthesis supported by fractional synthesis fPLLs and integer IO PLLs |
| Register state readback and writeback | Not available | Non-destructive register state readback and writeback for ASIC prototyping and other applications |

These innovations result in the following improvements:

- **Improved Core Logic Performance**: The HyperFlex core architecture combined with Intel's 14-nm Tri-Gate technology allows Intel Stratix 10 devices to achieve 2X the core performance compared to the previous generation

- **Lower Power**: Intel Stratix 10 devices use up to 70% lower power compared to the previous generation, enabled by 14-nm Intel Tri-Gate technology, the HyperFlex core architecture, and optional power saving features built into the architecture

- **Higher Density**: Intel Stratix 10 devices offer over five times the level of integration, with up to 5,500K logic elements (LEs) in a monolithic fabric, over 229 Mbits of embedded memory blocks (M20K), and 11,520 18x19 multipliers

- **Embedded Processing**: Intel Stratix 10 SoCs feature a Quad-Core 64-bit ARM Cortex-A53 processor optimized for power efficiency and software compatible with previous generation Arria and Cyclone SoC devices

- **Improved Transceiver Performance**: With up to 96 transceiver channels implemented in heterogeneous 3D SiP transceiver tiles, Intel Stratix 10 GX and SX devices support data rates up to 28.3 Gbps chip-to-chip and 28.3 Gbps across the backplane with signal conditioning circuits capable of equalizing over 30 dB of system loss

- **Improved DSP Performance**: The variable precision DSP block in Intel Stratix 10 devices features hard fixed and floating point capability, with up to 10 TeraFLOPS IEEE754 single-precision floating point performance

| SoC Subsystem | Feature | Description |
|---|---|---|
| | NAND flash controller | • 1 ONFI 1.0, 8- and 16-bit support |
| | General-purpose I/O (GPIO) | • Maximum of 48 software programmable GPIO |
| | Timers | • 4 general-purpose timers<br>• 4 watchdog timers |
| Secure Device Manager | Security | • Secure boot<br>• Advanced Encryption Standard (AES) and authentication (SHA/ECDSA) |
| External Memory Interface | External Memory Interface | • Hard Memory Controller with DDR4 and DDR3, and LPDDR3 |

## 1.4. Intel Stratix 10 Block Diagram

**Figure 2.     Intel Stratix 10 FPGA and SoC Architecture Block Diagram**
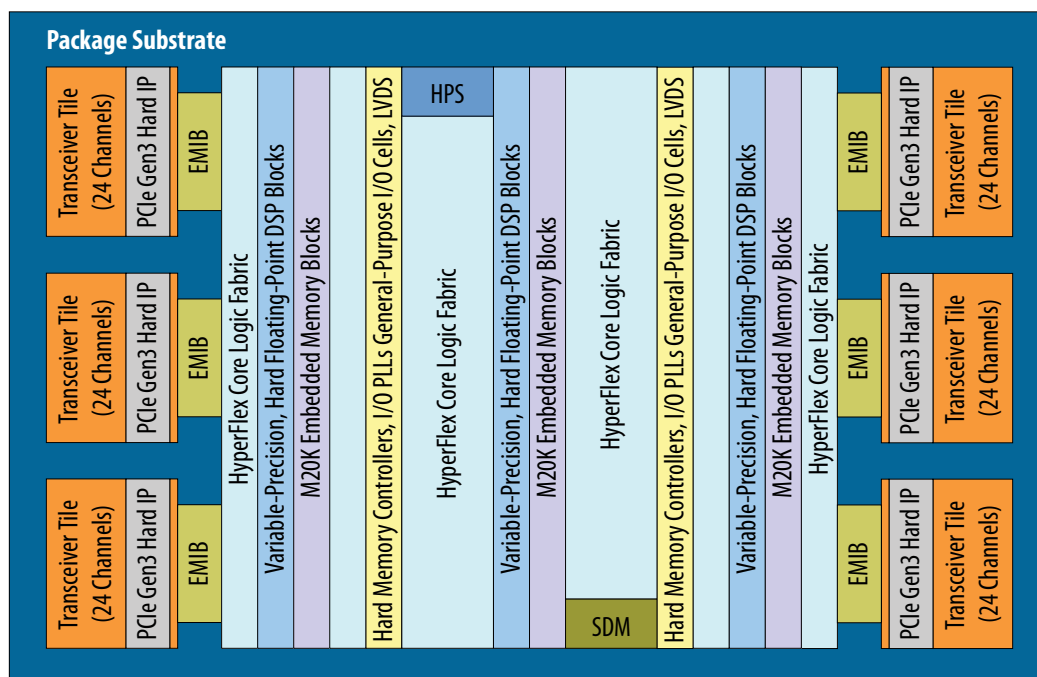


HPS: Quad ARM Cortex-A53 Hard Processor System
SDM: Secure Device Manager
EMIB: Embedded Multi-Die Interconnect Bridge

## 1.5.  Intel Stratix 10 FPGA and SoC Family Plan

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(1)  The number of 27x27 multipliers is one-half the number of 18x19 multipliers.

**Table 4.        Intel Stratix 10 GX/SX FPGA and SoC Family Plan—FPGA Core (part 1)**

| Intel Stratix 10 GX/SX Device Name | Logic Elements (KLE) | M20K Blocks | M20K Mbits | MLAB Counts | MLAB Mbits | 18x19 Multi-pliers [1] |
|---|---|---|---|---|---|---|
| GX 400/ SX 400 | 378 | 1,537 | 30 | 3,204 | 2 | 1,296 |
| GX 650/ SX 650 | 612 | 2,489 | 49 | 5,184 | 3 | 2,304 |
| GX 850/ SX 850 | 841 | 3,477 | 68 | 7,124 | 4 | 4,032 |
| GX 1100/ SX 1100 | 1,092 | 4,401 | 86 | 9,540 | 6 | 5,040 |
| GX 1650/ SX 1650 | 1,624 | 5,851 | 114 | 13,764 | 8 | 6,290 |
| GX 2100/ SX 2100 | 2,005 | 6,501 | 127 | 17,316 | 11 | 7,488 |
| GX 2500/ SX 2500 | 2,422 | 9,963 | 195 | 20,529 | 13 | 10,022 |
| GX 2800/ SX 2800 | 2,753 | 11,721 | 229 | 23,796 | 15 | 11,520 |
| GX 4500/ SX 4500 | 4,463 | 7,033 | 137 | 37,821 | 23 | 3,960 |
| GX 5500/ SX 5500 | 5,510 | 7,033 | 137 | 47,700 | 29 | 3,960 |

**Table 5.        Intel Stratix 10 GX/SX FPGA and SoC Family Plan—Interconnects, PLLs and Hard IP (part 2)**

| Intel Stratix 10 GX/SX Device Name | Interconnects | | PLLs | | Hard IP |
|---|---|---|---|---|---|
| | Maximum GPIOs | Maximum XCVR | fPLLs | I/O PLLs | PCIe Hard IP Blocks |
| GX 400/ SX 400 | 392 | 24 | 8 | 8 | 1 |
| GX 650/ SX 650 | 400 | 48 | 16 | 8 | 2 |
| GX 850/ SX 850 | 736 | 48 | 16 | 15 | 2 |
| GX 1100/ SX 1100 | 736 | 48 | 16 | 15 | 2 |
| GX 1650/ SX 1650 | 704 | 96 | 32 | 14 | 4 |
| GX 2100/ SX 2100 | 704 | 96 | 32 | 14 | 4 |
| GX 2500/ SX 2500 | 1160 | 96 | 32 | 24 | 4 |

*continued...*
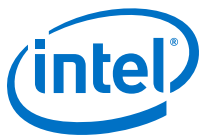
| Intel Stratix 10 GX/SX Device Name | F1152 HF35 (35x35 mm$^2$) | F1760 NF43 (42.5x42.5 mm$^2$) | F1760 NF43 (42.5x42.5 mm$^2$) |
|---|---|---|---|
| SX 2800 | | | |
| GX 4500/ SX 4500 | | | |
| GX 5500/ SX 5500 | | | |

**Table 7.     Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 2**

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers [2] [3] [4] [5] [6] [7]

| Intel Stratix 10 GX/SX Device Name | F2112 NF48 (47.5x47.5 mm$^2$) | F2397 UF50 (50x50 mm$^2$) | F2912 HF55 (55x55 mm$^2$) |
|---|---|---|---|
| GX 400/ SX 400 | | | |
| GX 650/ SX 650 | | | |
| GX 850/ SX 850 | 736, 16, 360, 48 | | |
| GX 1100/ SX 1100 | 736, 16, 360, 48 | | |
| GX 1650/ SX 1650 | | 704, 32, 336, 96 | |
| GX 2100/ SX 2100 | | 704, 32, 336, 96 | |
| GX 2500/ SX 2500 | | 704, 32, 336, 96 | 1160, 8, 576, 24 |
| GX 2800/ SX 2800 | | 704, 32, 336, 96 | 1160, 8, 576, 24 |
| GX 4500/ SX 4500 | | | 1640, 8, 816, 24 |
| GX 5500/ SX 5500 | | | 1640, 8, 816, 24 |

**Figure 4.** **HyperFlex Core Architecture**



■ New Hyper-Registers throughout the core fabric
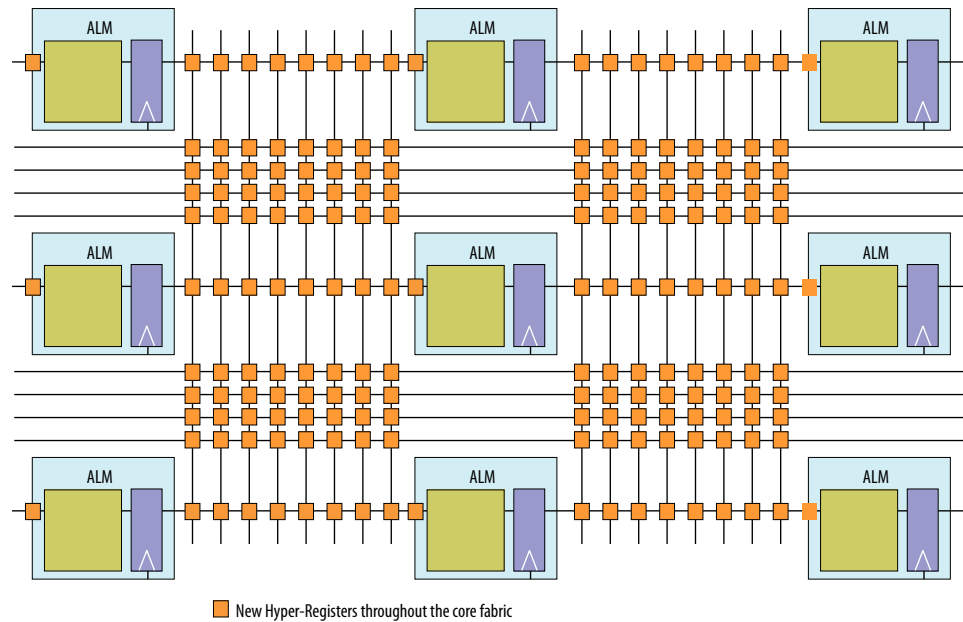
## 1.7. Heterogeneous 3D SiP Transceiver Tiles

Intel Stratix 10 FPGAs and SoCs feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles, each containing 24 full-duplex transceiver channels. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

**Figure 5.** **Monolithic Core Fabric and Heterogeneous 3D SiP Transceiver Tiles**
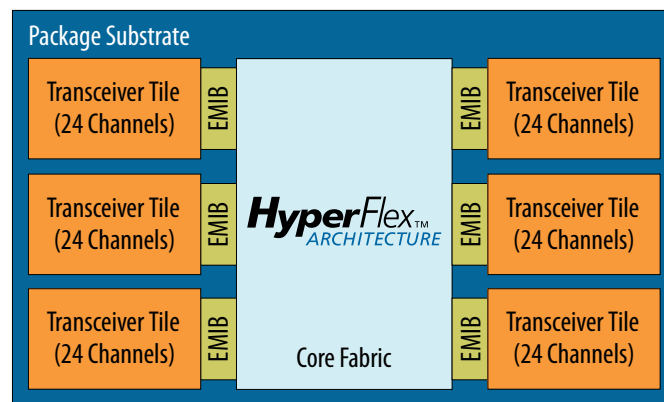
Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

## 1.8.1. PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- **ATX PLL**—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.

- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.

- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- **Variable Gain Amplifier (VGA)**—to optimize the receiver's dynamic range

- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation

- **Decision Feedback Equalizer (DFE)**—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections

- **On-Die Instrumentation (ODI)**—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing

**Figure 7.    Intel Stratix 10 Receiver Block Features**
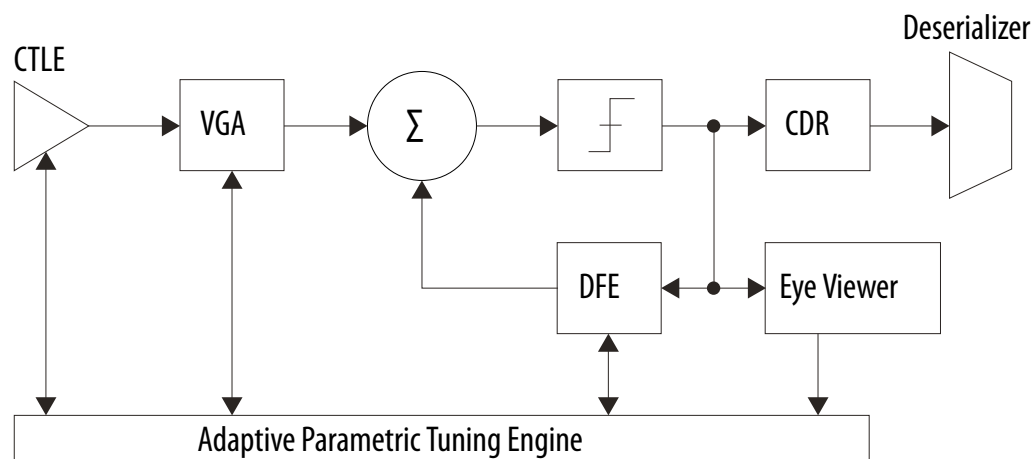


All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

**Table 8.    Transceiver PMA Features**

| Feature | Capability |
|---------|------------|
| Chip-to-Chip Data Rates | 1 Gbps [8] to 28.3 Gbps (Intel Stratix 10 GX/SX devices) |
| Backplane Support | Drive backplanes at data rates up to 28.3 Gbps, including 10GBASE-KR compliance |
| Optical Module Support | SFP+/SFP, XFP, CXP, QSFP/QSFP28, QSFPDD, CFP/CFP2/CFP4 |
| Cable Driving Support | SFP+ Direct Attach, PCI Express over cable, eSATA |
| Transmit Pre-Emphasis | 5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss |
| Continuous Time Linear Equalizer (CTLE) | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss |
| Decision Feedback Equalizer (DFE) | 15 fixed tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments |
| Advanced Digital Adaptive Parametric Tuning (ADAPT) | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance |
| ATX Transmit PLLs | Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols, with optional fractional frequency synthesis capability |
| Fractional PLLs | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost |
| | *continued...* |

[8]  Stratix 10 transceivers can support data rates below 1 Gbps with over sampling.

| PCS Protocol Support | Data Rate (Gbps) | Transmitter Data Path | Receiver Data Path |
|---|---|---|---|
| Enhanced PCS | 2.5 to 17.4 | FIFO, channel bonding, bit-slipper, and gear box | FIFO, block sync, bit-slipper, and gear box |
| 10GBASE-R | 10.3125 | FIFO, 64B/66B encoder, scrambler, FEC, and gear box | FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box |
| Interlaken | 4.9 to 17.4 | FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box | FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box |
| SFI-S/SFI-5.2 | 11.3 | FIFO, channel bonding, bit-slipper, and gear box | FIFO, bit-slipper, and gear box |
| IEEE 1588 | 1.25 to 10.3125 | FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box | FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box |
| SDI | up to 12.5 | FIFO and gear box | FIFO, bit-slipper, and gear box |
| GigE | 1.25 | Same as Standard PCS plus GigE state machine | Same as Standard PCS plus GigE state machine |
| PCS Direct | up to 28.3 | Custom | Custom |

**Related Information**

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

## 1.9. PCI Express Gen1/Gen2/Gen3 Hard IP

Intel Stratix 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, increased functionality, and designer productivity.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers. It also supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8/x16 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic (autonomous mode). This feature allows the PCI Express link to power up and complete link training in less than 100 ms, while the rest of the device is still in the process of being configured. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

The PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the device via protocol (CvP) across the PCI Express bus at Gen1/Gen2/Gen3 rates.

## 1.10. Interlaken PCS Hard IP

Intel Stratix 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Intel Stratix 10 devices.
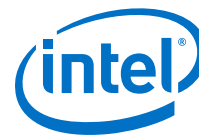
Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling

- FIFO buffering to lower latency and improve margin

- Timing calibration

- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

**Table 10.  External Memory Interface Performance**

The listed speeds are for the 1-rank case.

| Interface | Controller Type | Performance |
|---|---|---|
| DDR4 | Hard | 2666 Mbps |
| DDR3 | Hard | 2133 Mbps |
| QDRII+ | Soft | 1,100 Mtps |
| QDRII+ Xtreme | Soft | 1,266 Mtps |
| QDRIV | Soft | 2,133 Mtps |
| RLDRAM III | Soft | 2400 Mbps |
| RLDRAM II | Soft | 533 Mbps |

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

# 1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

**Figure 9.    Intel Stratix 10 FPGA and SoC ALM Block Diagram**
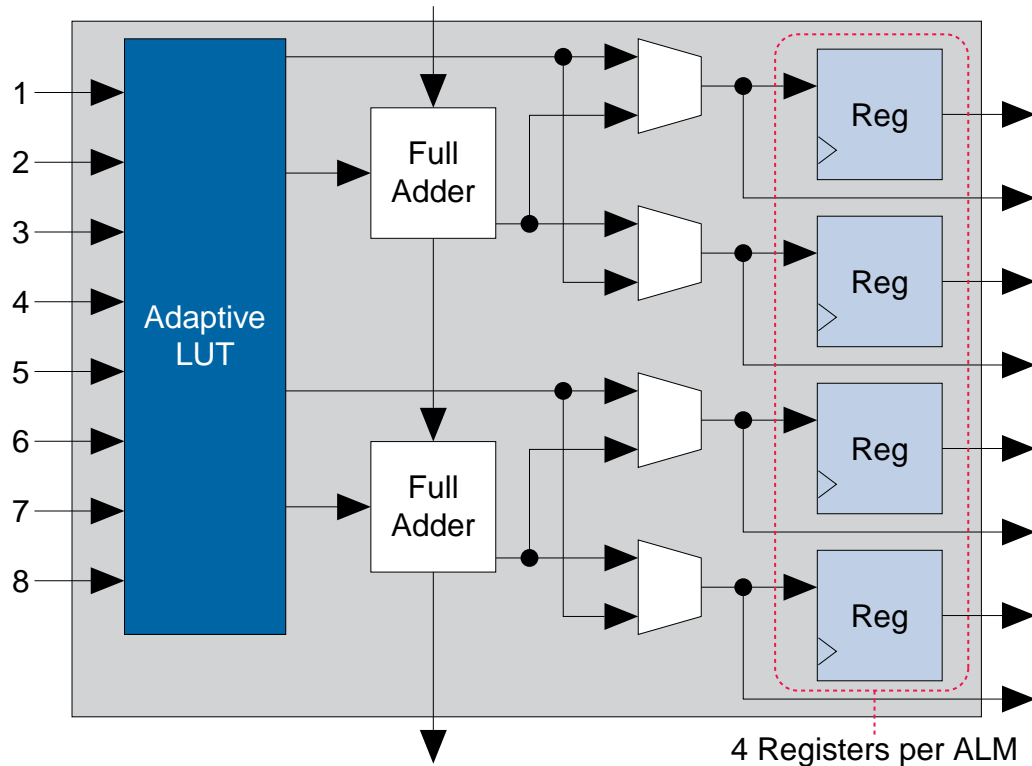


Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization

- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

## 1.14.  Core Clocking

Core clocking in Intel Stratix 10 devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.

**Figure 12.    DSP Block: Single Precision Floating Point Mode**
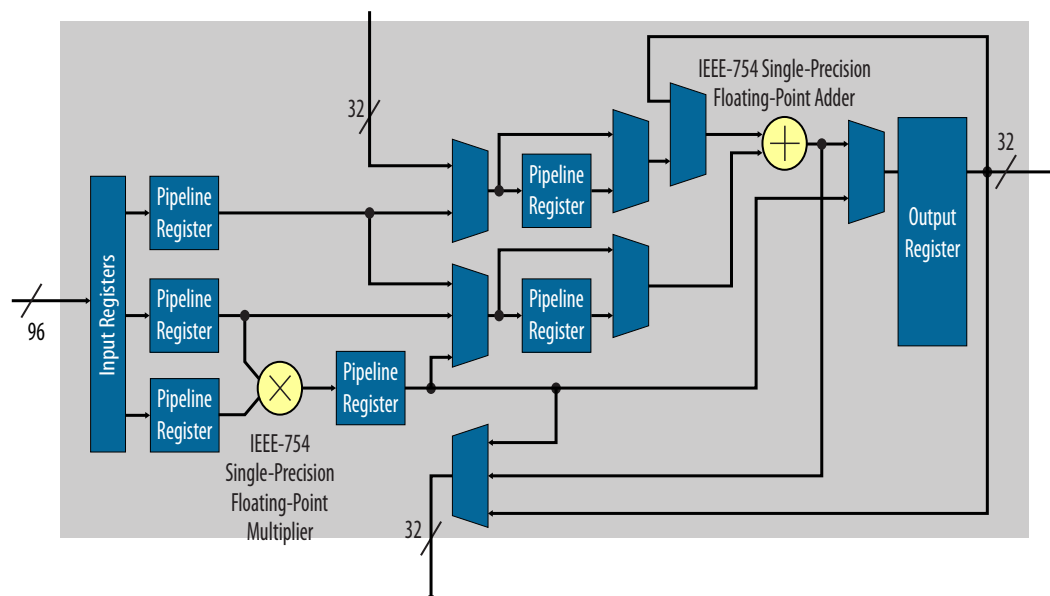


Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

**Table 12.    Variable Precision DSP Block Configurations**

| Multiplier Size | DSP Block Resources | Expected Usage |
|---|---|---|
| 18x19 bits | 1/2 of Variable Precision DSP Block | Medium precision fixed point |
| 27x27 bits | 1 Variable Precision DSP Block | High precision fixed point |
| 19x36 bits | 1 Variable Precision DSP Block with external adder | Fixed point FFTs |
| 36x36 bits | 2 Variable Precision DSP Blocks with external adder | Very high precision fixed point |
| 54x54 bits | 4 Variable Precision DSP Blocks with external adder | Double Precision floating point |
| Single Precision floating point | 1 Single Precision floating point adder, 1 Single Precision floating point multiplier | Floating point |

(intel®)

**Figure 14.  SDM Block Diagram**
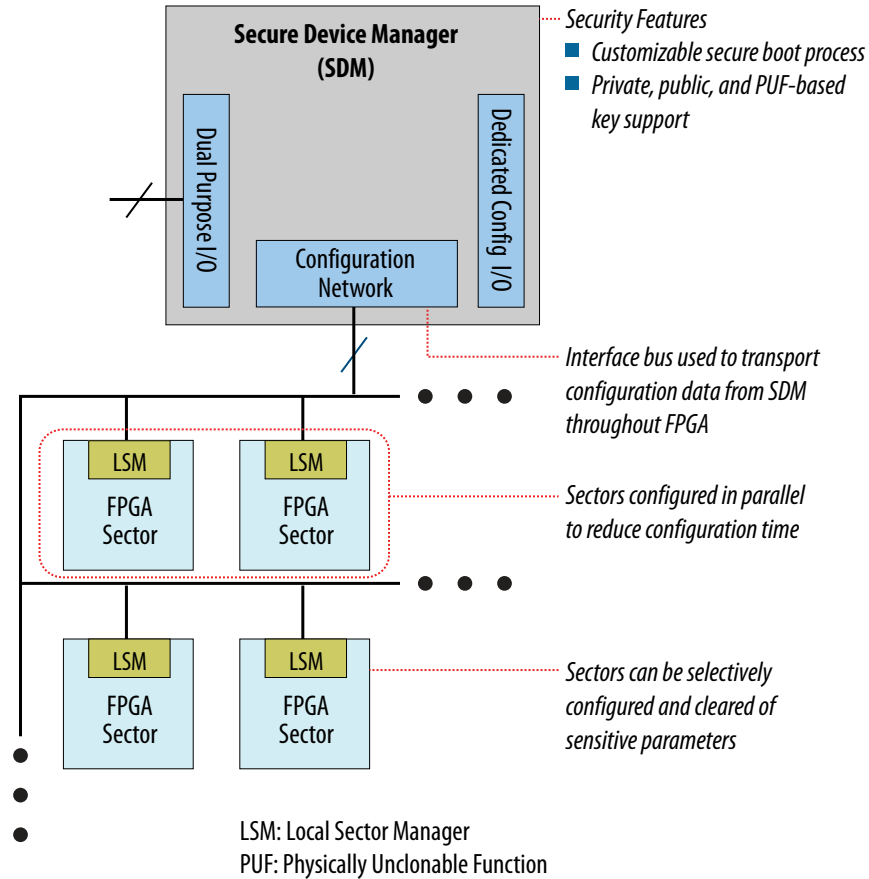


During configuration, Intel Stratix 10 devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.

The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager

- Reduced device configuration time, because sectors are configured in parallel

- Updateable configuration process

- Reconfiguration of one or more sectors independent of all other sectors

- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

## 1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption

- Multi-factor authentication

- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384

- Volatile and non-volatile encryption key storage and management

- Boot code authentication for the HPS

- Physically Unclonable Function (PUF) service

- Updateable configuration process

- Secure device maintenance and upgrade functions

- Side channel attack protection

- Scripted response to sensor inputs and security attacks, including selective sector zeroization

- Readback, JTAG and test mode disable

- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

## 1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be

powered up and active within the 100 ms time allowed by the PCI Express specification. Intel Stratix 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

## 1.23. Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Intel Quartus Prime design software

Dynamic reconfiguration in Intel Stratix 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multiprotocol or multi-rate support. Both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

## 1.24. Fast Forward Compile

The innovative Fast Forward Compile feature in the Intel Quartus Prime software identifies performance bottlenecks in your design and provides detailed, step-by-step performance improvement recommendations that you can then implement. The Compiler reports estimates of the maximum operating frequency that can be achieved by applying the recommendations. As part of the new Hyper-Aware design flow, Fast Forward Compile maximizes the performance of your Intel Stratix 10 design and achieves rapid timing closure.

Previously, this type of optimization required multiple time-consuming design iterations, including full design re-compilation to determine the effectiveness of the changes. Fast Forward Compile enables you to make better decisions about where to focus your optimization efforts, and how to increase your design performance and throughput. This technique removes much of the guesswork of performance exploration, resulting in fewer design iterations and as much as 2X core performance gains for Intel Stratix 10 designs.

## 1.25. Single Event Upset (SEU) Error Detection and Correction

Intel Stratix 10 FPGAs and SoCs offer robust SEU error detection and correction circuitry. The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running parity checker circuit with integrated ECC that automatically corrects one or two bit errors and detects higher order multibit errors.

The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 14-nm Tri-Gate process technology used for Intel Stratix 10 devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

## 1.26. Document Revision History for the Intel Stratix 10 GX/SX Device Overview

| Document Version | Changes |
|---|---|
| 2018.08.08 | Made the following changes:<br>• Changed the specs for QDRII+ and QDRII+ Xtreme and added specs for QDRIV in the "External Memory Interface Performance" table.<br>• Updated description of the power options in the "Sample Ordering COde and Available Options for Intel Stratix 10 Devices" figure.<br>• Changed the description of the technology and power management features in the "Intel Stratix 10 FPGA and SoC Common Device Features" table.<br>• Changed the description of SmartVID in the "Power Management" section.<br>• Changed the direction arrow from the coefficient registers block in the "DSP Block: High Precision Fixed Point Mode" figure. |
| 2017.10.30 | Made the following changes:<br>• Removed the embedded eSRAM feature globally.<br>• Removed the Low Power (VID) and Military operating temperature options, and package code 53 from the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure.<br>• Changed the Maximum transceiver data rate (chip-to-chip) specification for L-Tile devices in the "Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices" table. |
| 2016.10.31 | Made the following changes:<br>• Changed the number of available transceivers to 96, globally.<br>• Changed the single-precision floating point performance to 10 TeraFLOPS, globally.<br>• Changed the maximum datarate to 28.3 Gbps, globally.<br>• Changed some of the features listed in the "Stratix 10 GX/SX Device Overview" section.<br>• Changed descriptions for the GX and SX devices in the "Stratix 10 Family Variants" section.<br>• Changed the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure. |

*continued...*

| Document Version | Changes |
|---|---|
| | • Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table.<br>• Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table:<br>— Transceiver hard IP<br>— Internal memory blocks<br>— Core clock networks<br>— Packaging<br>• Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section.<br>• Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section.<br>• Removed footnotes from the "Transceiver PCS Features" table.<br>• Changed the HMC description in the "External Memory and General Purpose I/O" section.<br>• Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section.<br>• Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table.<br>• Changed the description in the "Internal Embedded Memory" section.<br>• Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table.<br>• Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section.<br>• Updated the "Key Features of the Stratix 10 HPS" table.<br>• Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table.<br>• Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table. |
| 2015.12.04 | Initial release. |