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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

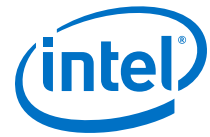
**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2800K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FBGA, FC (42.5x42.5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/1sx280ln3f43e2lg">https://www.e-xfl.com/product-detail/intel/1sx280ln3f43e2lg</a>



## 1. Intel® Stratix® 10 GX/SX Device Overview

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Intel's 14-nm Intel® Stratix® 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

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ISO  
9001:2015  
Registered



- Dedicated secure device manager (SDM) for:
  - Enhanced device configuration and security
  - AES-256, SHA-256/384 and ECDSA-256/384 encrypt/decrypt accelerators and authentication
  - Multi-factor authentication
  - Physically Unclonable Function (PUF) service and software programmable device configuration capability
- Comprehensive set of advanced power saving features delivering up to 70% lower power compared to previous generation high-performance FPGAs
- Non-destructive register state readback and writeback, to support ASIC prototyping and other applications

With these capabilities, Intel Stratix 10 FPGAs and SoCs are ideally suited for the most demanding applications in diverse markets such as:

- **Compute and Storage**—for custom servers, cloud computing and data center acceleration
- **Networking**—for Terabit, 400G and multi-100G bridging, aggregation, packet processing and traffic management
- **Optical Transport Networks**—for OTU4, 2xOTU4, 4xOTU4
- **Broadcast**—for high-end studio distribution, headend encoding/decoding, edge quadrature amplitude modulation (QAM)
- **Military**—for radar, electronic warfare, and secure communications
- **Medical**—for diagnostic scanners and diagnostic imaging
- **Test and Measurement**—for protocol and application testers
- **Wireless**—for next-generation 5G networks
- **ASIC Prototyping**—for designs that require the largest monolithic FPGA fabric with the highest I/O count

## 1.1. Intel Stratix 10 Family Variants

Intel Stratix 10 devices are available in FPGA (GX) and SoC (SX) variants.

- **Intel Stratix 10 GX** devices deliver up to 1 GHz core fabric performance and contain up to 5.5 million LEs in a monolithic fabric. They also feature up to 96 general purpose transceivers on separate transceiver tiles, and 2666 Mbps DDR4 external memory interface performance. The transceivers are capable of up to 28.3 Gbps short reach and across the backplane. These devices are optimized for FPGA applications that require the highest transceiver bandwidth and core fabric performance, with the power efficiency of Intel's industry-leading 14-nm Tri-Gate process technology.
- **Intel Stratix 10 SX** devices have a feature set that is identical to Intel Stratix 10 GX devices, with the addition of an embedded quad-core 64-bit ARM Cortex A53 hard processor system.



Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.



Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
<b>Logic density</b>	952 KLE (monolithic)	5,500 KLE (monolithic)
<b>Embedded memory (M20K)</b>	52 Mbits	229 Mbits
<b>18x19 multipliers</b>	3,926 <i>Note:</i> Multiplier is 18x18 in Stratix V devices.	11,520 <i>Note:</i> Multiplier is 18x19 in Intel Stratix 10 devices.
<b>Floating point DSP capability</b>	Up to 1 TFLOP, requires soft floating point adder and multiplier	Up to 10 TFLOPS, hard IEEE 754 compliant single precision floating point adder and multiplier
<b>Maximum transceivers</b>	66	96
<b>Maximum transceiver data rate (chip-to-chip)</b>	28.05 Gbps	28.3 Gbps L-Tile 28.3 Gbps H-Tile
<b>Maximum transceiver data rate (backplane)</b>	12.5 Gbps	12.5 Gbps L-Tile 28.3 Gbps H-Tile
<b>Hard memory controller</b>	None	DDR4 @ 1333 MHz/2666 Mbps DDR3 @ 1067 MHz/2133 Mbps
<b>Hard protocol IP</b>	PCIe Gen3 x8 (up to 4 instances)	PCIe Gen3 x16 (up to 4 instances) SR-IOV (4 physical functions / 2k virtual functions) on H-Tile devices 10GBASE-KR/40GBASE-KR4 FEC
<b>Core clocking and PLLs</b>	Global, quadrant and regional clocks supported by fractional-synthesis fPLLs	Programmable clock tree synthesis supported by fractional synthesis fPLLs and integer IO PLLs
<b>Register state readback and writeback</b>	Not available	Non-destructive register state readback and writeback for ASIC prototyping and other applications

These innovations result in the following improvements:

- **Improved Core Logic Performance:** The HyperFlex core architecture combined with Intel's 14-nm Tri-Gate technology allows Intel Stratix 10 devices to achieve 2X the core performance compared to the previous generation
- **Lower Power:** Intel Stratix 10 devices use up to 70% lower power compared to the previous generation, enabled by 14-nm Intel Tri-Gate technology, the HyperFlex core architecture, and optional power saving features built into the architecture
- **Higher Density:** Intel Stratix 10 devices offer over five times the level of integration, with up to 5,500K logic elements (LEs) in a monolithic fabric, over 229 Mbits of embedded memory blocks (M20K), and 11,520 18x19 multipliers
- **Embedded Processing:** Intel Stratix 10 SoCs feature a Quad-Core 64-bit ARM Cortex-A53 processor optimized for power efficiency and software compatible with previous generation Arria and Cyclone SoC devices
- **Improved Transceiver Performance:** With up to 96 transceiver channels implemented in heterogeneous 3D SiP transceiver tiles, Intel Stratix 10 GX and SX devices support data rates up to 28.3 Gbps chip-to-chip and 28.3 Gbps across the backplane with signal conditioning circuits capable of equalizing over 30 dB of system loss
- **Improved DSP Performance:** The variable precision DSP block in Intel Stratix 10 devices features hard fixed and floating point capability, with up to 10 TeraFLOPS IEEE754 single-precision floating point performance



- **Additional Hard IP:** Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking:** Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs:** The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

### 1.3. FPGA and SoC Features Summary

**Table 2. Intel Stratix 10 FPGA and SoC Common Device Features**

Feature	Description
Technology	<ul style="list-style-type: none"><li>• 14-nm Intel Tri-Gate (FinFET) process technology</li><li>• SmartVID controlled core voltage, standard power devices</li><li>• 0.85-V fixed core voltage, low static power devices available</li></ul>
Low power serial transceivers	<ul style="list-style-type: none"><li>• Up to 96 total transceivers available</li><li>• Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices</li><li>• Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices</li><li>• Extended range down to 125 Mbps with oversampling</li><li>• ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>• XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support</li><li>• Adaptive linear and decision feedback equalization</li><li>• Transmit pre-emphasis and de-emphasis</li><li>• Dynamic partial reconfiguration of individual transceiver channels</li><li>• On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)</li></ul>
General purpose I/Os	<ul style="list-style-type: none"><li>• Up to 1640 total GPIO available</li><li>• 1.6 Gbps LVDS—every pair can be configured as an input or output</li><li>• 1333 MHz/2666 Mbps DDR4 external memory interface</li><li>• 1067 MHz/2133 Mbps DDR3 external memory interface</li><li>• 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing</li><li>• On-chip termination (OCT)</li></ul>
Embedded hard IP	<ul style="list-style-type: none"><li>• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port</li><li>• DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller)</li><li>• Multiple hard IP instantiations in each device</li><li>• Single Root I/O Virtualization (SR-IOV)</li></ul>
Transceiver hard IP	<ul style="list-style-type: none"><li>• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>• 10G Ethernet PCS</li><li>• PCI Express PIPE interface</li><li>• Interlaken PCS</li><li>• Gigabit Ethernet PCS</li><li>• Deterministic latency support for Common Public Radio Interface (CPRI) PCS</li><li>• Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS</li><li>• 8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>• Custom mode support for proprietary protocols</li></ul>
continued...	



Feature	Description
Power management	<ul style="list-style-type: none"> <li>SmartVID controlled core voltage, standard power devices</li> <li>0.85-V fixed core voltage, low static power devices available</li> <li>Intel Quartus® Prime Pro Edition integrated power analysis</li> </ul>
High performance monolithic core fabric	<ul style="list-style-type: none"> <li>HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks</li> <li>Monolithic fabric minimizes compile times and increases logic utilization</li> <li>Enhanced adaptive logic module (ALM)</li> <li>Improved multi-track routing architecture reduces congestion and improves compile times</li> <li>Hierarchical core clocking architecture with programmable clock tree synthesis</li> <li>Fine-grained partial reconfiguration</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>M20K—20-Kbit with hard ECC support</li> <li>MLAB—640-bit distributed LUTRAM</li> </ul>
Variable precision DSP blocks	<ul style="list-style-type: none"> <li>IEEE 754-compliant hard single-precision floating point capability</li> <li>Supports signal processing with precision ranging from 18x19 up to 54x54</li> <li>Native 27x27 and 18x19 multiply modes</li> <li>64-bit accumulator and cascade for systolic FIRs</li> <li>Internal coefficient memory banks</li> <li>Pre-adder/subtractor improves efficiency</li> <li>Additional pipeline register increases performance and reduces power</li> </ul>
Phase locked loops (PLL)	<ul style="list-style-type: none"> <li>Fractional synthesis PLLs (fPLL) support both fractional and integer modes</li> <li>Fractional mode with third-order delta-sigma modulation</li> <li>Precision frequency synthesis</li> <li>Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering</li> </ul>
Core clock networks	<ul style="list-style-type: none"> <li>1 GHz fabric clocking</li> <li>667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface</li> <li>800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface</li> <li>Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks</li> <li>Clocks only synthesized where needed, to minimize dynamic power</li> </ul>
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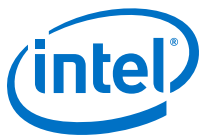


Feature	Description
Configuration	<ul style="list-style-type: none"><li>• Dedicated Secure Device Manager</li><li>• Software programmable device configuration</li><li>• Serial and parallel flash interface</li><li>• Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3</li><li>• Fine-grained partial reconfiguration of core fabric</li><li>• Dynamic reconfiguration of transceivers and PLLs</li><li>• Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication</li><li>• Physically Unclonable Function (PUF) service</li></ul>
Packaging	<ul style="list-style-type: none"><li>• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology</li><li>• Multiple devices with identical package footprints allows seamless migration across different device densities</li><li>• 1.0 mm ball-pitch FBGA packaging</li><li>• Lead and lead-free package options</li></ul>
Software and tools	<ul style="list-style-type: none"><li>• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow</li><li>• Fast Forward compiler to allow HyperFlex architecture performance exploration</li><li>• Transceiver toolkit</li><li>• Platform designer integration tool</li><li>• DSP Builder advanced blockset</li><li>• OpenCL™ support</li><li>• SoC Embedded Design Suite (EDS)</li></ul>

Table 3. Intel Stratix 10 SoC Specific Device Features

SoC Subsystem	Feature	Description
<b>Hard Processor System</b>	Multi-processor unit (MPU) core	<ul style="list-style-type: none"><li>• Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology</li><li>• Scalar floating-point unit supporting single and double precision</li><li>• ARM NEON media processing engine for each processor</li></ul>
	System Controllers	<ul style="list-style-type: none"><li>• System Memory Management Unit (SMMU)</li><li>• Cache Coherency Unit (CCU)</li></ul>
	Layer 1 Cache	<ul style="list-style-type: none"><li>• 32 KB L1 instruction cache with parity</li><li>• 32 KB L1 data cache with ECC</li></ul>
	Layer 2 Cache	<ul style="list-style-type: none"><li>• 1 MB Shared L2 Cache with ECC</li></ul>
	On-Chip Memory	<ul style="list-style-type: none"><li>• 256 KB On-Chip RAM</li></ul>
	Direct memory access (DMA) controller	<ul style="list-style-type: none"><li>• 8-Channel DMA</li></ul>
	Ethernet media access controller (EMAC)	<ul style="list-style-type: none"><li>• Three 10/100/1000 EMAC with integrated DMA</li></ul>
	USB On-The-Go controller (OTG)	<ul style="list-style-type: none"><li>• 2 USB OTG with integrated DMA</li></ul>
	UART controller	<ul style="list-style-type: none"><li>• 2 UART 16550 compatible</li></ul>
	Serial Peripheral Interface (SPI) controller	<ul style="list-style-type: none"><li>• 4 SPI</li></ul>
	I <sup>2</sup> C controller	<ul style="list-style-type: none"><li>• 5 I<sup>2</sup>C controllers</li></ul>
	SD/SDIO/MMC controller	<ul style="list-style-type: none"><li>• 1 eMMC version 4.5 with DMA and CE-ATA support</li><li>• SD, including eSD, version 3.0</li><li>• SDIO, including eSDIO, version 3.0</li><li>• CE-ATA - version 1.1</li></ul>
continued...		





**Table 4. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—FPGA Core (part 1)**

Intel Stratix 10 GX/SX Device Name	Logic Elements (KLE)	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multipliers <sup>(1)</sup>
GX 400/ SX 400	378	1,537	30	3,204	2	1,296
GX 650/ SX 650	612	2,489	49	5,184	3	2,304
GX 850/ SX 850	841	3,477	68	7,124	4	4,032
GX 1100/ SX 1100	1,092	4,401	86	9,540	6	5,040
GX 1650/ SX 1650	1,624	5,851	114	13,764	8	6,290
GX 2100/ SX 2100	2,005	6,501	127	17,316	11	7,488
GX 2500/ SX 2500	2,422	9,963	195	20,529	13	10,022
GX 2800/ SX 2800	2,753	11,721	229	23,796	15	11,520
GX 4500/ SX 4500	4,463	7,033	137	37,821	23	3,960
GX 5500/ SX 5500	5,510	7,033	137	47,700	29	3,960

**Table 5. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—Interconnects, PLLs and Hard IP (part 2)**

Intel Stratix 10 GX/SX Device Name	Interconnects		PLLs		Hard IP
	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 400/ SX 400	392	24	8	8	1
GX 650/ SX 650	400	48	16	8	2
GX 850/ SX 850	736	48	16	15	2
GX 1100/ SX 1100	736	48	16	15	2
GX 1650/ SX 1650	704	96	32	14	4
GX 2100/ SX 2100	704	96	32	14	4
GX 2500/ SX 2500	1160	96	32	24	4
continued...					



Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm <sup>2</sup> )	F1760 NF43 (42.5x42.5 mm <sup>2</sup> )	F1760 NF43 (42.5x42.5 mm <sup>2</sup> )
SX 2800			
GX 4500/ SX 4500			
GX 5500/ SX 5500			

**Table 7. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 2**

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup> <sup>(5)</sup> <sup>(6)</sup> <sup>(7)</sup>

Intel Stratix 10 GX/SX Device Name	F2112 NF48 (47.5x47.5 mm <sup>2</sup> )	F2397 UF50 (50x50 mm <sup>2</sup> )	F2912 HF55 (55x55 mm <sup>2</sup> )
GX 400/ SX 400			
GX 650/ SX 650			
GX 850/ SX 850	736, 16, 360, 48		
GX 1100/ SX 1100	736, 16, 360, 48		
GX 1650/ SX 1650		704, 32, 336, 96	
GX 2100/ SX 2100		704, 32, 336, 96	
GX 2500/ SX 2500		704, 32, 336, 96	1160, 8, 576, 24
GX 2800/ SX 2800		704, 32, 336, 96	1160, 8, 576, 24
GX 4500/ SX 4500			1640, 8, 816, 24
GX 5500/ SX 5500			1640, 8, 816, 24



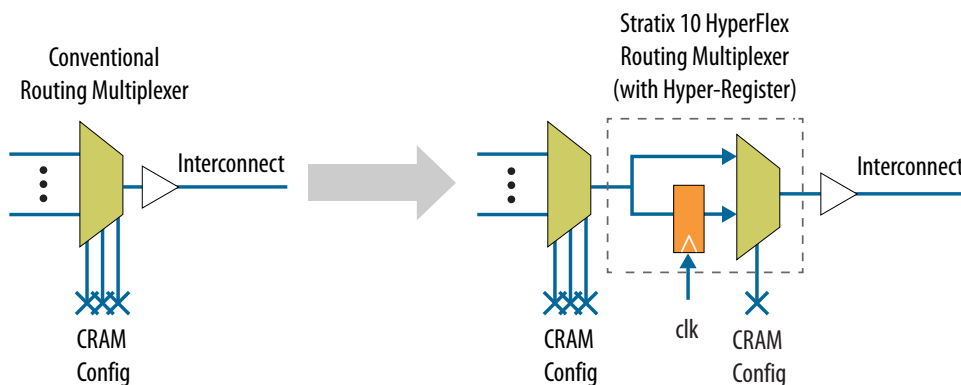
## 1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 3. Bypassable Hyper-Register



The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.



Feature	Capability
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation—Eye Viewer and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (Eye Viewer). Also inject jitter from transmitter to test link margin in system.
Dynamic Reconfiguration	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility.
Multiple PCS-PMA and PCS-Core to FPGA fabric interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

## 1.8.2. PCS Features

Intel Stratix 10 PMA channels interface with core logic through configurable and bypassable PCS interface layers.

The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. This feature provides the flexibility to implement a wide range of applications with 8, 10, 16, 20, 32, 40, or 64-bit interface width between each transceiver and the core logic.

The PCS also contains hard IP to support a variety of standard and proprietary protocols across a wide range of data rates and encoding schemes. The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports 64B/66B and 64B/67B encoded applications up to 17.4 Gbps. The enhanced PCS mode also includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit. For highly customized implementations, a PCS Direct mode provides an interface up to 64 bits wide to allow for custom encoding and support for data rates up to 28.3 Gbps.

For more information about the PCS-Core interface or the double rate transfer mode, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*, and the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.

**Table 9. Transceiver PCS Features**

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	1 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x2, x4, x8, x16	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core
PCI Express Gen3 x1, x2, x4, x8, x16	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit-slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
continued...			



Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

**Table 10. External Memory Interface Performance**

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

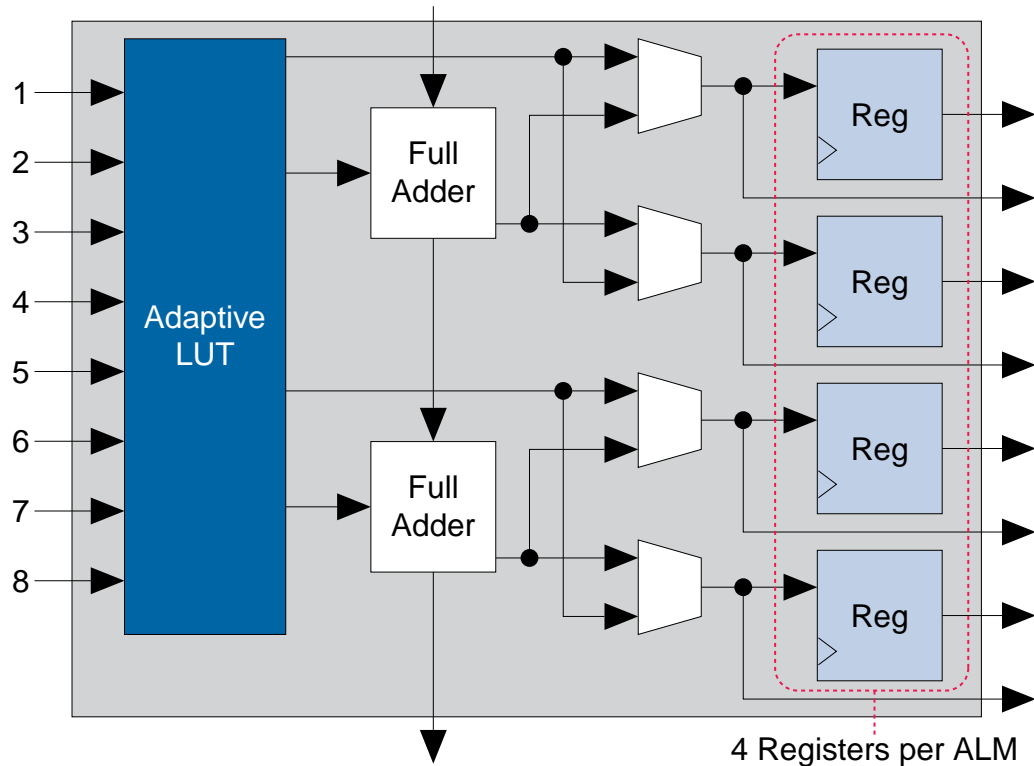
Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

### 1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

**Figure 9. Intel Stratix 10 FPGA and SoC ALM Block Diagram**



Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

## 1.14. Core Clocking

Core clocking in Intel Stratix 10 devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.



The core clock network in Intel Stratix 10 devices supports the new HyperFlex core architecture at clock rates up to 1 GHz. It also supports the hard memory controllers up to 2666 Mbps with a quarter rate transfer to the core. The core clock network is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

## 1.15. Fractional Synthesis PLLs and I/O PLLs

Intel Stratix 10 devices have up to 32 fractional synthesis PLLs (fPLL) available for use with transceivers or in the core fabric.

The fPLLs are located in the 3D SiP transceiver H-tiles, eight per tile, adjacent to the transceiver channels. The fPLLs can be used to reduce both the number of oscillators required on the board and the number of clock pins required, by synthesizing multiple clock frequencies from a single reference clock source. In addition to synthesizing reference clock frequencies for the transceiver transmit PLLs, the fPLLs can also be used directly for transmit clocking. Each fPLL can be independently configured for conventional integer mode, or enhanced fractional synthesis mode with third-order delta-sigma modulation.

In addition to the fPLLs, Intel Stratix 10 devices contain up to 34 integer I/O PLLs (IOPLLs) available for general purpose use in the core fabric and for simplifying the design of external memory interfaces and high-speed LVDS interfaces. The IOPLLs are located in each bank of 48 general purpose I/O, 1 per I/O bank, adjacent to the hard memory controllers and LVDS SerDes in each I/O bank. This makes it easier to close timing because the IOPLLs are tightly coupled with the I/Os that need to use them. The IOPLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay clock buffering.

## 1.16. Internal Embedded Memory

Intel Stratix 10 devices contain two types of embedded memory blocks: M20K (20-Kbit) and MLAB (640-bit).

The M20K and MLAB blocks are familiar block sizes carried over from previous Intel device families. The MLAB blocks are ideal for wide and shallow memories, while the M20K blocks are intended to support larger memory configurations and include hard ECC. Both M20K and MLAB embedded memory blocks can be configured as a single-port or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are highly flexible and support a number of memory configurations as shown in [Table 11](#) on page 25.

**Table 11. Internal Embedded Memory Block Configurations**

MLAB (640 bits)	M20K (20 Kbits)
64 x 10 (supported through emulation) 32 x 20	2K x 10 (or x8) 1K x 20 (or x16) 512 x 40 (or x32)

## 1.17. Variable Precision DSP Block

The Intel Stratix 10 DSP blocks are based upon the Variable Precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE-754 compliant floating point capability.

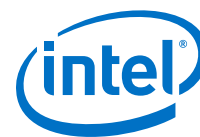
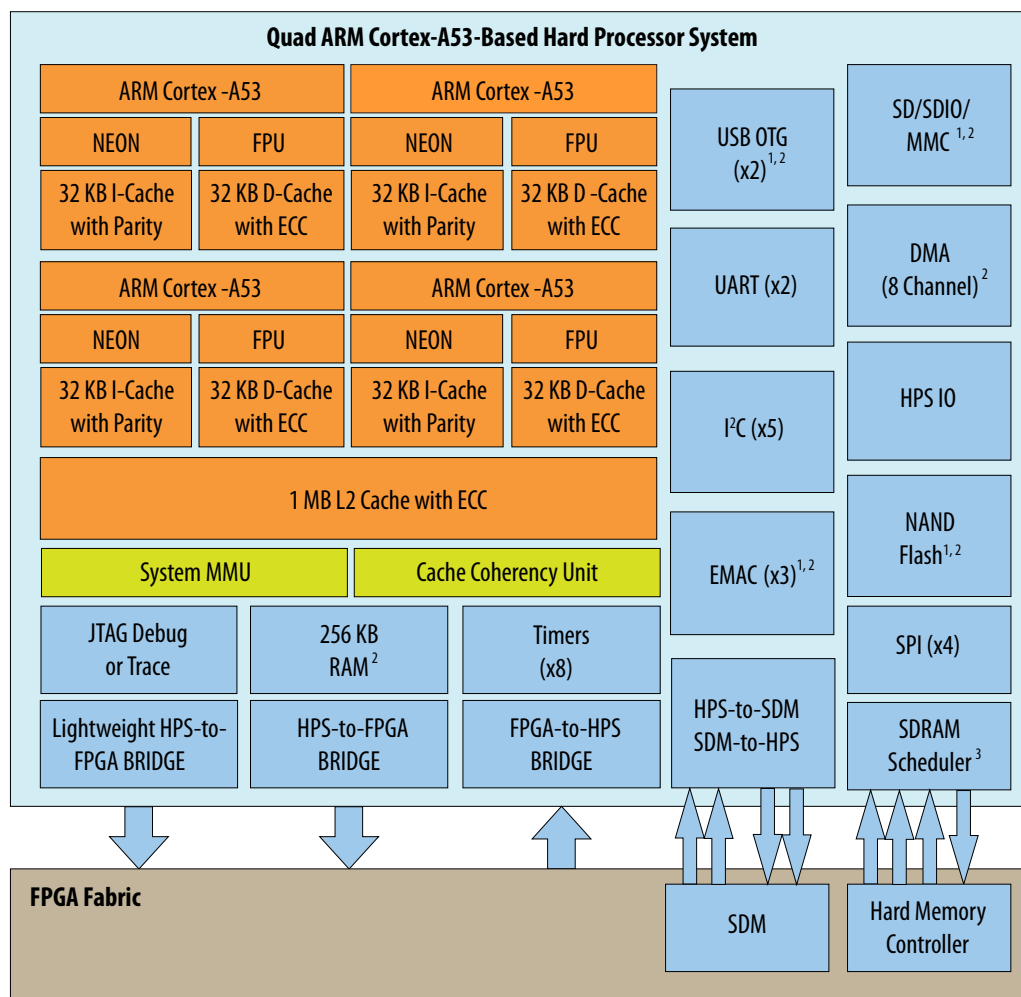


Figure 13. HPS Block Diagram



Notes:

1. Integrated direct memory access (DMA)
2. Integrated error correction code (ECC)
3. Multiport front-end interface to hard memory controller

### 1.18.1. Key Features of the Intel Stratix 10 HPS

Table 14. Key Features of the Intel Stratix 10 GX/SX HPS

Feature	Description
Quad-core ARM Cortex-A53 MPCore processor unit	<ul style="list-style-type: none"> <li>• 2.3 MIPS/MHz instruction efficiency</li> <li>• CPU frequency up to 1.5 GHz</li> <li>• At 1.5 GHz total performance of 13,800 MIPS</li> <li>• ARMv8-A architecture</li> <li>• Runs 64-bit and 32-bit ARM instructions</li> <li>• 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint</li> <li>• Jazelle® RCT execution architecture with 8-bit Java bytecodes</li> </ul>

continued...



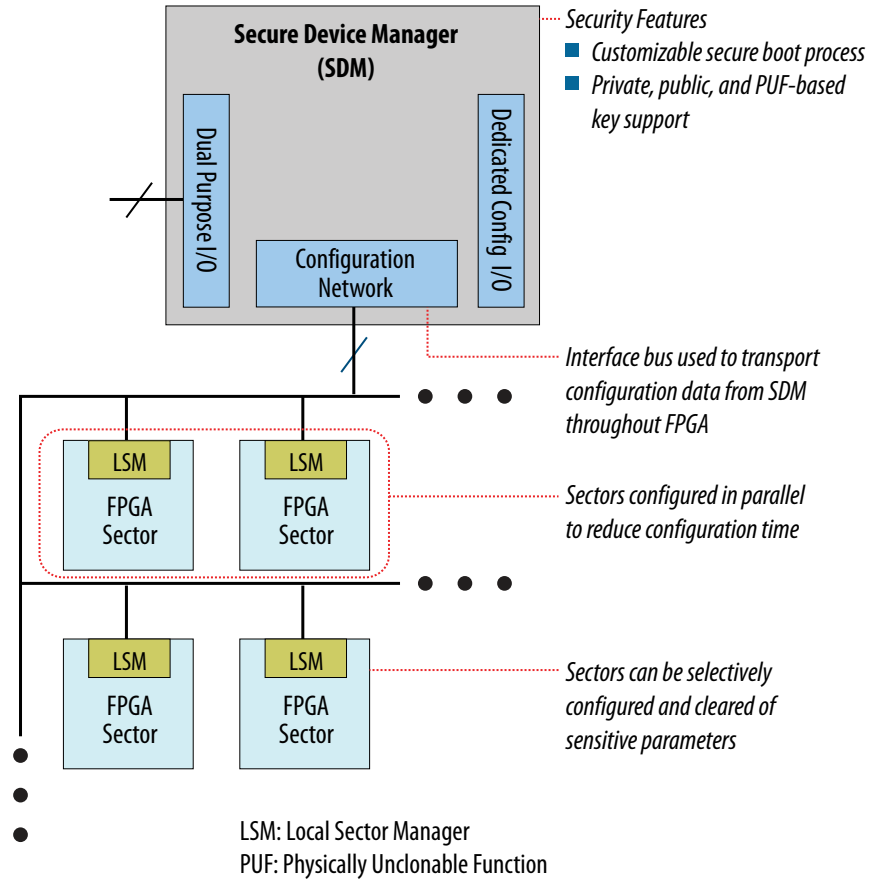


Feature	Description
	<ul style="list-style-type: none"> <li>Superscalar, variable length, out-of-order pipeline with dynamic branch prediction</li> <li>Improved ARM NEON™ media processing engine</li> <li>Single- and double-precision floating-point unit</li> <li>CoreSight™ debug and trace technology</li> </ul>
System Memory Management Unit	<ul style="list-style-type: none"> <li>Enables a unified memory model and extends hardware virtualization into peripherals implemented in the FPGA fabric</li> </ul>
Cache Coherency unit	<ul style="list-style-type: none"> <li>Changes in shared data stored in cache are propagated throughout the system providing bi-directional coherency for co-processing elements.</li> </ul>
Cache	<ul style="list-style-type: none"> <li>L1 Cache <ul style="list-style-type: none"> <li>32 KB of instruction cache w/ parity check</li> <li>32 KB of L1 data cache w /ECC</li> <li>Parity checking</li> </ul> </li> <li>L2 Cache <ul style="list-style-type: none"> <li>1MB shared</li> <li>8-way set associative</li> <li>SEU Protection with parity on TAG ram and ECC on data RAM</li> <li>Cache lockdown support</li> </ul> </li> </ul>
On-Chip Memory	<ul style="list-style-type: none"> <li>256 KB of scratch on-chip RAM</li> </ul>
External SDRAM and Flash Memory Interfaces for HPS	<ul style="list-style-type: none"> <li>Hard memory controller with support for DDR4, DDR3, LPDDR3 <ul style="list-style-type: none"> <li>40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC)</li> <li>Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies</li> <li>Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters</li> <li>Software Configurable Priority Scheduling on individual SDRAM bursts</li> <li>Fully programmable timing parameter support for all JEDEC-specified timing parameters</li> <li>Multiport front-end (MPFE) scheduler interface to the hard memory controller, which supports the AXI® Quality of Service (QoS) for interface to the FPGA fabric</li> </ul> </li> <li>NAND flash controller <ul style="list-style-type: none"> <li>ONFI 1.0</li> <li>Integrated descriptor based with DMA</li> <li>Programmable hardware ECC support</li> <li>Support for 8- and 16-bit Flash devices</li> </ul> </li> <li>Secure Digital SD/SDIO/MMC controller <ul style="list-style-type: none"> <li>eMMC 4.5</li> <li>Integrated descriptor based DMA</li> <li>CE-ATA digital commands supported</li> <li>50 MHz operating frequency</li> </ul> </li> <li>Direct memory access (DMA) controller <ul style="list-style-type: none"> <li>8-channel</li> <li>Supports up to 32 peripheral handshake interface</li> </ul> </li> </ul>

*continued...*



Figure 14. SDM Block Diagram



During configuration, Intel Stratix 10 devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.



The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

## 1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

## 1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be



powered up and active within the 100 ms time allowed by the PCI Express specification. Intel Stratix 10 devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

### 1.23. Partial and Dynamic Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.

In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Intel Quartus Prime design software

Dynamic reconfiguration in Intel Stratix 10 devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multiprotocol or multi-rate support. Both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

### 1.24. Fast Forward Compile

The innovative Fast Forward Compile feature in the Intel Quartus Prime software identifies performance bottlenecks in your design and provides detailed, step-by-step performance improvement recommendations that you can then implement. The Compiler reports estimates of the maximum operating frequency that can be achieved by applying the recommendations. As part of the new Hyper-Aware design flow, Fast Forward Compile maximizes the performance of your Intel Stratix 10 design and achieves rapid timing closure.

Previously, this type of optimization required multiple time-consuming design iterations, including full design re-compilation to determine the effectiveness of the changes. Fast Forward Compile enables you to make better decisions about where to focus your optimization efforts, and how to increase your design performance and throughput. This technique removes much of the guesswork of performance exploration, resulting in fewer design iterations and as much as 2X core performance gains for Intel Stratix 10 designs.

### 1.25. Single Event Upset (SEU) Error Detection and Correction

Intel Stratix 10 FPGAs and SoCs offer robust SEU error detection and correction circuitry. The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running parity checker circuit with integrated ECC that automatically corrects one or two bit errors and detects higher order multibit errors.



Document Version	Changes
	<ul style="list-style-type: none"> <li>• Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table.</li> <li>• Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table: <ul style="list-style-type: none"> <li>— Transceiver hard IP</li> <li>— Internal memory blocks</li> <li>— Core clock networks</li> <li>— Packaging</li> </ul> </li> <li>• Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section.</li> <li>• Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section.</li> <li>• Removed footnotes from the "Transceiver PCS Features" table.</li> <li>• Changed the HMC description in the "External Memory and General Purpose I/O" section.</li> <li>• Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section.</li> <li>• Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description in the "Internal Embedded Memory" section.</li> <li>• Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table.</li> <li>• Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section.</li> <li>• Updated the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table.</li> </ul>
2015.12.04	Initial release.