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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2800K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FBGA, FC (42.5x42.5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/1sx280ln3f43i2vg">https://www.e-xfl.com/product-detail/intel/1sx280ln3f43i2vg</a>



## 1. Intel® Stratix® 10 GX/SX Device Overview

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Intel's 14-nm Intel® Stratix® 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

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ISO  
9001:2015  
Registered



- Dedicated secure device manager (SDM) for:
  - Enhanced device configuration and security
  - AES-256, SHA-256/384 and ECDSA-256/384 encrypt/decrypt accelerators and authentication
  - Multi-factor authentication
  - Physically Unclonable Function (PUF) service and software programmable device configuration capability
- Comprehensive set of advanced power saving features delivering up to 70% lower power compared to previous generation high-performance FPGAs
- Non-destructive register state readback and writeback, to support ASIC prototyping and other applications

With these capabilities, Intel Stratix 10 FPGAs and SoCs are ideally suited for the most demanding applications in diverse markets such as:

- **Compute and Storage**—for custom servers, cloud computing and data center acceleration
- **Networking**—for Terabit, 400G and multi-100G bridging, aggregation, packet processing and traffic management
- **Optical Transport Networks**—for OTU4, 2xOTU4, 4xOTU4
- **Broadcast**—for high-end studio distribution, headend encoding/decoding, edge quadrature amplitude modulation (QAM)
- **Military**—for radar, electronic warfare, and secure communications
- **Medical**—for diagnostic scanners and diagnostic imaging
- **Test and Measurement**—for protocol and application testers
- **Wireless**—for next-generation 5G networks
- **ASIC Prototyping**—for designs that require the largest monolithic FPGA fabric with the highest I/O count

## 1.1. Intel Stratix 10 Family Variants

Intel Stratix 10 devices are available in FPGA (GX) and SoC (SX) variants.

- **Intel Stratix 10 GX** devices deliver up to 1 GHz core fabric performance and contain up to 5.5 million LEs in a monolithic fabric. They also feature up to 96 general purpose transceivers on separate transceiver tiles, and 2666 Mbps DDR4 external memory interface performance. The transceivers are capable of up to 28.3 Gbps short reach and across the backplane. These devices are optimized for FPGA applications that require the highest transceiver bandwidth and core fabric performance, with the power efficiency of Intel's industry-leading 14-nm Tri-Gate process technology.
- **Intel Stratix 10 SX** devices have a feature set that is identical to Intel Stratix 10 GX devices, with the addition of an embedded quad-core 64-bit ARM Cortex A53 hard processor system.



Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

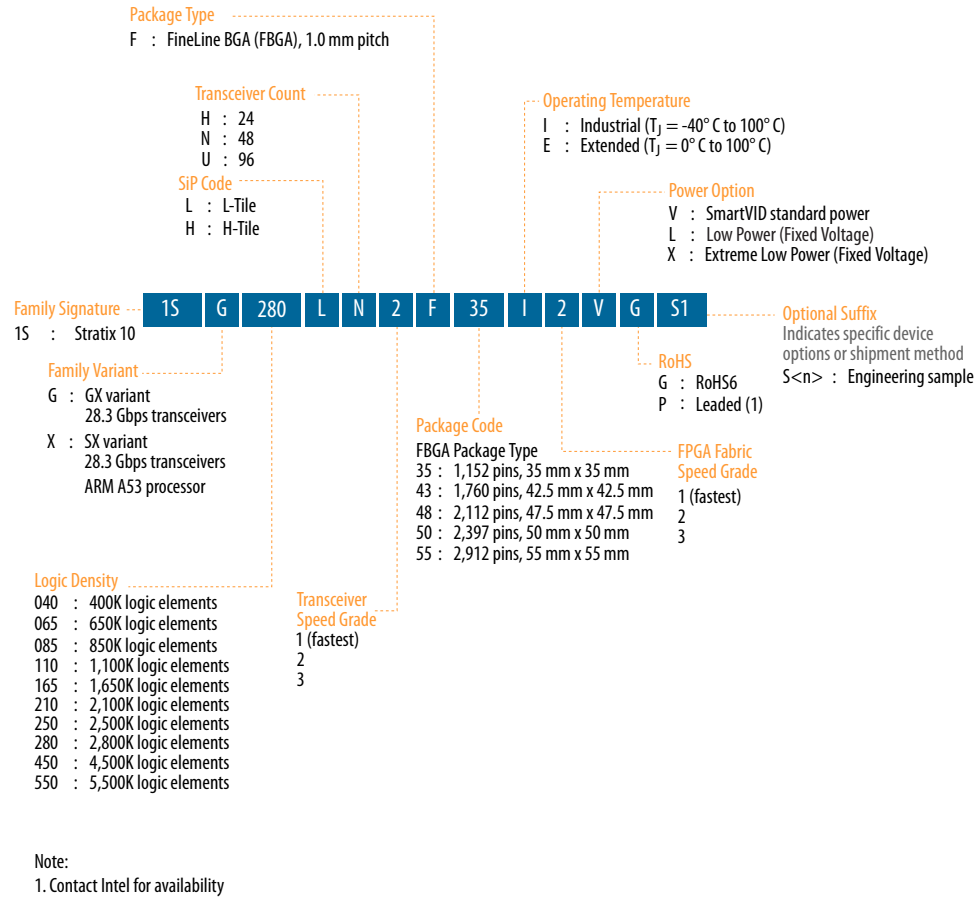
To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.



### 1.1.1. Available Options

**Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices**



## 1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

**Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices**

Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
<b>Process technology</b>	28-nm TSMC (planar transistor)	14 nm Intel Tri-Gate (FinFET)
<b>Hard processor core</b>	None	Quad-core 64-bit ARM Cortex-A53 (SoC only)
<b>Core architecture</b>	Conventional core architecture with conventional interconnect	HyperFlex core architecture with Hyper-Registers in the interconnect
<b>Core performance</b>	500 MHz	1 GHz
<b>Power dissipation</b>	1x	As low as 0.3x
<i>continued...</i>		



- **Additional Hard IP:** Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking:** Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs:** The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

### 1.3. FPGA and SoC Features Summary

**Table 2. Intel Stratix 10 FPGA and SoC Common Device Features**

Feature	Description
Technology	<ul style="list-style-type: none"><li>• 14-nm Intel Tri-Gate (FinFET) process technology</li><li>• SmartVID controlled core voltage, standard power devices</li><li>• 0.85-V fixed core voltage, low static power devices available</li></ul>
Low power serial transceivers	<ul style="list-style-type: none"><li>• Up to 96 total transceivers available</li><li>• Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices</li><li>• Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices</li><li>• Extended range down to 125 Mbps with oversampling</li><li>• ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>• XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support</li><li>• Adaptive linear and decision feedback equalization</li><li>• Transmit pre-emphasis and de-emphasis</li><li>• Dynamic partial reconfiguration of individual transceiver channels</li><li>• On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)</li></ul>
General purpose I/Os	<ul style="list-style-type: none"><li>• Up to 1640 total GPIO available</li><li>• 1.6 Gbps LVDS—every pair can be configured as an input or output</li><li>• 1333 MHz/2666 Mbps DDR4 external memory interface</li><li>• 1067 MHz/2133 Mbps DDR3 external memory interface</li><li>• 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing</li><li>• On-chip termination (OCT)</li></ul>
Embedded hard IP	<ul style="list-style-type: none"><li>• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port</li><li>• DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller)</li><li>• Multiple hard IP instantiations in each device</li><li>• Single Root I/O Virtualization (SR-IOV)</li></ul>
Transceiver hard IP	<ul style="list-style-type: none"><li>• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>• 10G Ethernet PCS</li><li>• PCI Express PIPE interface</li><li>• Interlaken PCS</li><li>• Gigabit Ethernet PCS</li><li>• Deterministic latency support for Common Public Radio Interface (CPRI) PCS</li><li>• Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS</li><li>• 8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>• Custom mode support for proprietary protocols</li></ul>
continued...	



Feature	Description
Power management	<ul style="list-style-type: none"> <li>SmartVID controlled core voltage, standard power devices</li> <li>0.85-V fixed core voltage, low static power devices available</li> <li>Intel Quartus® Prime Pro Edition integrated power analysis</li> </ul>
High performance monolithic core fabric	<ul style="list-style-type: none"> <li>HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks</li> <li>Monolithic fabric minimizes compile times and increases logic utilization</li> <li>Enhanced adaptive logic module (ALM)</li> <li>Improved multi-track routing architecture reduces congestion and improves compile times</li> <li>Hierarchical core clocking architecture with programmable clock tree synthesis</li> <li>Fine-grained partial reconfiguration</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>M20K—20-Kbit with hard ECC support</li> <li>MLAB—640-bit distributed LUTRAM</li> </ul>
Variable precision DSP blocks	<ul style="list-style-type: none"> <li>IEEE 754-compliant hard single-precision floating point capability</li> <li>Supports signal processing with precision ranging from 18x19 up to 54x54</li> <li>Native 27x27 and 18x19 multiply modes</li> <li>64-bit accumulator and cascade for systolic FIRs</li> <li>Internal coefficient memory banks</li> <li>Pre-adder/subtractor improves efficiency</li> <li>Additional pipeline register increases performance and reduces power</li> </ul>
Phase locked loops (PLL)	<ul style="list-style-type: none"> <li>Fractional synthesis PLLs (fPLL) support both fractional and integer modes</li> <li>Fractional mode with third-order delta-sigma modulation</li> <li>Precision frequency synthesis</li> <li>Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering</li> </ul>
Core clock networks	<ul style="list-style-type: none"> <li>1 GHz fabric clocking</li> <li>667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface</li> <li>800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface</li> <li>Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks</li> <li>Clocks only synthesized where needed, to minimize dynamic power</li> </ul>
<b>continued...</b>	



Feature	Description
Configuration	<ul style="list-style-type: none"> <li>Dedicated Secure Device Manager</li> <li>Software programmable device configuration</li> <li>Serial and parallel flash interface</li> <li>Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3</li> <li>Fine-grained partial reconfiguration of core fabric</li> <li>Dynamic reconfiguration of transceivers and PLLs</li> <li>Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication</li> <li>Physically Unclonable Function (PUF) service</li> </ul>
Packaging	<ul style="list-style-type: none"> <li>Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology</li> <li>Multiple devices with identical package footprints allows seamless migration across different device densities</li> <li>1.0 mm ball-pitch FBGA packaging</li> <li>Lead and lead-free package options</li> </ul>
Software and tools	<ul style="list-style-type: none"> <li>Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow</li> <li>Fast Forward compiler to allow HyperFlex architecture performance exploration</li> <li>Transceiver toolkit</li> <li>Platform designer integration tool</li> <li>DSP Builder advanced blockset</li> <li>OpenCL™ support</li> <li>SoC Embedded Design Suite (EDS)</li> </ul>

**Table 3. Intel Stratix 10 SoC Specific Device Features**

SoC Subsystem	Feature	Description
<b>Hard Processor System</b>	Multi-processor unit (MPU) core	<ul style="list-style-type: none"> <li>Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology</li> <li>Scalar floating-point unit supporting single and double precision</li> <li>ARM NEON media processing engine for each processor</li> </ul>
	System Controllers	<ul style="list-style-type: none"> <li>System Memory Management Unit (SMMU)</li> <li>Cache Coherency Unit (CCU)</li> </ul>
	Layer 1 Cache	<ul style="list-style-type: none"> <li>32 KB L1 instruction cache with parity</li> <li>32 KB L1 data cache with ECC</li> </ul>
	Layer 2 Cache	<ul style="list-style-type: none"> <li>1 MB Shared L2 Cache with ECC</li> </ul>
	On-Chip Memory	<ul style="list-style-type: none"> <li>256 KB On-Chip RAM</li> </ul>
	Direct memory access (DMA) controller	<ul style="list-style-type: none"> <li>8-Channel DMA</li> </ul>
	Ethernet media access controller (EMAC)	<ul style="list-style-type: none"> <li>Three 10/100/1000 EMAC with integrated DMA</li> </ul>
	USB On-The-Go controller (OTG)	<ul style="list-style-type: none"> <li>2 USB OTG with integrated DMA</li> </ul>
	UART controller	<ul style="list-style-type: none"> <li>2 UART 16550 compatible</li> </ul>
	Serial Peripheral Interface (SPI) controller	<ul style="list-style-type: none"> <li>4 SPI</li> </ul>
	I <sup>2</sup> C controller	<ul style="list-style-type: none"> <li>5 I<sup>2</sup>C controllers</li> </ul>
	SD/SDIO/MMC controller	<ul style="list-style-type: none"> <li>1 eMMC version 4.5 with DMA and CE-ATA support</li> <li>SD, including eSD, version 3.0</li> <li>SDIO, including eSDIO, version 3.0</li> <li>CE-ATA - version 1.1</li> </ul>
<i>continued...</i>		

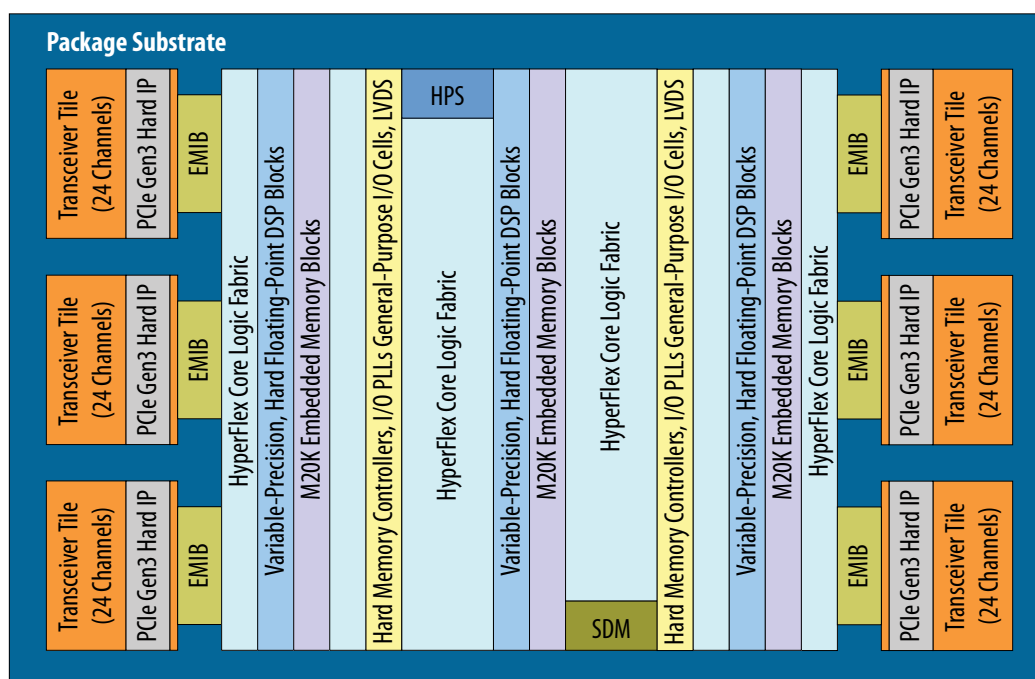




SoC Subsystem	Feature	Description
	NAND flash controller	<ul style="list-style-type: none"> <li>1 ONFI 1.0, 8- and 16-bit support</li> </ul>
	General-purpose I/O (GPIO)	<ul style="list-style-type: none"> <li>Maximum of 48 software programmable GPIO</li> </ul>
	Timers	<ul style="list-style-type: none"> <li>4 general-purpose timers</li> <li>4 watchdog timers</li> </ul>
<b>Secure Device Manager</b>	Security	<ul style="list-style-type: none"> <li>Secure boot</li> <li>Advanced Encryption Standard (AES) and authentication (SHA/ECDSA)</li> </ul>
<b>External Memory Interface</b>	External Memory Interface	<ul style="list-style-type: none"> <li>Hard Memory Controller with DDR4 and DDR3, and LPDDR3</li> </ul>

## 1.4. Intel Stratix 10 Block Diagram

Figure 2. Intel Stratix 10 FPGA and SoC Architecture Block Diagram



HPS: Quad ARM Cortex-A53 Hard Processor System

SDM: Secure Device Manager

EMIB: Embedded Multi-Die Interconnect Bridge

## 1.5. Intel Stratix 10 FPGA and SoC Family Plan

(1) The number of 27x27 multipliers is one-half the number of 18x19 multipliers.



Intel Stratix 10 GX/SX Device Name	Interconnects		PLLs		Hard IP
	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 2800/ SX 2800	1160	96	32	24	4
GX 4500/ SX 4500	1640	24	8	34	1
GX 5500/ SX 5500	1640	24	8	34	1

**Table 6. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 1**Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup> <sup>(5)</sup> <sup>(6)</sup> <sup>(7)</sup>

Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm <sup>2</sup> )	F1760 NF43 (42.5x42.5 mm <sup>2</sup> )	F1760 NF43 (42.5x42.5 mm <sup>2</sup> )
GX 400/ SX 400	392, 8, 192, 24		
GX 650/ SX 650	392, 8, 192, 24	400, 16, 192, 48	
GX 850/ SX 850			688, 16, 336, 48
GX 1100/ SX 1100			688, 16, 336, 48
GX 1650/ SX 1650			688, 16, 336, 48
GX 2100/ SX 2100			688, 16, 336, 48
GX 2500/ SX 2500			688, 16, 336, 48
GX 2800/ SX 2800			688, 16, 336, 48
<b>continued...</b>			

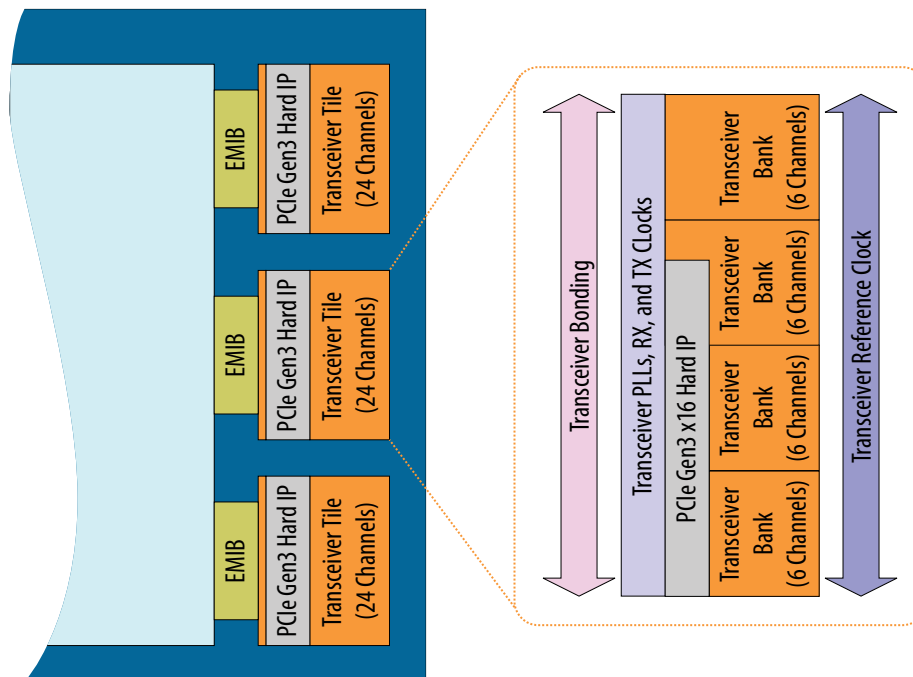
<sup>(2)</sup> All packages are ball grid arrays with 1.0 mm pitch.<sup>(3)</sup> High-Voltage I/O pins are used for 3 V and 2.5 V interfacing.<sup>(4)</sup> Each LVDS pair can be configured as either a differential input or a differential output.<sup>(5)</sup> High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.<sup>(6)</sup> Each package column offers pin migration (common circuit board footprint) for all devices in the column.<sup>(7)</sup> Intel Stratix 10 GX devices are pin migratable with Intel Stratix 10 SX devices in the same package.



Each transceiver tile contains:

- 24 full-duplex transceiver channels (PMA and PCS)
- Reference clock distribution network
- Transmit PLLs
- High-speed clocking and bonding networks
- One instance of PCI Express hard IP

**Figure 6. Heterogeneous 3D SiP Transceiver Tile Architecture**



## 1.8. Intel Stratix 10 Transceivers

Intel Stratix 10 devices offer up to 96 total full-duplex transceiver channels. These channels provide continuous data rates from 1 Gbps to 28.3 Gbps for chip-to-chip, chip-to-module, and backplane applications. In each device, two thirds of the transceivers can be configured up to the maximum data rate of 28.3 Gbps to drive 100G interfaces and C form-factor pluggable CFP2/CFP4 optical modules. For longer-reach backplane driving applications, advanced adaptive equalization circuits are used to equalize over 30 dB of system loss.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.



Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

### 1.8.1. PMA Features

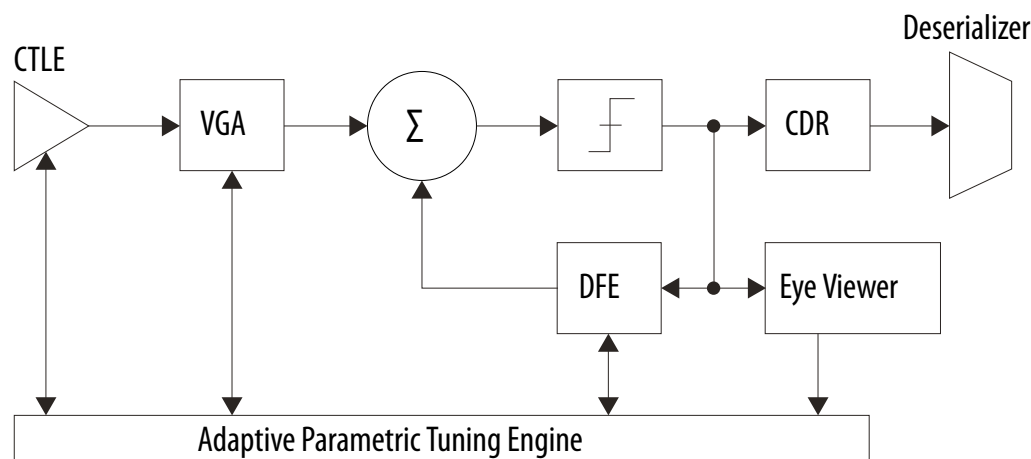
PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- **ATX PLL**—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.
- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.
- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- **Variable Gain Amplifier (VGA)**—to optimize the receiver's dynamic range
- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation
- **Decision Feedback Equalizer (DFE)**—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections
- **On-Die Instrumentation (ODI)**—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing

**Figure 7. Intel Stratix 10 Receiver Block Features**

All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

**Table 8. Transceiver PMA Features**

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps <sup>(8)</sup> to 28.3 Gbps (Intel Stratix 10 GX/SX devices)
Backplane Support	Drive backplanes at data rates up to 28.3 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, QSFPDD, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	15 fixed tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Advanced Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols, with optional fractional frequency synthesis capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost

*continued...*

<sup>(8)</sup> Stratix 10 transceivers can support data rates below 1 Gbps with over sampling.



PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit-slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 12.5	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.3	Custom	Custom

### Related Information

[Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide](#)

## 1.9. PCI Express Gen1/Gen2/Gen3 Hard IP

Intel Stratix 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, increased functionality, and designer productivity.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers. It also supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8/x16 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic (autonomous mode). This feature allows the PCI Express link to power up and complete link training in less than 100 ms, while the rest of the device is still in the process of being configured. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

The PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the device via protocol (CvP) across the PCI Express bus at Gen1/Gen2/Gen3 rates.

## 1.10. Interlaken PCS Hard IP

Intel Stratix 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Intel Stratix 10 devices.



Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

**Table 10. External Memory Interface Performance**

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

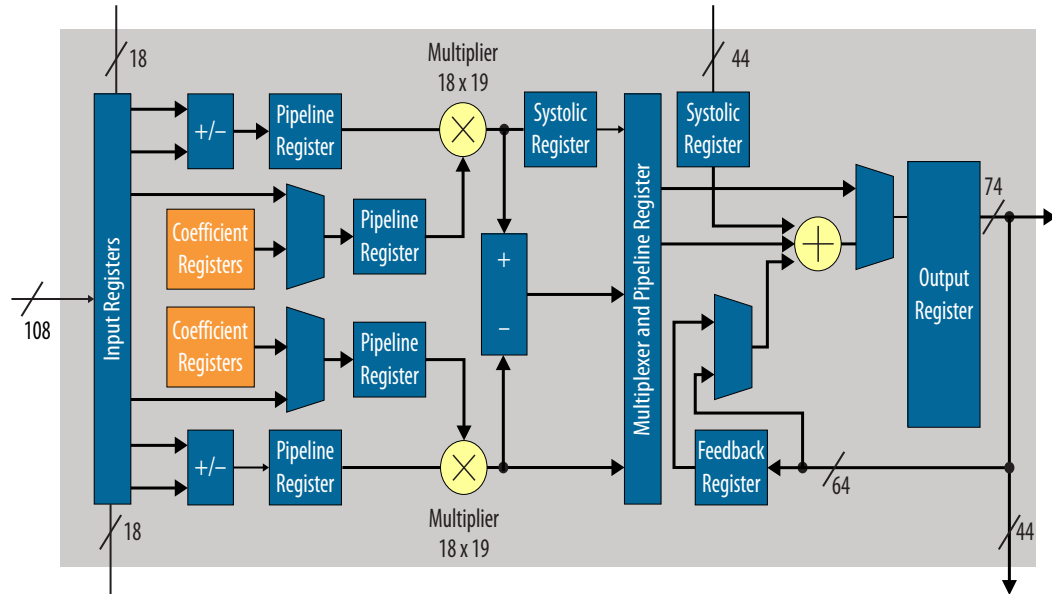
### 1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

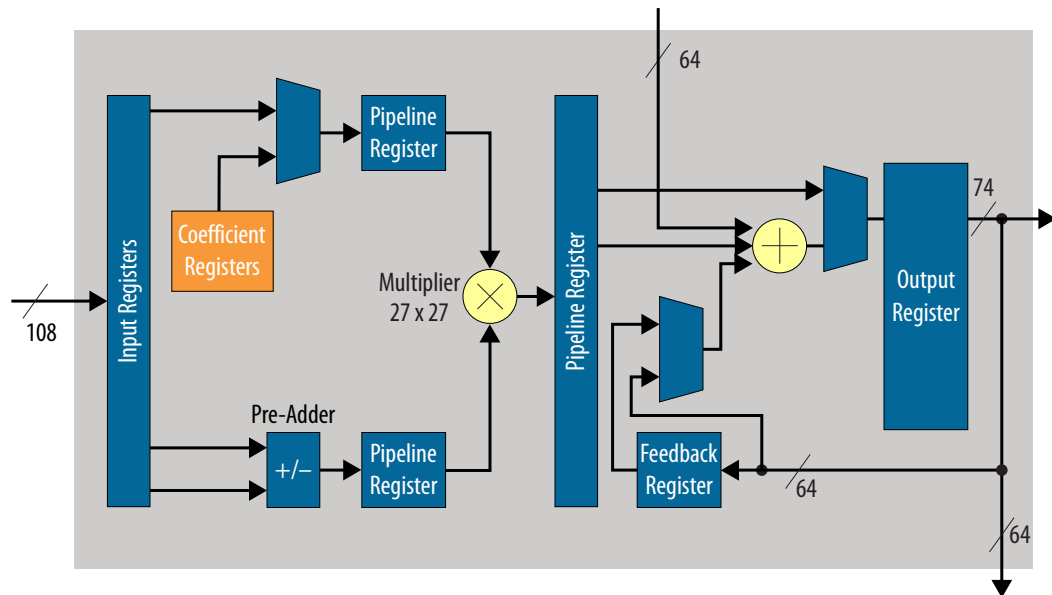
The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

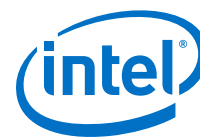
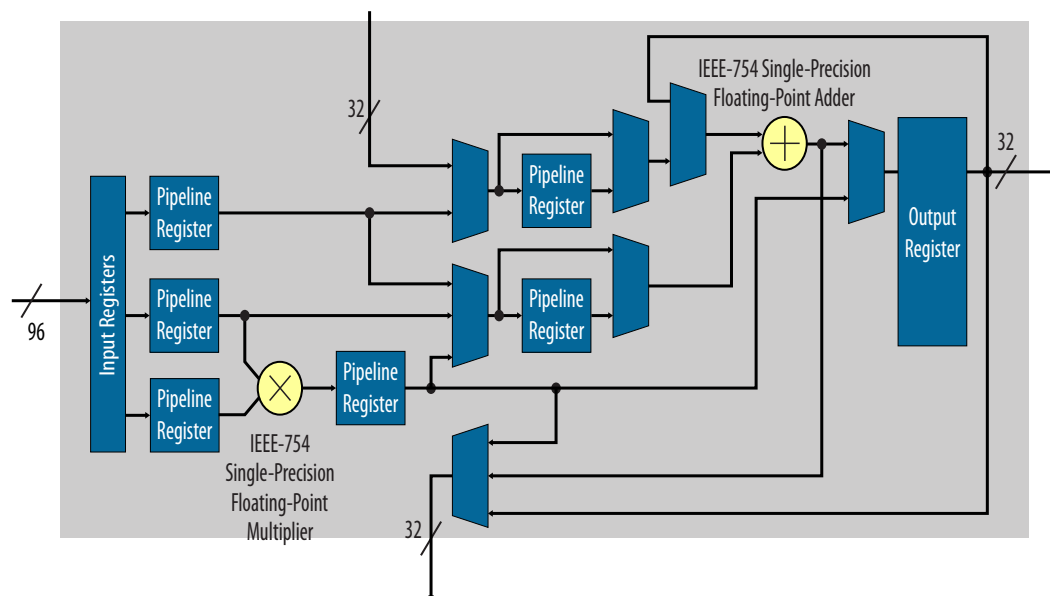
**Figure 10. DSP Block: Standard Precision Fixed Point Mode**



**Figure 11. DSP Block: High Precision Fixed Point Mode**





**Figure 12. DSP Block: Single Precision Floating Point Mode**

Each DSP block can be independently configured at compile time as either dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

In floating point mode, each DSP block provides one single precision floating point multiplier and adder. Floating point additions, multiplications, mult-adds and mult-accumulates are supported.

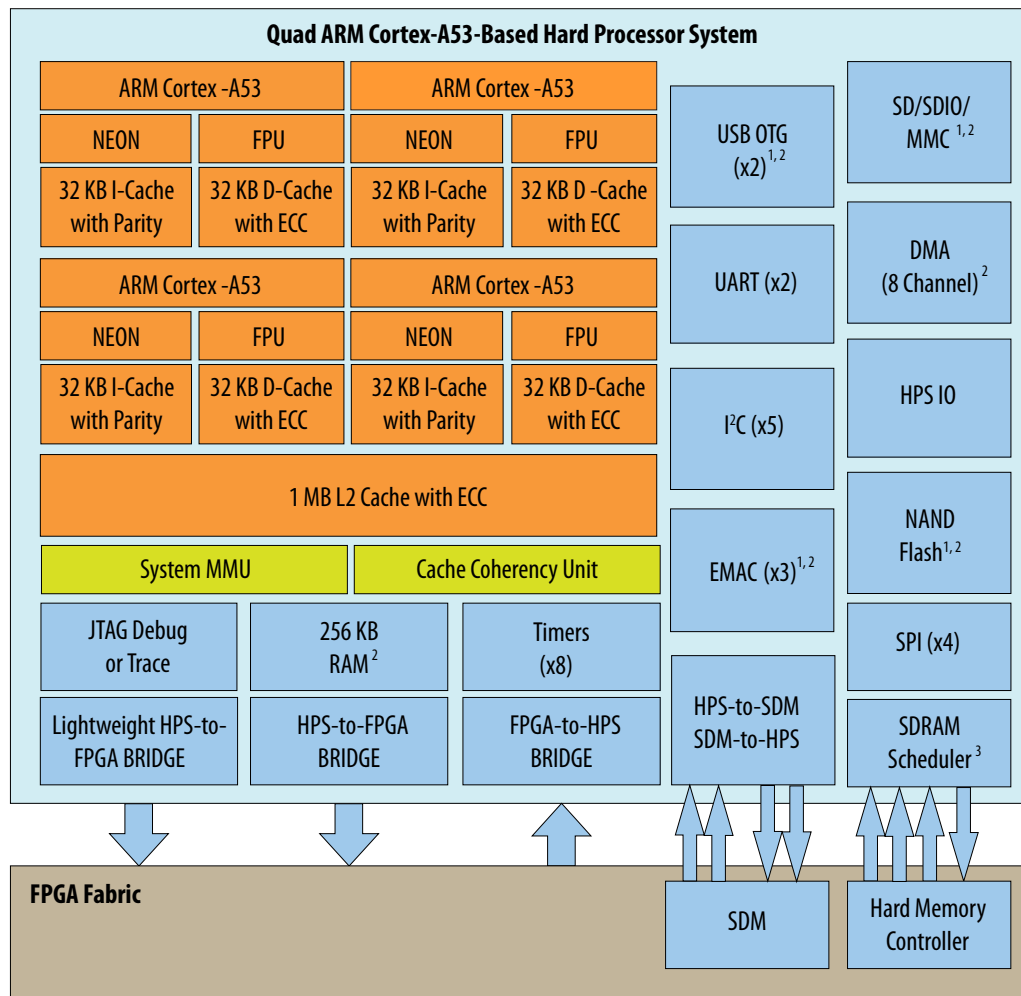
The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

**Table 12. Variable Precision DSP Block Configurations**

Multiplier Size	DSP Block Resources	Expected Usage
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFTs
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double Precision floating point
Single Precision floating point	1 Single Precision floating point adder, 1 Single Precision floating point multiplier	Floating point



Figure 13. HPS Block Diagram



- Notes:
1. Integrated direct memory access (DMA)
  2. Integrated error correction code (ECC)
  3. Multiport front-end interface to hard memory controller

### 1.18.1. Key Features of the Intel Stratix 10 HPS

Table 14. Key Features of the Intel Stratix 10 GX/SX HPS

Feature	Description
Quad-core ARM Cortex-A53 MPCore processor unit	<ul style="list-style-type: none"> <li>• 2.3 MIPS/MHz instruction efficiency</li> <li>• CPU frequency up to 1.5 GHz</li> <li>• At 1.5 GHz total performance of 13,800 MIPS</li> <li>• ARMv8-A architecture</li> <li>• Runs 64-bit and 32-bit ARM instructions</li> <li>• 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint</li> <li>• Jazelle® RCT execution architecture with 8-bit Java bytecodes</li> </ul>

*continued...*



## 1.19. Power Management

Intel Stratix 10 devices leverage the advanced Intel 14-nm Tri-Gate process technology, the all new HyperFlex core architecture to enable Hyper-Folding, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

With the new HyperFlex core architecture, designs can run 2X faster than previous generation FPGAs. With 2X performance and same required throughput, architects can cut the data path width in half to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

The optional power reduction techniques in Intel Stratix 10 devices include:

- **Available Low Static Power Devices**—Intel Stratix 10 devices are available with a fixed core voltage that provides lower static power than the SmartVID standard power devices, while maintaining device performance

Furthermore, Intel Stratix 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

## 1.20. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.



The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

## 1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

## 1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be



Document Version	Changes
	<ul style="list-style-type: none"> <li>• Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table.</li> <li>• Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table: <ul style="list-style-type: none"> <li>— Transceiver hard IP</li> <li>— Internal memory blocks</li> <li>— Core clock networks</li> <li>— Packaging</li> </ul> </li> <li>• Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section.</li> <li>• Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section.</li> <li>• Removed footnotes from the "Transceiver PCS Features" table.</li> <li>• Changed the HMC description in the "External Memory and General Purpose I/O" section.</li> <li>• Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section.</li> <li>• Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description in the "Internal Embedded Memory" section.</li> <li>• Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table.</li> <li>• Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section.</li> <li>• Updated the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table.</li> </ul>
2015.12.04	Initial release.