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Intel - 1SX280LU2F50E2LG Datasheet



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What are **Embedded - System On Chip (SoC)**?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore [™] with CoreSight [™]
Flash Size	-
RAM Size	256КВ
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2800K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2397-BBGA, FCBGA
Supplier Device Package	2397-FBGA, FC (50x50)
Purchase URL	https://www.e-xfl.com/product-detail/intel/1sx280lu2f50e2lg

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Contents

1.	Intel [®] Stratix [®] 10 GX/SX Device Overview	3
	1.1. Intel Stratix 10 Family Variants	4
	1.1.1. Available Options	6
	1.2. Innovations in Intel Stratix 10 FPGAs and SoCs	6
	1.3. FPGA and SoC Features Summary	8
	1.4. Intel Stratix 10 Block Diagram	11
	1.5. Intel Stratix 10 FPGA and SoC Family Plan	11
	1.6. HyperFlex Core Architecture	15
	1.7. Heterogeneous 3D SiP Transceiver Tiles	16
	1.8. Intel Stratix 10 Transceivers	17
	1.8.1. PMA Features	18
	1.8.2. PCS Features	20
	1.9. PCI Express Gen1/Gen2/Gen3 Hard IP	21
	1.10. Interlaken PCS Hard IP	21
	1.11. 10G Ethernet Hard IP	22
	1.12. External Memory and General Purpose I/O	22
	1.13. Adaptive Logic Module (ALM)	23
	1.14. Core Clocking	24
	1.15. Fractional Synthesis PLLs and I/O PLLs	25
	1.16. Internal Embedded Memory	25
	1.17. Variable Precision DSP Block	25
	1.18. Hard Processor System (HPS)	28
	1.18.1. Key Features of the Intel Stratix 10 HPS	29
	1.19. Power Management	32
	1.20. Device Configuration and Secure Device Manager (SDM)	32
	1.21. Device Security	34
	1.22. Configuration via Protocol Using PCI Express	34
	1.23. Partial and Dynamic Reconfiguration	35
	1.24. Fast Forward Compile	35
	1.25. Single Event Upset (SEU) Error Detection and Correction	35
	1.26. Document Revision History for the Intel Stratix 10 GX/SX Device Overview	36



1. Intel[®] Stratix[®] **10** GX/SX Device Overview

Intel's 14-nm Intel[®] Stratix[®] 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex[™] core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM[®] Cortex[®]-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express[®] Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

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Common to all Intel Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- M20K (20 kbit) embedded memory blocks
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units
- Fractional synthesis and integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose IO cells

To clock these building blocks, Intel Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Intel Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.



1.1.1. Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices



1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices

Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Process technology	28-nm TSMC (planar transistor)	14 nm Intel Tri-Gate (FinFET)
Hard processor core	None	Quad-core 64-bit ARM Cortex-A53 (SoC only)
Core architecture	Conventional core architecture with conventional interconnect	HyperFlex core architecture with Hyper-Registers in the interconnect
Core performance	500 MHz	1 GHz
Power dissipation	1x	As low as 0.3x
		continued



- Additional Hard IP: Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking**: Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs**: The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

1.3. FPGA and SoC Features Summary

Table 2. Intel Stratix 10 FPGA and SoC Common Device Features

Feature	Description		
Technology	 14-nm Intel Tri-Gate (FinFET) process technology SmartVID controlled core voltage, standard power devices 0.85-V fixed core voltage, low static power devices available 		
Low power serial transceivers	 Up to 96 total transceivers available Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices Extended range down to 125 Mbps with oversampling ATX transmit PLLs with user-configurable fractional synthesis capability XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support Adaptive linear and decision feedback equalization Transmit pre-emphasis and de-emphasis Dynamic partial reconfiguration of individual transceiver channels On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring) 		
General purpose I/Os	 Up to 1640 total GPIO available 1.6 Gbps LVDS—every pair can be configured as an input or output 1333 MHz/2666 Mbps DDR4 external memory interface 1067 MHz/2133 Mbps DDR3 external memory interface 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing On-chip termination (OCT) 		
Embedded hard IP	 PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller) Multiple hard IP instantiations in each device Single Root I/O Virtualization (SR-IOV) 		
Transceiver hard IP	 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) 10G Ethernet PCS PCI Express PIPE interface Interlaken PCS Gigabit Ethernet PCS Deterministic latency support for Common Public Radio Interface (CPRI) PCS Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS 8B/10B, 64B/66B, 64B/67B encoders and decoders Custom mode support for proprietary protocols 		
	continued		

1. Intel[®] Stratix[®] 10 GX/SX Device Overview S10-OVERVIEW | 2018.08.08



SoC Subsystem	Feature	Description
	NAND flash controller	• 1 ONFI 1.0, 8- and 16-bit support
	General-purpose I/O (GPIO)	Maximum of 48 software programmable GPIO
	Timers	 4 general-purpose timers 4 watchdog timers
Secure Device Manager	Security	 Secure boot Advanced Encryption Standard (AES) and authentication (SHA/ECDSA)
External Memory Interface	External Memory Interface	 Hard Memory Controller with DDR4 and DDR3, and LPDDR3

1.4. Intel Stratix 10 Block Diagram

Figure 2. Intel Stratix 10 FPGA and SoC Architecture Block Diagram



HPS: Quad ARM Cortex-A53 Hard Processor System SDM: Secure Device Manager EMIB: Embedded Multi-Die Interconnect Bridge

1.5. Intel Stratix 10 FPGA and SoC Family Plan

⁽¹⁾ The number of 27x27 multipliers is one-half the number of 18x19 multipliers.



Intel Stratix 10 GX/SX Device Name	Logic Elements (KLE)	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	18x19 Multi- pliers ⁽¹⁾
GX 400/ SX 400	378	1,537	30	3,204	2	1,296
GX 650/ SX 650	612	2,489	49	5,184	3	2,304
GX 850/ SX 850	841	3,477	68	7,124	4	4,032
GX 1100/ SX 1100	1,092	4,401	86	9,540	6	5,040
GX 1650/ SX 1650	1,624	5,851	114	13,764	8	6,290
GX 2100/ SX 2100	2,005	6,501	127	17,316	11	7,488
GX 2500/ SX 2500	2,422	9,963	195	20,529	13	10,022
GX 2800/ SX 2800	2,753	11,721	229	23,796	15	11,520
GX 4500/ SX 4500	4,463	7,033	137	37,821	23	3,960
GX 5500/ SX 5500	5,510	7,033	137	47,700	29	3,960

Table 4. Intel Stratix 10 GX/SX FPGA and SoC Family Plan—FPGA Core (part 1)

Table 5.Intel Stratix 10 GX/SX FPGA and SoC Family Plan—Interconnects, PLLs and
Hard IP (part 2)

Intel Stratix 10	Interco	Interconnects		PLLs	
Name	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 400/ SX 400	392	24	8	8	1
GX 650/ SX 650	400	48	16	8	2
GX 850/ SX 850	736	48	16	15	2
GX 1100/ SX 1100	736	48	16	15	2
GX 1650/ SX 1650	704	96	32	14	4
GX 2100/ SX 2100	704	96	32	14	4
GX 2500/ SX 2500	1160	96	32	24	4
continued					



Intel Stratix 10	Interconnects		PLLs		Hard IP
GX/SX Device Name	Maximum GPIOs	Maximum XCVR	fPLLs	I/O PLLs	PCIe Hard IP Blocks
GX 2800/ SX 2800	1160	96	32	24	4
GX 4500/ SX 4500	1640	24	8	34	1
GX 5500/ SX 5500	1640	24	8	34	1

Table 6.Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 1

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers (2) (3) (4) (5) (6) (7)

Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm ²)	F1760 NF43 (42.5x42.5 mm ²)	F1760 NF43 (42.5x42.5 mm ²)
GX 400/ SX 400	392, 8, 192, 24		
GX 650/ SX 650	392, 8, 192, 24	400, 16, 192, 48	
GX 850/ SX 850			688, 16, 336, 48
GX 1100/ SX 1100			688, 16, 336, 48
GX 1650/ SX 1650			688, 16, 336, 48
GX 2100/ SX 2100			688, 16, 336, 48
GX 2500/ SX 2500			688, 16, 336, 48
GX 2800/			688, 16, 336, 48

⁽²⁾ All packages are ball grid arrays with 1.0 mm pitch.

- ⁽³⁾ High-Voltage I/O pins are used for 3 V and 2.5 V interfacing.
- ⁽⁴⁾ Each LVDS pair can be configured as either a differential input or a differential output.
- ⁽⁵⁾ High-Voltage I/O pins and LVDS pairs are included in the General Purpose I/O count. Transceivers are counted separately.
- ⁽⁶⁾ Each package column offers pin migration (common circuit board footprint) for all devices in the column.
- ⁽⁷⁾ Intel Stratix 10 GX devices are pin migratable with Intel Stratix 10 SX devices in the same package.



Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm ²)	F1760 NF43 (42.5x42.5 mm ²)	F1760 NF43 (42.5x42.5 mm ²)
SX 2800			
GX 4500/ SX 4500			
GX 5500/ SX 5500			

Table 7. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 2

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers (2) (3) (4) (5) (6) (7)

Intel Stratix 10 GX/SX Device Name	F2112 NF48 (47.5x47.5 mm ²)	F2397 UF50 (50x50 mm ²)	F2912 HF55 (55x55 mm ²)
GX 400/ SX 400			
GX 650/ SX 650			
GX 850/ SX 850	736, 16, 360, 48		
GX 1100/ SX 1100	736, 16, 360, 48		
GX 1650/ SX 1650		704, 32, 336, 96	
GX 2100/ SX 2100		704, 32, 336, 96	
GX 2500/ SX 2500		704, 32, 336, 96	1160, 8, 576, 24
GX 2800/ SX 2800		704, 32, 336, 96	1160, 8, 576, 24
GX 4500/ SX 4500			1640, 8, 816, 24
GX 5500/ SX 5500			1640, 8, 816, 24



Figure 4. HyperFlex Core Architecture



New Hyper-Registers throughout the core fabric

1.7. Heterogeneous 3D SiP Transceiver Tiles

Intel Stratix 10 FPGAs and SoCs feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles, each containing 24 full-duplex transceiver channels. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

Figure 5. Monolithic Core Fabric and Heterogeneous 3D SiP Transceiver Tiles





Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

1.8.1. PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- ATX PLL—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.
- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.
- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multiprotocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- Variable Gain Amplifier (VGA)—to optimize the receiver's dynamic range
- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation
- Decision Feedback Equalizer (DFE)—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections
- On-Die Instrumentation (ODI)—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing



Feature	Capability
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation— Eye Viewer and Jitter Margin Tool	Simplify board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (Eye Viewer). Also inject jitter from transmitter to test link margin in system.
Dynamic Reconfiguration	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility.
Multiple PCS-PMA and PCS- Core to FPGA fabric interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

1.8.2. PCS Features

Intel Stratix 10 PMA channels interface with core logic through configurable and bypassable PCS interface layers.

The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. This feature provides the flexibility to implement a wide range of applications with 8, 10, 16, 20, 32, 40, or 64-bit interface width between each transceiver and the core logic.

The PCS also contains hard IP to support a variety of standard and proprietary protocols across a wide range of data rates and encoding schemes. The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports 64B/66B and 64B/67B encoded applications up to 17.4 Gbps. The enhanced PCS mode also includes an integrated 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit. For highly customized implementations, a PCS Direct mode provides an interface up to 64 bits wide to allow for custom encoding and support for data rates up to 28.3 Gbps.

For more information about the PCS-Core interface or the double rate transfer mode, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*, and the *Intel Stratix 10 E-Tile Transceiver PHY User Guide*.

PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Standard PCS	1 to 12.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slipper, channel bonding	Rate match FIFO, word-aligner, 8B/10B decoder, byte deserializer, byte ordering
PCI Express Gen1/Gen2 x1, x2, x4, x8, x16	2.5 and 5.0	Same as Standard PCS plus PIPE 2.0 interface to core	Same as Standard PCS plus PIPE 2.0 interface to core
PCI Express Gen3 x1, x2, x4, x8, x16	8.0	Phase compensation FIFO, byte serializer, encoder, scrambler, bit- slipper, gear box, channel bonding, and PIPE 3.0 interface to core, auto speed negotiation	Rate match FIFO (0-600 ppm mode), word-aligner, decoder, descrambler, phase compensation FIFO, block sync, byte deserializer, byte ordering, PIPE 3.0 interface to core, auto speed negotiation
CPRI	0.6144 to 9.8	Same as Standard PCS plus deterministic latency serialization	Same as Standard PCS plus deterministic latency deserialization
			continued

Table 9. Transceiver PCS Features



PCS Protocol Support	Data Rate (Gbps)	Transmitter Data Path	Receiver Data Path
Enhanced PCS	2.5 to 17.4	FIFO, channel bonding, bit-slipper, and gear box	FIFO, block sync, bit-slipper, and gear box
10GBASE-R	10.3125	FIFO, 64B/66B encoder, scrambler, FEC, and gear box	FIFO, 64B/66B decoder, descrambler, block sync, FEC, and gear box
Interlaken	4.9 to 17.4	FIFO, channel bonding, frame generator, CRC-32 generator, scrambler, disparity generator, bit- slipper, and gear box	FIFO, CRC-32 checker, frame sync, descrambler, disparity checker, block sync, and gear box
SFI-S/SFI-5.2	11.3	FIFO, channel bonding, bit-slipper, and gear box	FIFO, bit-slipper, and gear box
IEEE 1588	1.25 to 10.3125	FIFO (fixed latency), 64B/66B encoder, scrambler, and gear box	FIFO (fixed latency), 64B/66B decoder, descrambler, block sync, and gear box
SDI	up to 12.5	FIFO and gear box	FIFO, bit-slipper, and gear box
GigE	1.25	Same as Standard PCS plus GigE state machine	Same as Standard PCS plus GigE state machine
PCS Direct	up to 28.3	Custom	Custom

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

1.9. PCI Express Gen1/Gen2/Gen3 Hard IP

Intel Stratix 10 devices contain embedded PCI Express hard IP designed for performance, ease-of-use, increased functionality, and designer productivity.

The PCI Express hard IP consists of the PHY, Data Link, and Transaction layers. It also supports PCI Express Gen1/Gen2/Gen3 end point and root port, in x1/x2/x4/x8/x16 lane configurations. The PCI Express hard IP is capable of operating independently from the core logic (autonomous mode). This feature allows the PCI Express link to power up and complete link training in less than 100 ms, while the rest of the device is still in the process of being configured. The hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

The PCI Express hard IP has improved end-to-end data path protection using Error Checking and Correction (ECC). In addition, the hard IP supports configuration of the device via protocol (CvP) across the PCI Express bus at Gen1/Gen2/Gen3 rates.

1.10. Interlaken PCS Hard IP

Intel Stratix 10 devices have integrated Interlaken PCS hard IP supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS hard IP is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which has demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS hard IP is present in every transceiver channel in Intel Stratix 10 devices.



Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios[®] II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Table 10. External Memory Interface Performance

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.





Figure 9. Intel Stratix 10 FPGA and SoC ALM Block Diagram

Key features and capabilities of the ALM include:

- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the new HyperFlex architecture, enables Intel Stratix 10 devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Stratix 10 ALM architecture.

1.14. Core Clocking

Core clocking in Intel Stratix 10 devices makes use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.



	Quad ARM Cortex-A53-Based Hard Processor System							
	ARM Cort	tex -A5	53	ARM		tex -A53		SD/SDIO/
	NEON		FPU	NEON		FPU	USB OTG $(-2)^{1/2}$	MMC ^{1,2}
	32 KB I-Cache with Parity	32 K w	B D-Cache vith ECC	32 KB I-Cache with Parity		32 KB D -Cache with ECC	(XZ)	
	ARM Cort	tex -A5	53	ARM Cortex -A53		UART (x2)	DMA (8 Channel) ²	
	NEON		FPU	NEON		FPU		
	32 KB I-Cache with Parity	32 K w	B D-Cache vith ECC	32 KB I-Ca with Par	ache ity	32 KB D-Cache with ECC	l²C (x5)	HPS IO
	1 MB L2 Cache with FCC							
	System MMU		Cache Coherency Unit		EMAC (x3) ^{1, 2}	NAND Flash ^{1, 2}		
	JTAG Debug or Trace	bug 256 :e R/		5 KB AM ²		Timers (x8)		SPI (x4)
	Lightweight HPS-to- FPGA BRIDGE		HPS-te BRI	o-FPGA DGE		FPGA-to-HPS BRIDGE	HPS-to-SDM SDM-to-HPS	SDRAM Scheduler ³
FP	'GA Fabric						SDM	Hard Memory Controller

Figure 13. HPS Block Diagram

Notes:

1. Integrated direct memory access (DMA)

2. Integrated error correction code (ECC)

3. Multiport front-end interface to hard memory controller

1.18.1. Key Features of the Intel Stratix 10 HPS

Table 14. Key Features of the Intel Stratix 10 GX/SX HPS

Feature	Description		
Quad-core ARM Cortex-A53 MPCore processor unit	 2.3 MIPS/MHz instruction efficiency CPU frequency up to 1.5 GHz At 1.5 GHz total performance of 13,800 MIPS ARMv8-A architecture Runs 64-bit and 32-bit ARM instructions 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint Jazelle[®] RCT execution architecture with 8-bit Java bytecodes 		
	continued		



1.19. Power Management

Intel Stratix 10 devices leverage the advanced Intel 14-nm Tri-Gate process technology, the all new HyperFlex core architecture to enable Hyper-Folding, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

With the new HyperFlex core architecture, designs can run 2X faster than previous generation FPGAs. With 2X performance and same required throughput, architects can cut the data path width in half to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

The optional power reduction techniques in Intel Stratix 10 devices include:

• Available Low Static Power Devices—Intel Stratix 10 devices are available with a fixed core voltage that provides lower static power than the SmartVID standard power devices, while maintaining device performance

Furthermore, Intel Stratix 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

1.20. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.



Figure 14. SDM Block Diagram



During configuration, Intel Stratix 10 devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.



The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process
- Reconfiguration of one or more sectors independent of all other sectors
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

1.21. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Stratix 10 FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Boot code authentication for the HPS
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)

The SDM and associated security services provide a robust, multi-layered security solution for your Intel Stratix 10 design.

1.22. Configuration via Protocol Using PCI Express

Configuration via protocol using PCI Express allows the FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured, this technique allows the PCI Express bus to be





The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.

The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 14-nm Tri-Gate process technology used for Intel Stratix 10 devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

1.26. Document Revision History for the Intel Stratix **10** GX/SX Device Overview

Document Version	Changes
2018.08.08	 Made the following changes: Changed the specs for QDRII+ and QDRII+ Xtreme and added specs for QDRIV in the "External Memory Interface Performance" table. Updated description of the power options in the "Sample Ordering COde and Available Options for Intel Stratix 10 Devices" figure. Changed the description of the technology and power management features in the "Intel Stratix 10 FPGA and SoC Common Device Features" table. Changed the description of SmartVID in the "Power Management" section. Changed the direction arrow from the coefficient registers block in the "DSP Block: High Precision Fixed Point Mode" figure.
2017.10.30	 Made the following changes: Removed the embedded eSRAM feature globally. Removed the Low Power (VID) and Military operating temperature options, and package code 53 from the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure. Changed the Maximum transceiver data rate (chip-to-chip) specification for L-Tile devices in the "Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices" table.
2016.10.31	 Made the following changes: Changed the number of available transceivers to 96, globally. Changed the single-precision floating point performance to 10 TeraFLOPS, globally. Changed the maximum datarate to 28.3 Gbps, globally. Changed some of the features listed in the "Stratix 10 GX/SX Device Overview" section. Changed descriptions for the GX and SX devices in the "Stratix 10 Family Variants" section. Changed the "Sample Ordering Code and Available Options for Stratix 10 Devices" figure.