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### **[Embedded - System On Chip \(SoC\): The Heart of Modern Embedded Systems](#)**

[Embedded - System On Chip \(SoC\)](#) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are [Embedded - System On Chip \(SoC\)](#)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 2800K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	2397-BBGA, FCBGA
Supplier Device Package	2397-FBGA, FC (50x50)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/1sx280lu3f50i3vg">https://www.e-xfl.com/product-detail/intel/1sx280lu3f50i3vg</a>



## 1. Intel® Stratix® 10 GX/SX Device Overview

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Intel's 14-nm Intel® Stratix® 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Intel Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric. Intel Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Intel Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees

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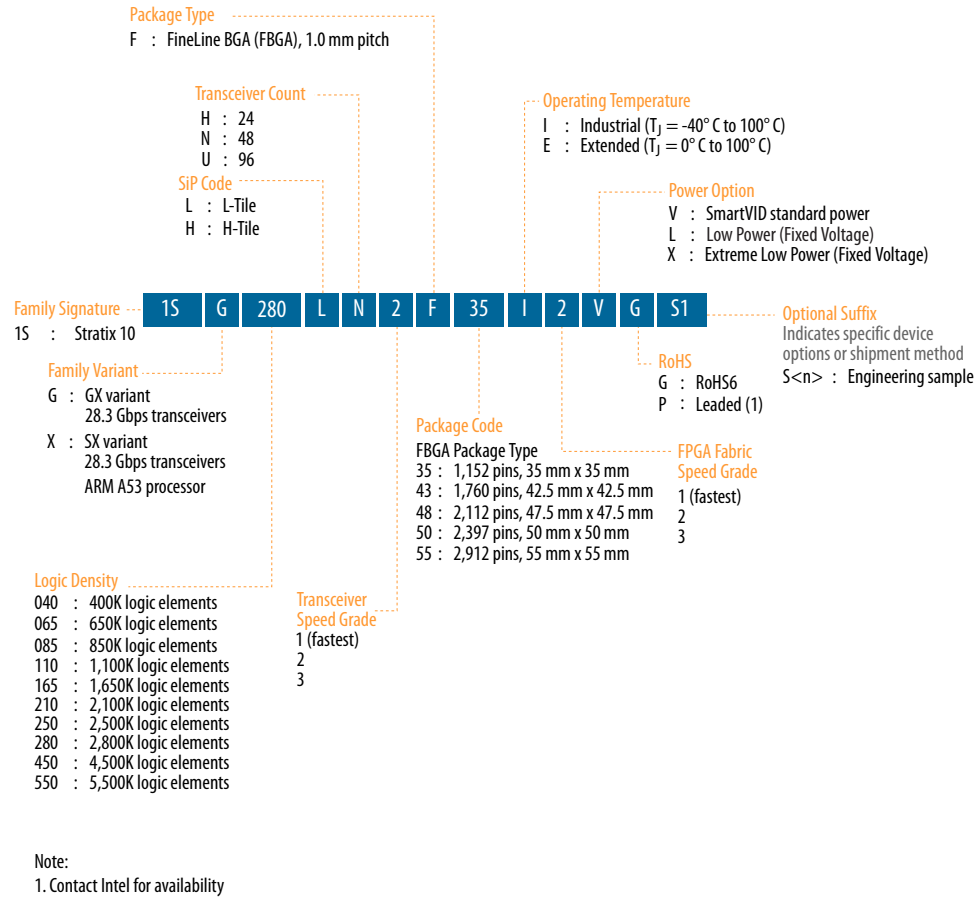
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### 1.1.1. Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Stratix 10 Devices



## 1.2. Innovations in Intel Stratix 10 FPGAs and SoCs

Intel Stratix 10 FPGAs and SoCs deliver many significant improvements over the previous generation high-performance Stratix V FPGAs.

Table 1. Key Features of Intel Stratix 10 Devices Compared to Stratix V Devices

Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
Process technology	28-nm TSMC (planar transistor)	14 nm Intel Tri-Gate (FinFET)
Hard processor core	None	Quad-core 64-bit ARM Cortex-A53 (SoC only)
Core architecture	Conventional core architecture with conventional interconnect	HyperFlex core architecture with Hyper-Registers in the interconnect
Core performance	500 MHz	1 GHz
Power dissipation	1x	As low as 0.3x
continued...		



Feature	Stratix V FPGAs	Intel Stratix 10 FPGAs and SoCs
<b>Logic density</b>	952 KLE (monolithic)	5,500 KLE (monolithic)
<b>Embedded memory (M20K)</b>	52 Mbits	229 Mbits
<b>18x19 multipliers</b>	3,926 <i>Note:</i> Multiplier is 18x18 in Stratix V devices.	11,520 <i>Note:</i> Multiplier is 18x19 in Intel Stratix 10 devices.
<b>Floating point DSP capability</b>	Up to 1 TFLOP, requires soft floating point adder and multiplier	Up to 10 TFLOPS, hard IEEE 754 compliant single precision floating point adder and multiplier
<b>Maximum transceivers</b>	66	96
<b>Maximum transceiver data rate (chip-to-chip)</b>	28.05 Gbps	28.3 Gbps L-Tile 28.3 Gbps H-Tile
<b>Maximum transceiver data rate (backplane)</b>	12.5 Gbps	12.5 Gbps L-Tile 28.3 Gbps H-Tile
<b>Hard memory controller</b>	None	DDR4 @ 1333 MHz/2666 Mbps DDR3 @ 1067 MHz/2133 Mbps
<b>Hard protocol IP</b>	PCIe Gen3 x8 (up to 4 instances)	PCIe Gen3 x16 (up to 4 instances) SR-IOV (4 physical functions / 2k virtual functions) on H-Tile devices 10GBASE-KR/40GBASE-KR4 FEC
<b>Core clocking and PLLs</b>	Global, quadrant and regional clocks supported by fractional-synthesis fPLLs	Programmable clock tree synthesis supported by fractional synthesis fPLLs and integer IO PLLs
<b>Register state readback and writeback</b>	Not available	Non-destructive register state readback and writeback for ASIC prototyping and other applications

These innovations result in the following improvements:

- **Improved Core Logic Performance:** The HyperFlex core architecture combined with Intel's 14-nm Tri-Gate technology allows Intel Stratix 10 devices to achieve 2X the core performance compared to the previous generation
- **Lower Power:** Intel Stratix 10 devices use up to 70% lower power compared to the previous generation, enabled by 14-nm Intel Tri-Gate technology, the HyperFlex core architecture, and optional power saving features built into the architecture
- **Higher Density:** Intel Stratix 10 devices offer over five times the level of integration, with up to 5,500K logic elements (LEs) in a monolithic fabric, over 229 Mbits of embedded memory blocks (M20K), and 11,520 18x19 multipliers
- **Embedded Processing:** Intel Stratix 10 SoCs feature a Quad-Core 64-bit ARM Cortex-A53 processor optimized for power efficiency and software compatible with previous generation Arria and Cyclone SoC devices
- **Improved Transceiver Performance:** With up to 96 transceiver channels implemented in heterogeneous 3D SiP transceiver tiles, Intel Stratix 10 GX and SX devices support data rates up to 28.3 Gbps chip-to-chip and 28.3 Gbps across the backplane with signal conditioning circuits capable of equalizing over 30 dB of system loss
- **Improved DSP Performance:** The variable precision DSP block in Intel Stratix 10 devices features hard fixed and floating point capability, with up to 10 TeraFLOPS IEEE754 single-precision floating point performance



- **Additional Hard IP:** Intel Stratix 10 devices include many more hard IP blocks than previous generation devices, with a hard memory controller included in each bank of 48 general purpose IOs, a hard PCIe Gen3 x16 full protocol stack in each transceiver tile, and a hard 10GBASE-KR/40GBASE-KR4 FEC in every transceiver channel
- **Enhanced Core Clocking:** Intel Stratix 10 devices feature programmable clock tree synthesis; clock trees are only synthesized where needed, increasing the flexibility and reducing the power dissipation of the clocking solution
- **Additional Core PLLs:** The core fabric in Intel Stratix 10 devices is supported by both integer IO PLLs and fractional synthesis fPLLs, resulting in a greater total number of PLLs available than the previous generation

### 1.3. FPGA and SoC Features Summary

**Table 2. Intel Stratix 10 FPGA and SoC Common Device Features**

Feature	Description
Technology	<ul style="list-style-type: none"><li>• 14-nm Intel Tri-Gate (FinFET) process technology</li><li>• SmartVID controlled core voltage, standard power devices</li><li>• 0.85-V fixed core voltage, low static power devices available</li></ul>
Low power serial transceivers	<ul style="list-style-type: none"><li>• Up to 96 total transceivers available</li><li>• Continuous operating range of 1 Gbps to 28.3 Gbps for Intel Stratix 10 GX/SX devices</li><li>• Backplane support up to 28.3 Gbps for Intel Stratix 10 GX/SX devices</li><li>• Extended range down to 125 Mbps with oversampling</li><li>• ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>• XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support</li><li>• Adaptive linear and decision feedback equalization</li><li>• Transmit pre-emphasis and de-emphasis</li><li>• Dynamic partial reconfiguration of individual transceiver channels</li><li>• On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)</li></ul>
General purpose I/Os	<ul style="list-style-type: none"><li>• Up to 1640 total GPIO available</li><li>• 1.6 Gbps LVDS—every pair can be configured as an input or output</li><li>• 1333 MHz/2666 Mbps DDR4 external memory interface</li><li>• 1067 MHz/2133 Mbps DDR3 external memory interface</li><li>• 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing</li><li>• On-chip termination (OCT)</li></ul>
Embedded hard IP	<ul style="list-style-type: none"><li>• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port</li><li>• DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller)</li><li>• Multiple hard IP instantiations in each device</li><li>• Single Root I/O Virtualization (SR-IOV)</li></ul>
Transceiver hard IP	<ul style="list-style-type: none"><li>• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>• 10G Ethernet PCS</li><li>• PCI Express PIPE interface</li><li>• Interlaken PCS</li><li>• Gigabit Ethernet PCS</li><li>• Deterministic latency support for Common Public Radio Interface (CPRI) PCS</li><li>• Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS</li><li>• 8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>• Custom mode support for proprietary protocols</li></ul>
continued...	



Feature	Description
Power management	<ul style="list-style-type: none"> <li>SmartVID controlled core voltage, standard power devices</li> <li>0.85-V fixed core voltage, low static power devices available</li> <li>Intel Quartus® Prime Pro Edition integrated power analysis</li> </ul>
High performance monolithic core fabric	<ul style="list-style-type: none"> <li>HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks</li> <li>Monolithic fabric minimizes compile times and increases logic utilization</li> <li>Enhanced adaptive logic module (ALM)</li> <li>Improved multi-track routing architecture reduces congestion and improves compile times</li> <li>Hierarchical core clocking architecture with programmable clock tree synthesis</li> <li>Fine-grained partial reconfiguration</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>M20K—20-Kbit with hard ECC support</li> <li>MLAB—640-bit distributed LUTRAM</li> </ul>
Variable precision DSP blocks	<ul style="list-style-type: none"> <li>IEEE 754-compliant hard single-precision floating point capability</li> <li>Supports signal processing with precision ranging from 18x19 up to 54x54</li> <li>Native 27x27 and 18x19 multiply modes</li> <li>64-bit accumulator and cascade for systolic FIRs</li> <li>Internal coefficient memory banks</li> <li>Pre-adder/subtractor improves efficiency</li> <li>Additional pipeline register increases performance and reduces power</li> </ul>
Phase locked loops (PLL)	<ul style="list-style-type: none"> <li>Fractional synthesis PLLs (fPLL) support both fractional and integer modes</li> <li>Fractional mode with third-order delta-sigma modulation</li> <li>Precision frequency synthesis</li> <li>Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering</li> </ul>
Core clock networks	<ul style="list-style-type: none"> <li>1 GHz fabric clocking</li> <li>667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface</li> <li>800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface</li> <li>Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks</li> <li>Clocks only synthesized where needed, to minimize dynamic power</li> </ul>
<b>continued...</b>	



Feature	Description
Configuration	<ul style="list-style-type: none"><li>• Dedicated Secure Device Manager</li><li>• Software programmable device configuration</li><li>• Serial and parallel flash interface</li><li>• Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3</li><li>• Fine-grained partial reconfiguration of core fabric</li><li>• Dynamic reconfiguration of transceivers and PLLs</li><li>• Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication</li><li>• Physically Unclonable Function (PUF) service</li></ul>
Packaging	<ul style="list-style-type: none"><li>• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology</li><li>• Multiple devices with identical package footprints allows seamless migration across different device densities</li><li>• 1.0 mm ball-pitch FBGA packaging</li><li>• Lead and lead-free package options</li></ul>
Software and tools	<ul style="list-style-type: none"><li>• Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow</li><li>• Fast Forward compiler to allow HyperFlex architecture performance exploration</li><li>• Transceiver toolkit</li><li>• Platform designer integration tool</li><li>• DSP Builder advanced blockset</li><li>• OpenCL™ support</li><li>• SoC Embedded Design Suite (EDS)</li></ul>

Table 3. Intel Stratix 10 SoC Specific Device Features

SoC Subsystem	Feature	Description
<b>Hard Processor System</b>	Multi-processor unit (MPU) core	<ul style="list-style-type: none"><li>• Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology</li><li>• Scalar floating-point unit supporting single and double precision</li><li>• ARM NEON media processing engine for each processor</li></ul>
	System Controllers	<ul style="list-style-type: none"><li>• System Memory Management Unit (SMMU)</li><li>• Cache Coherency Unit (CCU)</li></ul>
	Layer 1 Cache	<ul style="list-style-type: none"><li>• 32 KB L1 instruction cache with parity</li><li>• 32 KB L1 data cache with ECC</li></ul>
	Layer 2 Cache	<ul style="list-style-type: none"><li>• 1 MB Shared L2 Cache with ECC</li></ul>
	On-Chip Memory	<ul style="list-style-type: none"><li>• 256 KB On-Chip RAM</li></ul>
	Direct memory access (DMA) controller	<ul style="list-style-type: none"><li>• 8-Channel DMA</li></ul>
	Ethernet media access controller (EMAC)	<ul style="list-style-type: none"><li>• Three 10/100/1000 EMAC with integrated DMA</li></ul>
	USB On-The-Go controller (OTG)	<ul style="list-style-type: none"><li>• 2 USB OTG with integrated DMA</li></ul>
	UART controller	<ul style="list-style-type: none"><li>• 2 UART 16550 compatible</li></ul>
	Serial Peripheral Interface (SPI) controller	<ul style="list-style-type: none"><li>• 4 SPI</li></ul>
	I <sup>2</sup> C controller	<ul style="list-style-type: none"><li>• 5 I<sup>2</sup>C controllers</li></ul>
	SD/SDIO/MMC controller	<ul style="list-style-type: none"><li>• 1 eMMC version 4.5 with DMA and CE-ATA support</li><li>• SD, including eSD, version 3.0</li><li>• SDIO, including eSDIO, version 3.0</li><li>• CE-ATA - version 1.1</li></ul>
continued...		



Intel Stratix 10 GX/SX Device Name	F1152 HF35 (35x35 mm <sup>2</sup> )	F1760 NF43 (42.5x42.5 mm <sup>2</sup> )	F1760 NF43 (42.5x42.5 mm <sup>2</sup> )
SX 2800			
GX 4500/ SX 4500			
GX 5500/ SX 5500			

**Table 7. Intel Stratix 10 GX/SX FPGA and SoC Family Package Plan, part 2**

Cell legend: General Purpose I/Os, High-Voltage I/Os, LVDS Pairs, Transceivers <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup> <sup>(5)</sup> <sup>(6)</sup> <sup>(7)</sup>

Intel Stratix 10 GX/SX Device Name	F2112 NF48 (47.5x47.5 mm <sup>2</sup> )	F2397 UF50 (50x50 mm <sup>2</sup> )	F2912 HF55 (55x55 mm <sup>2</sup> )
GX 400/ SX 400			
GX 650/ SX 650			
GX 850/ SX 850	736, 16, 360, 48		
GX 1100/ SX 1100	736, 16, 360, 48		
GX 1650/ SX 1650		704, 32, 336, 96	
GX 2100/ SX 2100		704, 32, 336, 96	
GX 2500/ SX 2500		704, 32, 336, 96	1160, 8, 576, 24
GX 2800/ SX 2800		704, 32, 336, 96	1160, 8, 576, 24
GX 4500/ SX 4500			1640, 8, 816, 24
GX 5500/ SX 5500			1640, 8, 816, 24





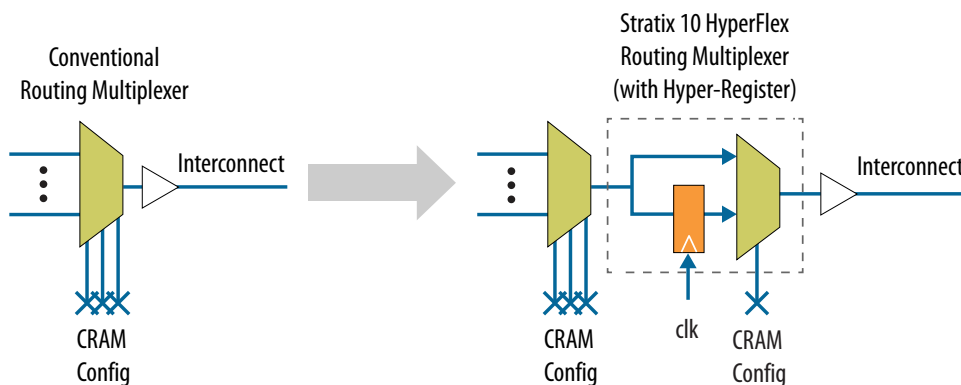
## 1.6. HyperFlex Core Architecture

Intel Stratix 10 FPGAs and SoCs are based on a monolithic core fabric featuring the new HyperFlex core architecture. The HyperFlex core architecture delivers 2X the clock frequency performance and up to 70% lower power compared to previous generation high-end FPGAs. Along with this performance breakthrough, the HyperFlex core architecture delivers a number of advantages including:

- **Higher Throughput**—Leverages 2X core clock frequency performance to obtain throughput breakthroughs
- **Improved Power Efficiency**—Uses reduced IP size, enabled by HyperFlex, to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 70% versus previous generation devices
- **Greater Design Functionality**—Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity**—Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALM), the HyperFlex core architecture introduces additional bypassable registers everywhere throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks.

**Figure 3. Bypassable Hyper-Register**

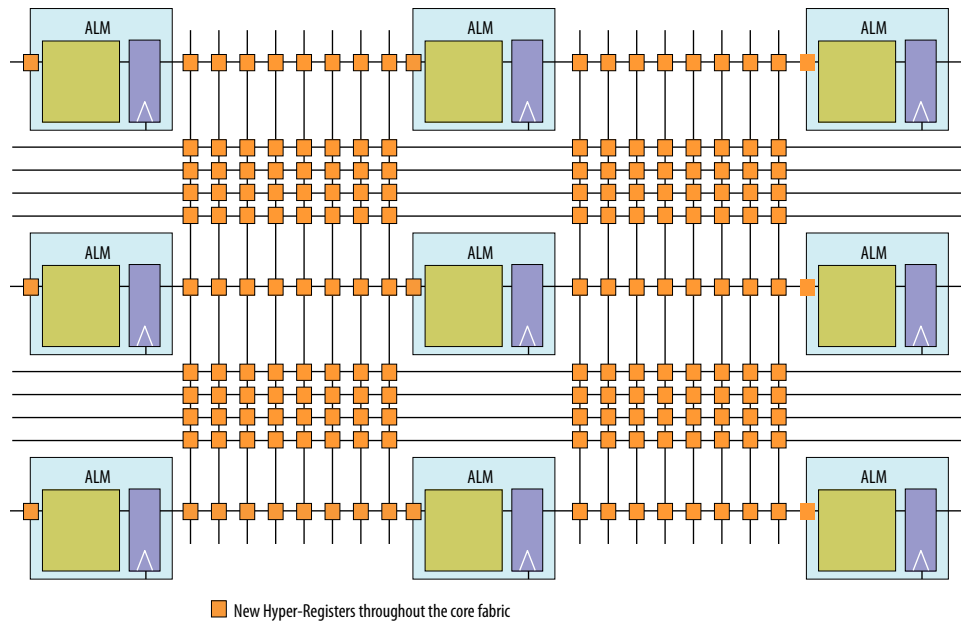


The Hyper-Registers enable the following key design techniques to achieve the 2X core performance increases:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

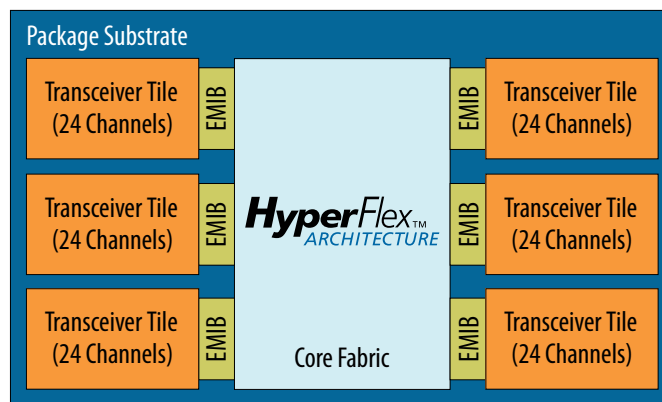
**Figure 4. HyperFlex Core Architecture**



## 1.7. Heterogeneous 3D SiP Transceiver Tiles

Intel Stratix 10 FPGAs and SoCs feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles, each containing 24 full-duplex transceiver channels. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

**Figure 5. Monolithic Core Fabric and Heterogeneous 3D SiP Transceiver Tiles**





Within each transceiver tile, the transceivers are arranged in four banks of six PMA-PCS groups. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

### 1.8.1. PMA Features

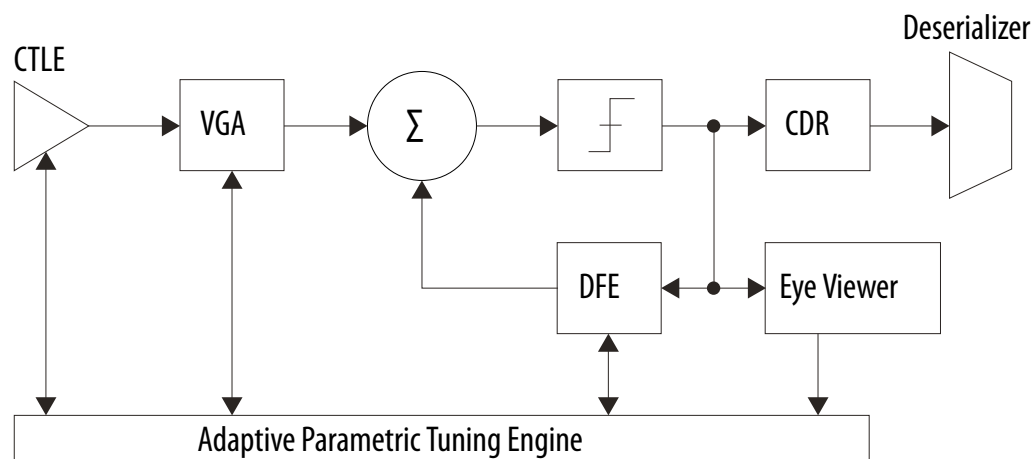
PMA channels are comprised of transmitter (TX), receiver (RX), and high speed clocking resources.

Intel Stratix 10 device features provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter LC tank-based (ATX) PLLs with optional fractional synthesis capability, channel PLLs operating as clock multiplier units (CMUs), and fractional synthesis PLLs (fPLLs).

- **ATX PLL**—can be configured in integer mode, or optionally, in a new fractional synthesis mode. Each ATX PLL spans the full frequency range of the supported data rate range providing a stable, flexible clock source with the lowest jitter.
- **CMU PLL**—when not being used as a transceiver, select PMA channels can be configured as channel PLLs operating as CMUs to provide an additional master clock source within the transceiver bank.
- **fPLL**—In addition, dedicated fPLLs are available with precision frequency synthesis capabilities. fPLLs can be used to synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators for multi-protocol and multi-rate applications.

On the receiver side, each PMA has an independent channel PLL that allows analog tracking for clock-data recovery. Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

- **Variable Gain Amplifier (VGA)**—to optimize the receiver's dynamic range
- **Continuous Time Linear Equalizer (CTLE)**—to compensate for channel losses with lowest power dissipation
- **Decision Feedback Equalizer (DFE)**—to provide additional equalization capability on backplanes even in the presence of crosstalk and reflections
- **On-Die Instrumentation (ODI)**—to provide on-chip eye monitoring capabilities (Eye Viewer). This capability helps to optimize link equalization parameters during board bring-up and supports in-system link diagnostics and equalization margin testing

**Figure 7. Intel Stratix 10 Receiver Block Features**

All link equalization parameters feature automatic adaptation using the new Advanced Digital Adaptive Parametric Tuning (ADAPT) circuit. This circuit is used to dynamically set DFE tap weights, adjust CTLE parameters, and optimize VGA gain and threshold voltage. Finally, optimal and consistent signal integrity is ensured by using the new hardened Precision Signal Integrity Calibration Engine (PreSICE) to automatically calibrate all transceiver circuit blocks on power-up. This gives the most link margin and ensures robust, reliable, and error-free operation.

**Table 8. Transceiver PMA Features**

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps <sup>(8)</sup> to 28.3 Gbps (Intel Stratix 10 GX/SX devices)
Backplane Support	Drive backplanes at data rates up to 28.3 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, QSFPDD, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	5-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	15 fixed tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Advanced Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and VGA blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
ATX Transmit PLLs	Low jitter ATX (inductor-capacitor) transmit PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols, with optional fractional frequency synthesis capability
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost

*continued...*

<sup>(8)</sup> Stratix 10 transceivers can support data rates below 1 Gbps with over sampling.

### 1.11. 10G Ethernet Hard IP

Intel Stratix 10 devices include IEEE 802.3 10-Gbps Ethernet (10GbE) compliant 10GBASE-R PCS and PMA hard IP. The scalable 10GbE hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks.

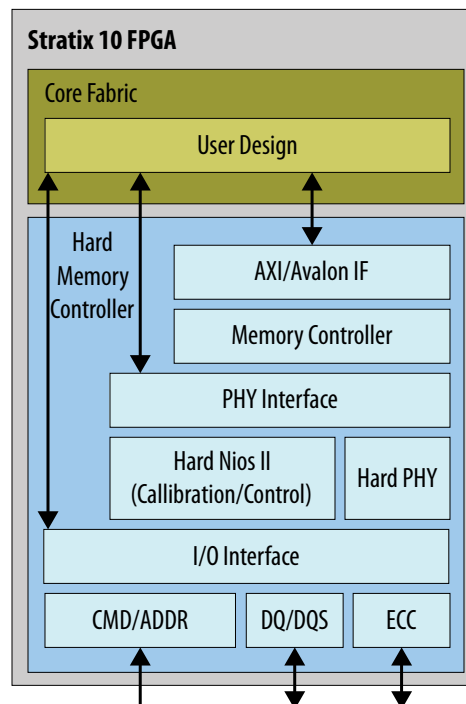
The integrated serial transceivers simplify multi-port 10GbE systems compared to 10 GbE Attachment Unit Interface (XAUI) interfaces that require an external XAUI-to-10G PHY. Furthermore, the integrated transceivers incorporate signal conditioning circuits, which enable direct connection to standard 10G XFP and SFP+ pluggable optical modules. The transceivers also support backplane Ethernet applications and include a hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) circuit that can be used for both 10G and 40G applications. The integrated 10G Ethernet hard IP and 10G transceivers save external PHY cost, board space and system power. The 10G Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

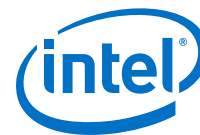
### 1.12. External Memory and General Purpose I/O

Intel Stratix 10 devices offer substantial external memory bandwidth, with up to ten 72-bit wide DDR4 memory interfaces running at up to 2666 Mbps.

This bandwidth is provided along with the ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. The external memory interfaces can be configured up to a maximum width of 144 bits when using either hard or soft memory controllers.

**Figure 8. Hard Memory Controller**





Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Stratix 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Stratix 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

**Table 10. External Memory Interface Performance**

The listed speeds are for the 1-rank case.

Interface	Controller Type	Performance
DDR4	Hard	2666 Mbps
DDR3	Hard	2133 Mbps
QDRII+	Soft	1,100 Mtps
QDRII+ Xtreme	Soft	1,266 Mtps
QDRIV	Soft	2,133 Mtps
RLDRAM III	Soft	2400 Mbps
RLDRAM II	Soft	533 Mbps

In addition to parallel memory interfaces, Intel Stratix 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Stratix 10 high-speed serial transceivers, which connect up to four HMC links, with each link running at data rates of 15 Gbps (HMC short reach specification).

Intel Stratix 10 devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces. LVDS rates up to 1.6 Gbps are supported, with each pair of pins having both a differential driver and a differential input buffer. This enables configurable direction for each LVDS pair.

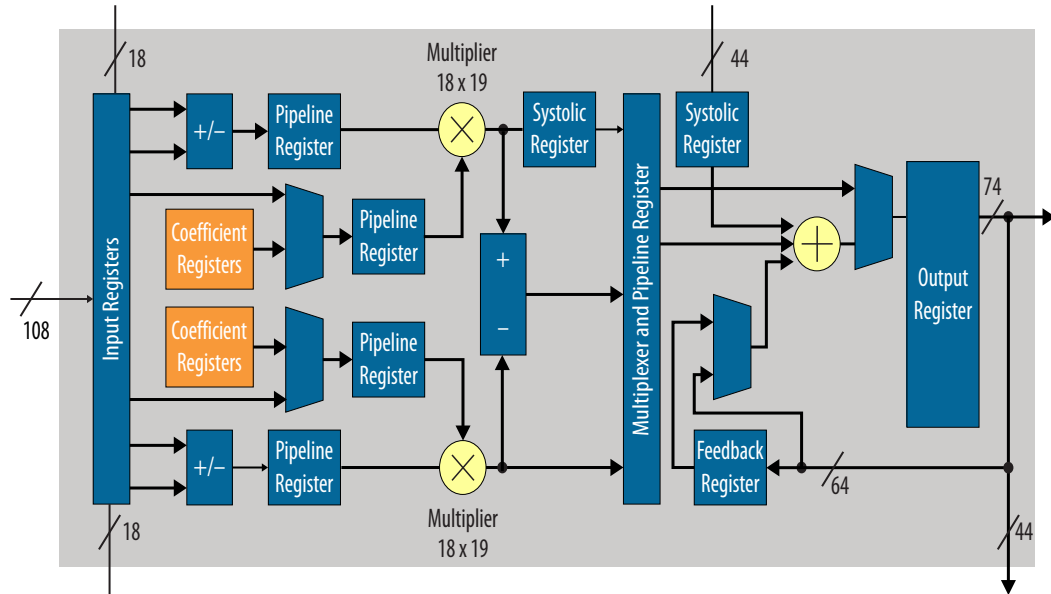
### 1.13. Adaptive Logic Module (ALM)

Intel Stratix 10 devices use a similar adaptive logic module (ALM) as the previous generation Arria 10 and Stratix V FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

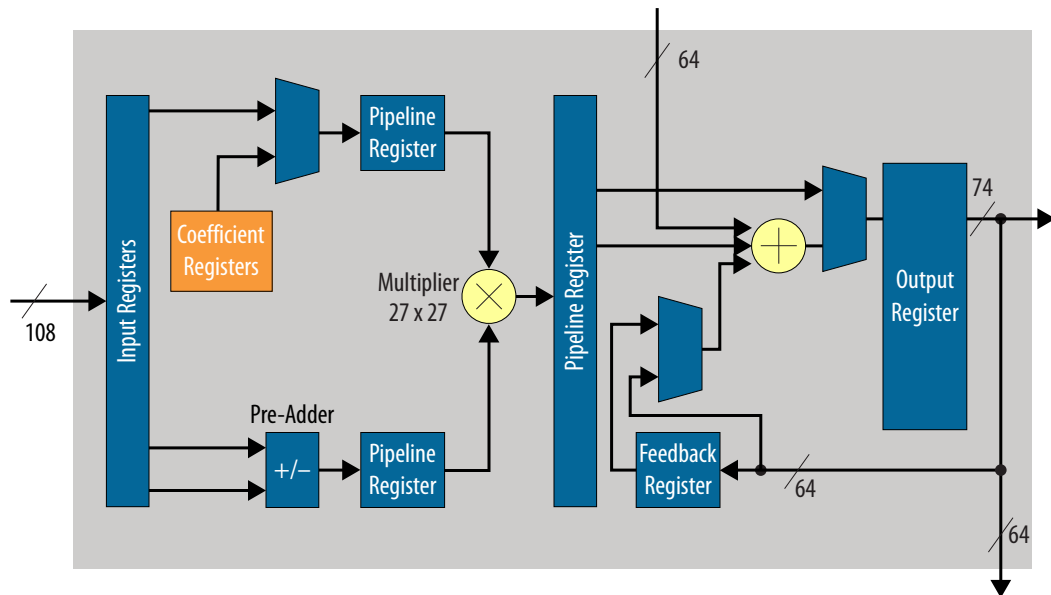
The ALM block diagram shown in the following figure has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

The DSP blocks can be configured to support signal processing with precision ranging from 18x19 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption.

**Figure 10. DSP Block: Standard Precision Fixed Point Mode**



**Figure 11. DSP Block: High Precision Fixed Point Mode**





Complex multiplication is very common in DSP algorithms. One of the most popular applications of complex multipliers is the FFT algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The Variable Precision DSP block supports the FFT algorithm with proportional increase in DSP resources as the precision grows.

**Table 13. Complex Multiplication With Variable Precision DSP Block**

Complex Multiplier Size	DSP Block Resources	FFT Usage
18x19 bits	2 Variable Precision DSP Blocks	Resource optimized FFT
27x27 bits	4 Variable Precision DSP Blocks	Highest precision FFT

For FFT applications with high dynamic range requirements, the Intel FFT IP Core offers an option of single precision floating point implementation with resource usage and performance similar to high precision fixed point implementations.

Other features of the DSP block include:

- Hard 18-bit and 25-bit pre-adders
- Hard floating point multipliers and adders
- 64-bit dual accumulator (for separate I, Q product accumulations)
- Cascaded output adder chains for 18- and 27-bit FIR filters
- Embedded coefficient registers for 18- and 27-bit coefficients
- Fully independent multiplier outputs
- Inferability using HDL templates supplied by the Intel Quartus Prime software for most modes

The Variable Precision DSP block is ideal to support the growing trend towards higher bit precision in high performance DSP applications. At the same time, it can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. With the Variable Precision DSP block architecture and hard floating point multipliers and adders, Intel Stratix 10 devices can efficiently support many different precision levels up to and including floating point implementations. This flexibility can result in increased system performance, reduced power consumption, and reduce architecture constraints on system algorithm designers.

## 1.18. Hard Processor System (HPS)

The Intel Stratix 10 SoC Hard Processor System (HPS) is Intel's industry leading third generation HPS. Leveraging the performance of Intel's 14-nm Tri-Gate technology, Intel Stratix 10 SoC devices more than double the performance of previous generation SoCs with an integrated quad-core 64-bit ARM Cortex-A53. The HPS also enables system-wide hardware virtualization capabilities by adding a system memory management unit. These architecture improvements ensure that Intel Stratix 10 SoCs will meet the requirements of current and future embedded markets, including wireless and wireline communications, data center acceleration, and numerous military applications.





Feature	Description
	<ul style="list-style-type: none"><li>• Superscalar, variable length, out-of-order pipeline with dynamic branch prediction</li><li>• Improved ARM NEON™ media processing engine</li><li>• Single- and double-precision floating-point unit</li><li>• CoreSight™ debug and trace technology</li></ul>
System Memory Management Unit	<ul style="list-style-type: none"><li>• Enables a unified memory model and extends hardware virtualization into peripherals implemented in the FPGA fabric</li></ul>
Cache Coherency unit	<ul style="list-style-type: none"><li>• Changes in shared data stored in cache are propagated throughout the system providing bi-directional coherency for co-processing elements.</li></ul>
Cache	<ul style="list-style-type: none"><li>• L1 Cache<ul style="list-style-type: none"><li>— 32 KB of instruction cache w/ parity check</li><li>— 32 KB of L1 data cache w /ECC</li><li>— Parity checking</li></ul></li><li>• L2 Cache<ul style="list-style-type: none"><li>— 1MB shared</li><li>— 8-way set associative</li><li>— SEU Protection with parity on TAG ram and ECC on data RAM</li><li>— Cache lockdown support</li></ul></li></ul>
On-Chip Memory	<ul style="list-style-type: none"><li>• 256 KB of scratch on-chip RAM</li></ul>
External SDRAM and Flash Memory Interfaces for HPS	<ul style="list-style-type: none"><li>• Hard memory controller with support for DDR4, DDR3, LPDDR3<ul style="list-style-type: none"><li>— 40-bit (32-bit + 8-bit ECC) with select packages supporting 72-bit (64-bit + 8-bit ECC)</li><li>— Support for up to 2666 Mbps DDR4 and 2166 Mbps DDR3 frequencies</li><li>— Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters</li><li>— Software Configurable Priority Scheduling on individual SDRAM bursts</li><li>— Fully programmable timing parameter support for all JEDEC-specified timing parameters</li><li>— Multiport front-end (MPFE) scheduler interface to the hard memory controller, which supports the AXI® Quality of Service (QoS) for interface to the FPGA fabric</li></ul></li><li>• NAND flash controller<ul style="list-style-type: none"><li>— ONFI 1.0</li><li>— Integrated descriptor based with DMA</li><li>— Programmable hardware ECC support</li><li>— Support for 8- and 16-bit Flash devices</li></ul></li><li>• Secure Digital SD/SDIO/MMC controller<ul style="list-style-type: none"><li>— eMMC 4.5</li><li>— Integrated descriptor based DMA</li><li>— CE-ATA digital commands supported</li><li>— 50 MHz operating frequency</li></ul></li><li>• Direct memory access (DMA) controller<ul style="list-style-type: none"><li>— 8-channel</li><li>— Supports up to 32 peripheral handshake interface</li></ul></li></ul>
continued...	



Feature	Description
Communication Interface Controllers	<ul style="list-style-type: none"> <li>Three 10/100/1000 Ethernet media access controls (MAC) with integrated DMA               <ul style="list-style-type: none"> <li>Supports RGMII and RMII external PHY Interfaces</li> <li>Option to support other PHY interfaces through FPGA logic                   <ul style="list-style-type: none"> <li>GMII</li> <li>MII</li> <li>RMII (requires MII to RMII adapter)</li> <li>RGMII (requires GMII to RGMII adapter)</li> <li>SGMII (requires GMII to SGMII adapter)</li> </ul> </li> <li>Supports IEEE 1588-2002 and IEEE 1588-2008 standards for precision networked clock synchronization</li> <li>Supports IEEE 802.1Q VLAN tag detection for reception frames</li> <li>Supports Ethernet AVB standard</li> </ul> </li> <li>Two USB On-the-Go (OTG) controllers with DMA               <ul style="list-style-type: none"> <li>Dual-Role Device (device and host functions)                   <ul style="list-style-type: none"> <li>High-speed (480 Mbps)</li> <li>Full-speed (12 Mbps)</li> <li>Low-speed (1.5 Mbps)</li> <li>Supports USB 1.1 (full-speed and low-speed)</li> </ul> </li> <li>Integrated descriptor-based scatter-gather DMA</li> <li>Support for external ULPI PHY</li> <li>Up to 16 bidirectional endpoints, including control endpoint</li> <li>Up to 16 host channels</li> <li>Supports generic root hub</li> <li>Configurable to OTG 1.3 and OTG 2.0 modes</li> </ul> </li> <li>Five I<sup>2</sup>C controllers (three can be used by EMAC for MIO to external PHY)               <ul style="list-style-type: none"> <li>Support both 100Kbps and 400Kbps modes</li> <li>Support both 7-bit and 10-bit addressing modes</li> <li>Support Master and Slave operating mode</li> </ul> </li> <li>Two UART 16550 compatible               <ul style="list-style-type: none"> <li>Programmable baud rate up to 115.2Kbaud</li> </ul> </li> <li>Four serial peripheral interfaces (SPI) (2 Master, 2 Slaves)               <ul style="list-style-type: none"> <li>Full and Half duplex</li> </ul> </li> </ul>
Timers and I/O	<ul style="list-style-type: none"> <li>Timers               <ul style="list-style-type: none"> <li>4 general-purpose timers</li> <li>4 watchdog timers</li> </ul> </li> <li>48 HPS direct I/O allow HPS peripherals to connect directly to I/O</li> <li>Up to three IO48 banks may be assigned to HPS for HPS DDR access</li> </ul>
Interconnect to Logic Core	<ul style="list-style-type: none"> <li>FPGA-to-HPS Bridge               <ul style="list-style-type: none"> <li>Allows IP bus masters in the FPGA fabric to access to HPS bus slaves</li> <li>Configurable 32-, 64-, or 128-bit AMBA AXI interface</li> </ul> </li> <li>HPS-to-FPGA Bridge               <ul style="list-style-type: none"> <li>Allows HPS bus masters to access bus slaves in FPGA fabric</li> <li>Configurable 32-, 64-, or 128-bit AMBA AXI interface allows high-bandwidth HPS master transactions to FPGA fabric</li> </ul> </li> <li>HPS-to-SDM and SDM-to-HPS Bridges               <ul style="list-style-type: none"> <li>Allows the HPS to reach the SDM block and the SDM to bootstrap the HPS</li> </ul> </li> <li>Light Weight HPS-to-FPGA Bridge               <ul style="list-style-type: none"> <li>Light weight 32-bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in FPGA fabric</li> </ul> </li> <li>FPGA-to-HPS SDRAM Bridge               <ul style="list-style-type: none"> <li>Up to three AMBA AXI interfaces supporting 32, 64, or 128-bit data paths</li> </ul> </li> </ul>



## 1.19. Power Management

Intel Stratix 10 devices leverage the advanced Intel 14-nm Tri-Gate process technology, the all new HyperFlex core architecture to enable Hyper-Folding, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 70% compared to previous generation high-performance Stratix V devices.

Intel Stratix 10 standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Stratix 10 device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; it is not an option. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications.

With the new HyperFlex core architecture, designs can run 2X faster than previous generation FPGAs. With 2X performance and same required throughput, architects can cut the data path width in half to save power. This optimization is called Hyper-Folding. Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks, at configuration time.

The optional power reduction techniques in Intel Stratix 10 devices include:

- **Available Low Static Power Devices**—Intel Stratix 10 devices are available with a fixed core voltage that provides lower static power than the SmartVID standard power devices, while maintaining device performance

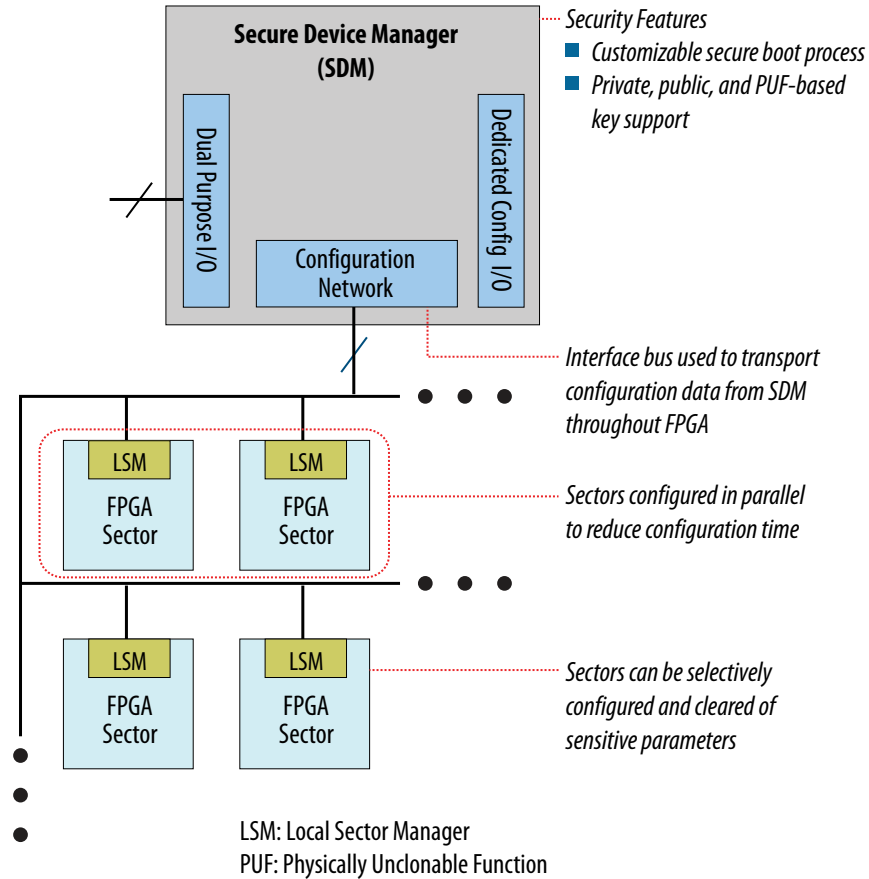
Furthermore, Intel Stratix 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

## 1.20. Device Configuration and Secure Device Manager (SDM)

All Intel Stratix 10 devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.



Figure 14. SDM Block Diagram



During configuration, Intel Stratix 10 devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.



Document Version	Changes
	<ul style="list-style-type: none"> <li>• Changed the features listed in the "Key Features of Stratix 10 Devices Compared to Stratix V Devices" table.</li> <li>• Changed the descriptions of the following areas of the "Stratix 10 FPGA and SoC Common Device Features" table: <ul style="list-style-type: none"> <li>— Transceiver hard IP</li> <li>— Internal memory blocks</li> <li>— Core clock networks</li> <li>— Packaging</li> </ul> </li> <li>• Reorganized and updated all tables in the "Stratix 10 FPGA and SoC Family Plan" section.</li> <li>• Removed the "Migration Between Arria 10 FPGAs and Stratix 10 FPGAs" section.</li> <li>• Removed footnotes from the "Transceiver PCS Features" table.</li> <li>• Changed the HMC description in the "External Memory and General Purpose I/O" section.</li> <li>• Changed the number of fPLLs in the "Fractional Synthesis PLLs and I/O PLLs" section.</li> <li>• Clarified HMC data width support in the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description in the "Internal Embedded Memory" section.</li> <li>• Changed the datarate for the Standard PCS and SDI PCS features in the "Transceiver PCS Features" table.</li> <li>• Added a note to the "PCI Express Gen1/Gen2/Gen3 Hard IP" section.</li> <li>• Updated the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description for the Cache coherency unit in the "Key Features of the Stratix 10 HPS" table.</li> <li>• Changed the description for the external SDRAM and Flash memory interfaces for HPS in the "Key Features of the Stratix 10 HPS" table.</li> </ul>
2015.12.04	Initial release.