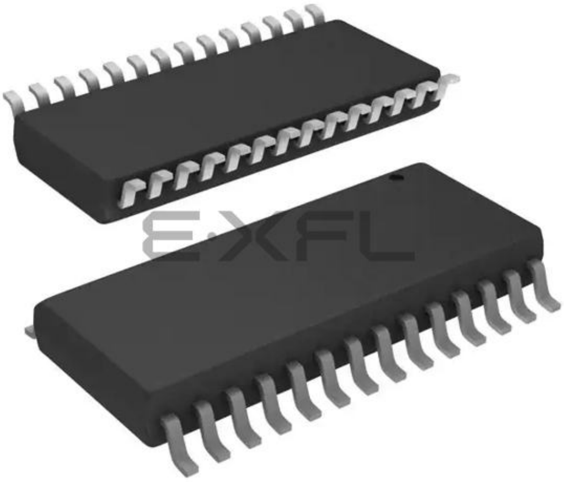
Microchip Technology - PIC16F72T-E/SO Datasheet



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Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f72t-e-so

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1.0 DEVICE OVERVIEW

This document contains device specific information for the operation of the PIC16F72 device. Additional information may be found in the PIC™ Mid-Range MCU Reference Manual (DS33023), which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F72 belongs to the Mid-Range family of the PIC devices. A block diagram of the device is shown in Figure 1-1.

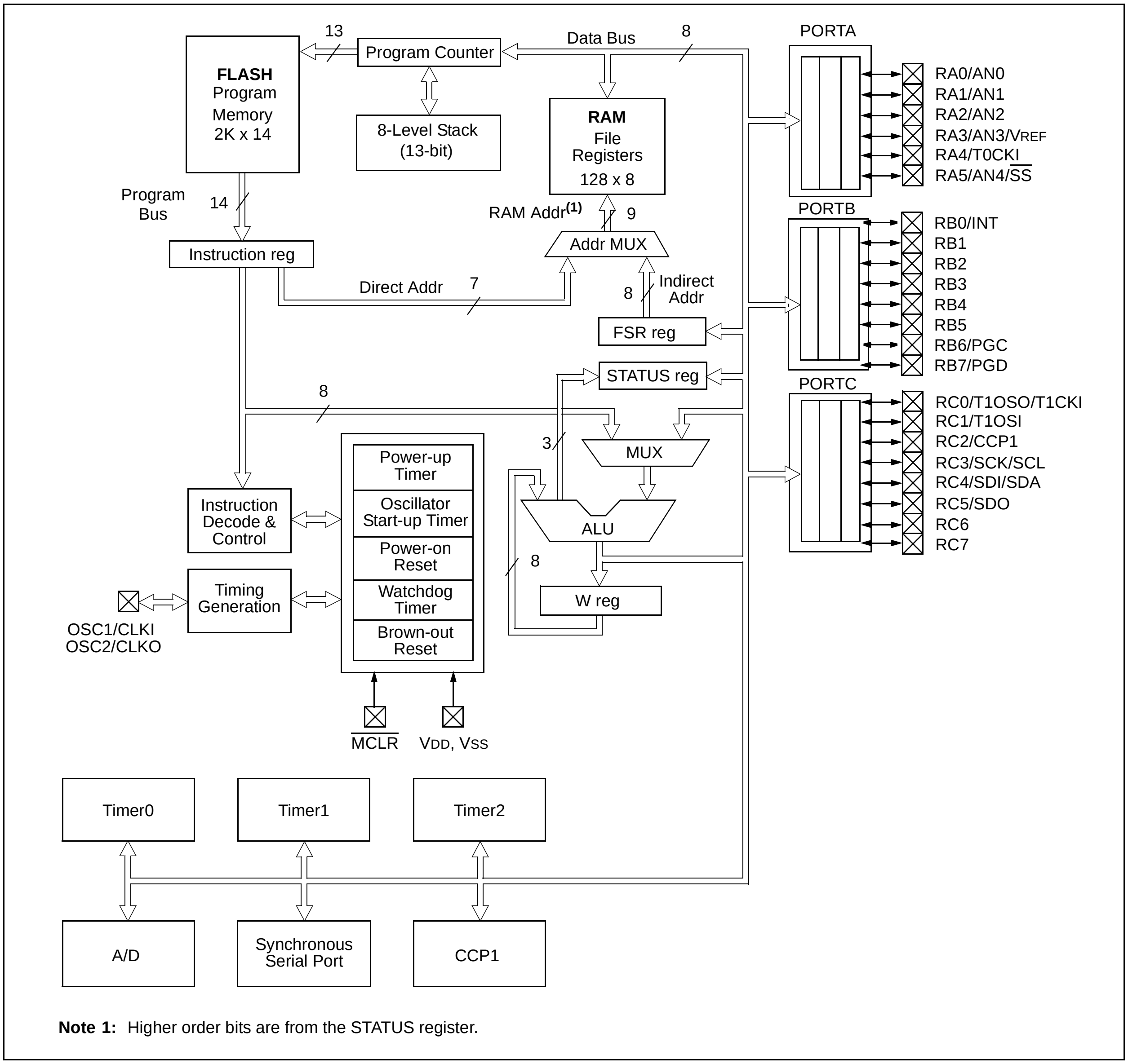
The program memory contains 2K words, which translate to 2048 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 128 bytes.

There are 22 I/O pins that are user configurable on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input
- Timer1 clock/oscillator
- Capture/Compare/PWM
- A/D converter
- SPI/I^{2}C

Table 1-1 details the pinout of the device with descriptions and details for each pin.

FIGURE 1-1: PIC16F72 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see Section 12.0, Instruction Set Summary.

Note 1: The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h - 1FFh)
`0` = Bank 0, 1 (00h - FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4 **$\overline{\text{TO}}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions)(1)
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

bit 0 **C:** Carry/$\overline{\text{borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions)(1,2)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

2: For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.5 PIR1 Register

This register contains the individual flag bits for the Peripheral interrupts.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT FLAG REGISTER 1 (ADDRESS 0Ch)

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **ADIF:** A/D Converter Interrupt Flag bit
`1` = An A/D conversion completed
`0` = The A/D conversion is not complete

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3 **SSPIF:** Synchronous Serial Port (SSP) Interrupt Flag bit
`1` = The SSP interrupt condition has occurred, and must be cleared in software before returning from the Interrupt Service Routine.
The conditions that will set this bit are a transmission/reception has taken place.
`0` = No SSP interrupt condition has occurred

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
<u>Capture mode:</u>
`1` = A TMR1 register capture occurred (must be cleared in software)
`0` = No TMR1 register capture occurred
<u>Compare mode:</u>
`1` = A TMR1 register compare match occurred (must be cleared in software)
`0` = No TMR1 register compare match occurred
<u>PWM mode:</u>
Unused in this mode

bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
`1` = TMR2 to PR2 match occurred (must be cleared in software)
`0` = No TMR2 to PR2 match occurred

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
`1` = TMR1 register overflowed (must be cleared in software)
`0` = TMR1 register did not overflow

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

3.2 PORTB and the TRISB Register

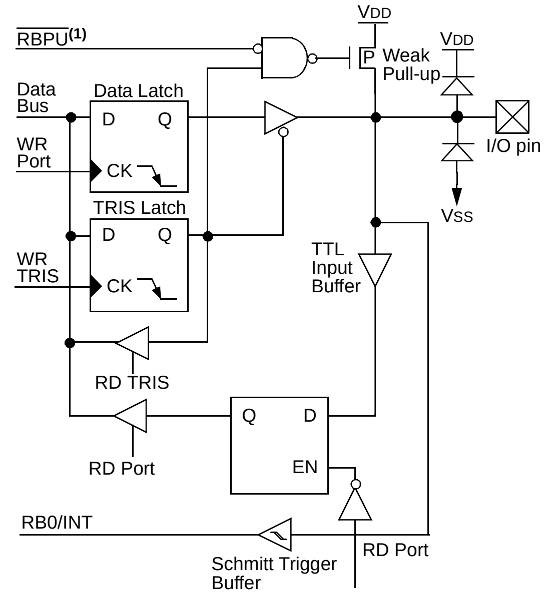
PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

EXAMPLE 3-2: INITIALIZING PORTB

```
BANKSEL  PORTB    ; Select bank for PORTB
CLRF     PORTB    ; Initialize PORTB by
                  ; clearing output
                  ; data latches
BANKSEL  TRISB    ; Select Bank for TRISB
MOVLW    0xCF     ; Value used to
                  ; initialize data
                  ; direction
MOVWF    TRISB    ; Set RB<3:0> as inputs
                  ; RB<5:4> as outputs
                  ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 3-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION<7>).

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'd together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

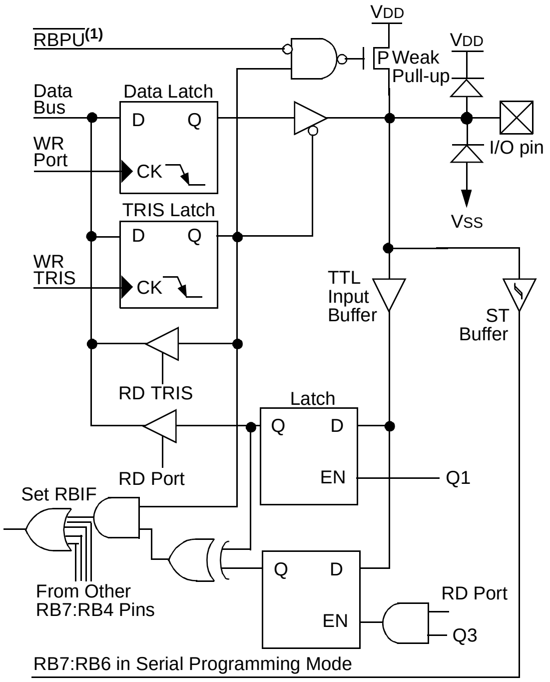
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

This interrupt-on-mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression. Refer to the Embedded Control Handbook, *"Implementing Wake-Up on Key Stroke"* (AN552).

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION<6>).

FIGURE 3-4: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION<7>).

5.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow, that will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 5.5.1).

In Asynchronous Counter mode, Timer1 cannot be used as a time base for capture or compare operations.

5.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register. Data in the Timer1 register (TMR1) may become corrupted. Corruption occurs when the timer enable is turned off at the same instant that a ripple carry occurs in the timer module.

Reading the 16-bit value requires some care. Examples 12-2 and 12-3 in the PIC™ Mid-Range MCU Family Reference Manual (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

5.6 Timer1 Oscillator

A crystal oscillator circuit is built between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 5-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

TABLE 5-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz	33 pF	33 pF
	100 kHz	15 pF	15 pF
	200 kHz	15 pF	15 pF
These values are for design guidance only.			

Note 1: Higher capacitance increases the stability of oscillator, but also increases the start-up time.

2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

5.7 Timer1 Interrupt

The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

5.8 Resetting Timer1 Using a CCP Trigger Output

If the CCP module is configured in Compare mode to generate a “special event trigger" signal (CCP1M3:CCP1M0 = `1011`), the signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Note: The special event triggers from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this RESET operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer1.

REGISTER 6-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6-3 **TOUTPS3:TOUTPS0:** Timer2 Output Postscale Select bits

`0000` = 1:1 Postscale
`0001` = 1:2 Postscale
`0010` = 1:3 Postscale
•
•
•
`1111` = 1:16 Postscale

bit 2 **TMR2ON:** Timer2 On bit

`1` = Timer2 is on
`0` = Timer2 is off

bit 1-0 **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits

`00` = Prescaler is 1
`01` = Prescaler is 4
`1x` = Prescaler is 16

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
- n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	`0000 000x`	`0000 000u`
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	`-0-- 0000`	`0000 0000`
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	`-0-- 0000`	`0000 0000`
11h	TMR2	Timer2 Module Register								`0000 0000`	`0000 0000`
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	`-000 0000`	`-000 0000`
92h	PR2	Timer2 Period Register								`1111 1111`	`1111 1111`

Legend: `x` = unknown, `u` = unchanged, `-` = unimplemented, read as ‘0’. Shaded cells are not used by the Timer2 module.

7.3 Reading the FLASH Program Memory

To read a program memory location, the user must write two bytes of the address to the PMADRL and PMADRH registers and then set control bit, RD (PMCON1<0>). Once the read control bit is set, the program memory FLASH controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the "`BSF PMCON1,RD`" instruction to be ignored. The data is available in the very next cycle in the PMDATL and PMDATH registers; therefore, it can be read as two bytes in the following instructions. PMDATL and PMDATH registers will hold this value until another read, or until it is written to by the user (during a write operation).

7.4 Operation During Code Protect

The FLASH program memory control can read anywhere within the program memory, whether or not the program memory is code protected.

This does not compromise the code, because there is no way to rewrite a portion of the program memory, or leave contents of a program memory read in a register while changing modes.

EXAMPLE 7-1: FLASH PROGRAM READ

```
BANKSEL PMADRH          ; Select Bank for PMADRH
MOVLW   MS_PROG_EE_ADDR ;
MOVWF   PMADRH          ; MS Byte of Program Address to read
MOVLW   LS_PROG_EE_ADDR ;
MOVWF   PMADRL          ; LS Byte of Program Address to read
BANKSEL PMCON1          ; Select Bank for PMCON1
BSF     PMCON1, RD      ; EE Read
                        ;
NOP                     ; Any instructions here are ignored as program
NOP                     ; memory is read in second cycle after BSF PMCON1,RD
                        ;
                        ; First instruction after BSF PMCON1,RD executes normally
BANKSEL PMDATL          ; Select Bank for PMDATL
MOVF    PMDATL, W       ; W = LS Byte of Program PMDATL
MOVF    PMDATH, W       ; W = MS Byte of Program PMDATL
```

TABLE 7-1: REGISTERS ASSOCIATED WITH PROGRAM FLASH

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
10Dh	PMADRL	Address Register Low Byte								`xxxx xxxx`	`uuuu uuuu`
10Fh	PMADRH	—	—	—	Address Register High Byte					`xxxx xxxx`	`uuuu uuuu`
10Ch	PMDATL	Data Register Low Byte								`xxxx xxxx`	`uuuu uuuu`
10Eh	PMDATH	—	—	Data Register High Byte						`xxxx xxxx`	`uuuu uuuu`
18Ch	PMCON1	—(1)	—	—	—	—	—	—	RD	`1--- ---0`	`1--- ---0`

Legend: `x` = unknown, `u` = unchanged, r = reserved, `-` = unimplemented, read as '0'.
Shaded cells are not used during FLASH access.

Note 1: This bit always reads as a '1'.

Maximum PWM resolution (bits) for a given PWM frequency is calculated using Equation 8-3.

EQUATION 8-3: PWM MAX RESOLUTION

$$\text{PWM Maximum Resolution} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

For a sample PWM period and duty cycle calculation, see the PIC™ Mid-Range MCU Reference Manual (DS33023).

8.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 8-4: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	`0000 000x`	`0000 000u`
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	`-0-- 0000`	`0000 0000`
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	`-0-- 0000`	`0000 0000`
87h	TRISC	PORTC Data Direction Register								`1111 1111`	`1111 1111`
11h	TMR2	Timer2 Module Register								`0000 0000`	`0000 0000`
92h	PR2	Timer2 Module Period Register								`1111 1111`	`1111 1111`
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	`-000 0000`	`-000 0000`
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								`xxxx xxxx`	`uuuu uuuu`
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								`xxxx xxxx`	`uuuu uuuu`
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	`--00 0000`	`--00 0000`

Legend: `x` = unknown, `u` = unchanged, `-` = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.

FIGURE 9-2: SPI MODE TIMING, MASTER MODE

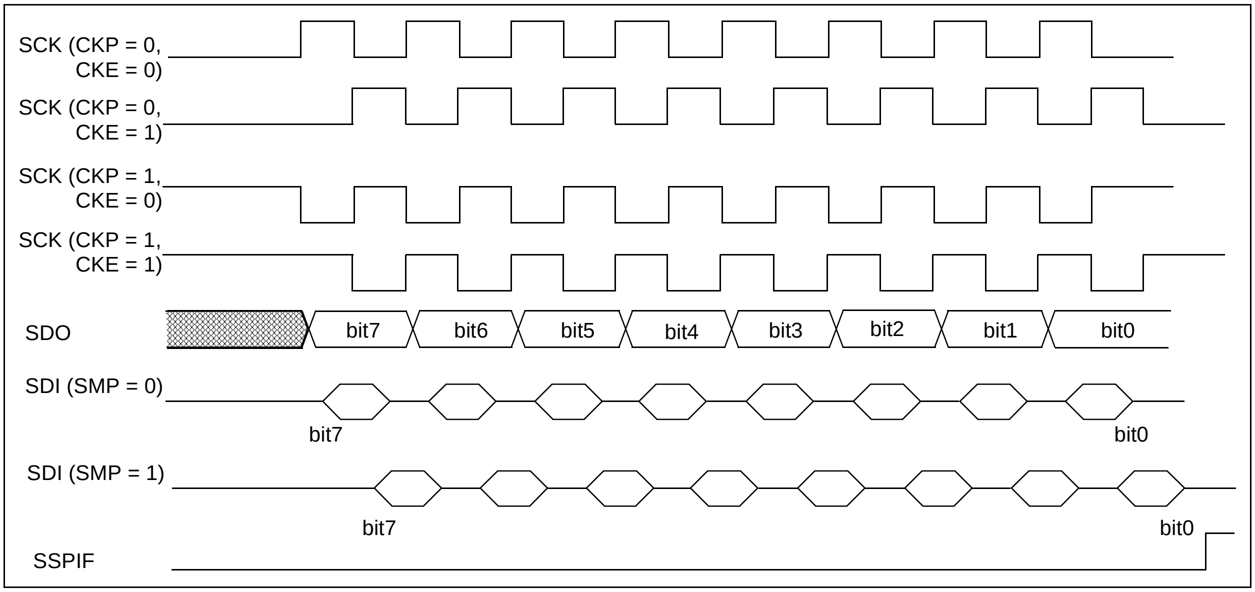


FIGURE 9-3: SPI MODE TIMING (SLAVE MODE WITH CKE = 0)

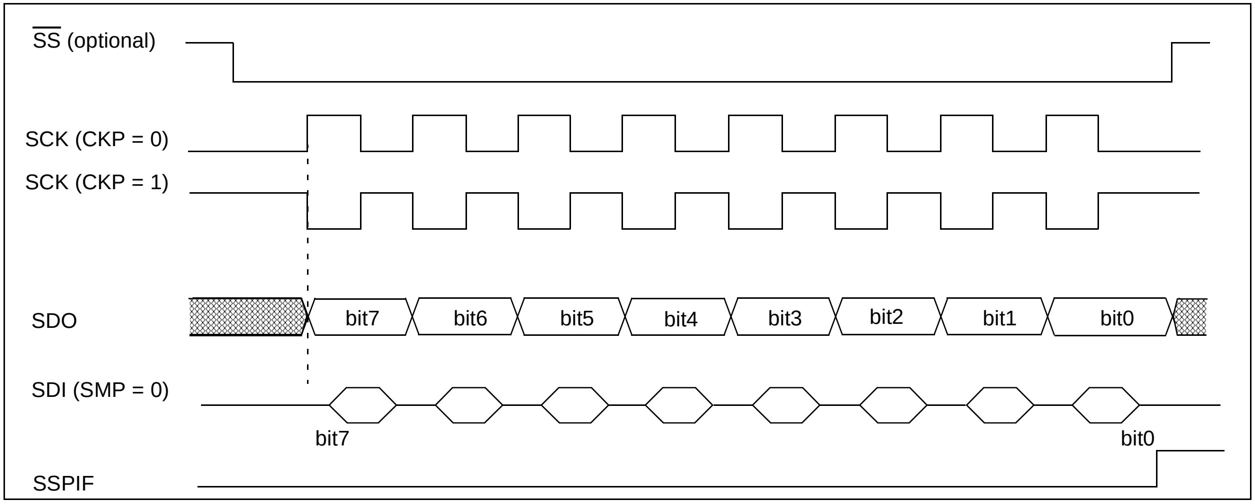
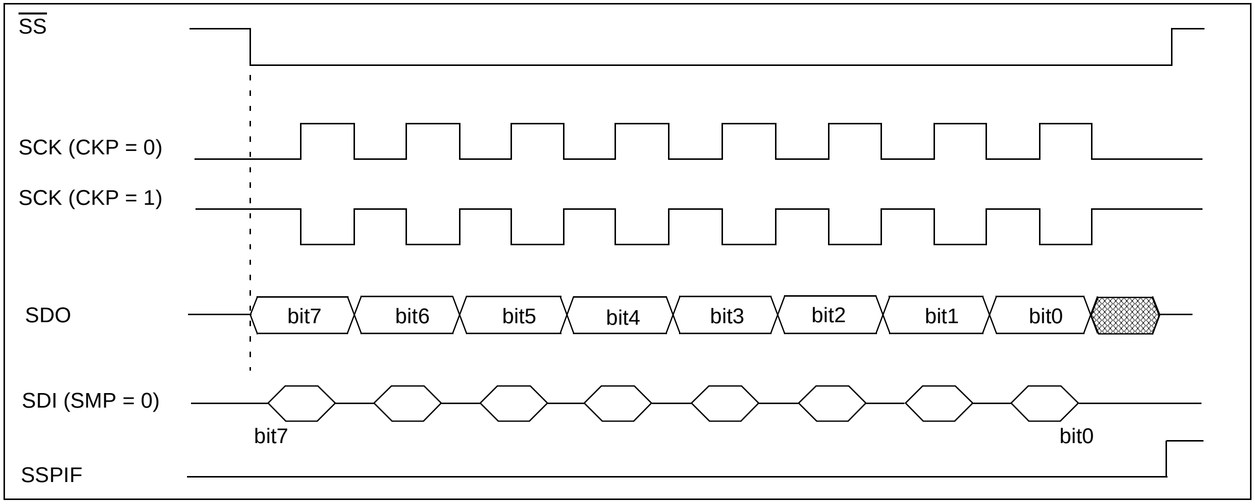


FIGURE 9-4: SPI MODE TIMING (SLAVE MODE WITH CKE = 1)



11.13 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator that does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKI pin. That means that the WDT will run, even if the clock on the OSC1/CLKI and OSC2/CLKO pins of the device has been stopped, for example, by execution of a `SLEEP` instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

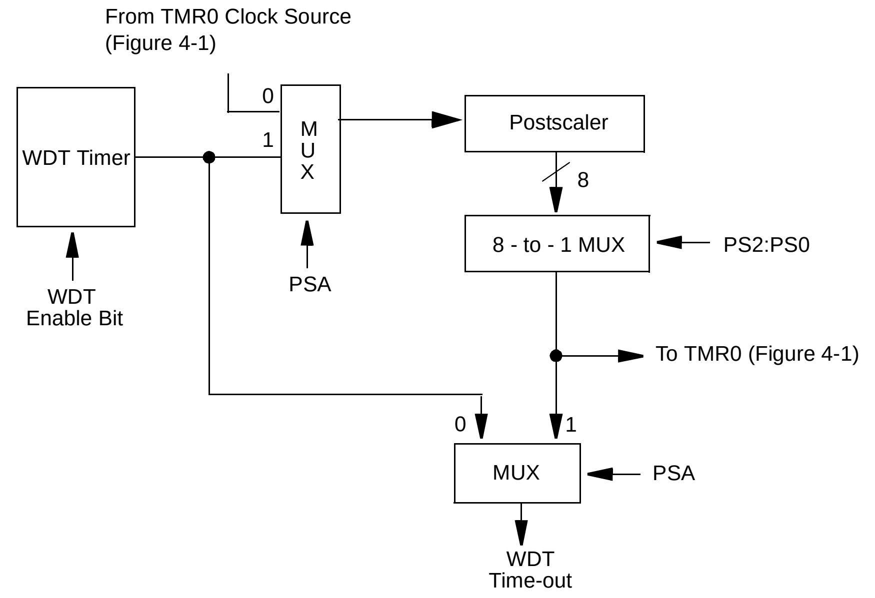
The WDT can be permanently disabled by clearing configuration bit WDTEN (see Section 11.1).

WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION register.

Note 1: The `CLRWDT` and `SLEEP` instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

2: When a `CLRWDT` instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 11-11: WATCHDOG TIMER BLOCK DIAGRAM



Note: PSA and PS2:PS0 are bits in the OPTION register.

TABLE 11-7: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	**(1)**	BOREN[(1)]	—	CP	$\overline{\text{PWRTEN}}$[(1)]	WDTEN	FOSC1	FOSC0
81h,181h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 11-1 for operation of these bits.

14.1 DC Characteristics: PIC16F72 (Industrial, Extended) PIC16LF72 (Industrial)

<table>
<tr><td colspan="3">PIC16LF72
(Industrial)</td><td colspan="5">Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial</td></tr>
<tr><td colspan="3">PIC16F72
(Industrial, Extended)</td><td colspan="5">Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial
-40°C ≤ TA ≤ +125°C for extended</td></tr>
<tr><th>Param No.</th><th>Sym</th><th>Characteristic</th><th>Min</th><th>Typ†</th><th>Max</th><th>Units</th><th>Conditions</th></tr>
<tr><td rowspan="2">D001</td><td rowspan="2">VDD</td><td colspan="6">Supply Voltage</td></tr>
<tr><td>PIC16LF72</td><td>2.0
2.5
2.2</td><td>—
—
—</td><td>5.5
5.5
5.5</td><td>V
V
V</td><td>A/D not used, -40°C to +85°C
A/D in use, -40°C to +85°C
A/D in use, 0°C to +85°C</td></tr>
<tr><td>D001
D001A</td><td></td><td>PIC16F72</td><td>4.0
VBOR*</td><td>—
—</td><td>5.5
5.5</td><td>V
V</td><td>All configurations
BOR enabled (Note 7)</td></tr>
<tr><td>D002*</td><td>VDR</td><td>RAM Data Retention Voltage (Note 1)</td><td>—</td><td>1.5</td><td>—</td><td>V</td><td></td></tr>
<tr><td>D003</td><td>VPOR</td><td>VDD Start Voltage to ensure internal Power-on Reset signal</td><td>—</td><td>VSS</td><td>—</td><td>V</td><td>See section on Power-on Reset for details</td></tr>
<tr><td>D004*</td><td>SVDD</td><td>VDD Rise Rate to ensure internal Power-on Reset signal</td><td>0.05</td><td>—</td><td>—</td><td>V/ms</td><td>See section on Power-on Reset for details</td></tr>
<tr><td>D005</td><td>VBOR</td><td>Brown-out Reset Voltage</td><td>3.65</td><td>4.0</td><td>4.35</td><td>V</td><td>BOREN bit in configuration word enabled</td></tr>
</table>

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements in active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

14.1 DC Characteristics: PIC16F72 (Industrial, Extended) PIC16LF72 (Industrial) (Continued)

PIC16LF72 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC16F72 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	IDD	**Supply Current (Notes 2, 5)**					
D010		PIC16LF72	—	0.4	2.0	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V **(Note 4)**
D010A			—	25	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D010		PIC16F72	-	0.9	4	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V **(Note 4)**
D013			—	5.2	15	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D015*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	25	200	µA	BOR enabled, VDD = 5.0V
	IPD	**Power-down Current (Notes 3, 5)**					
D020		PIC16LF72	—	2.0	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			—	0.1	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D020		PIC16F72	—	5.0	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021				0.1	19	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D023*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	25	200	µA	BOR enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements in active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

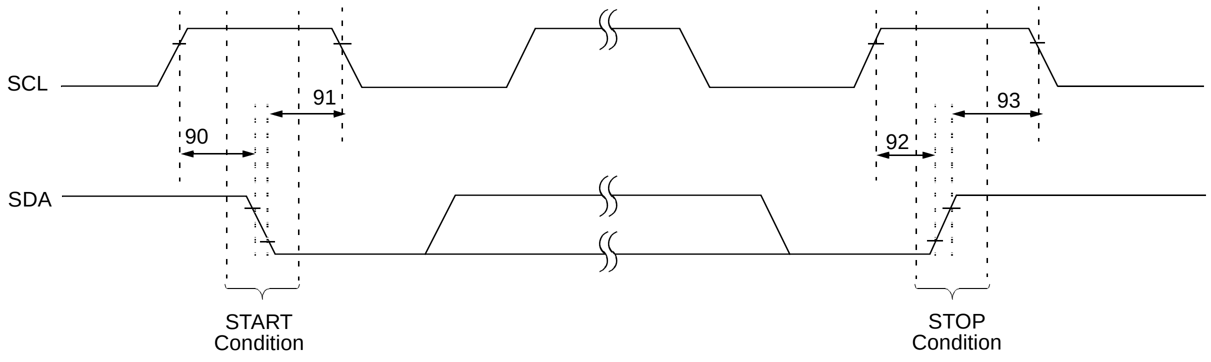
TABLE 14-6: SPI MODE REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input		TCY	—	—	ns	
71*	TscH	SCK input high time (Slave mode)		TCY + 20	—	—	ns	
72*	TscL	SCK input low time (Slave mode)		TCY + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75*	TdoR	SDO data output rise time	Standard(**F**) Extended(**LF**)	— —	10 25	25 50	ns ns	
76*	TdoF	SDO data output fall time		—	10	25	ns	
77*	TssH2doZ	$\overline{SS}$↑ to SDO output hi-impedance		10	—	50	ns	
78*	TscR	SCK output rise time (Master mode)	Standard(**F**) Extended(**LF**)	— —	10 25	25 50	ns ns	
79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	Standard(**F**) Extended(**LF**)	— —	— —	50 145	ns ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		TCY	—	—	ns	
82*	TssL2doV	SDO data output valid after $\overline{SS}$↓ edge		—	—	50	ns	
83*	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge		1.5 TCY + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-14: I²C BUS START/STOP BITS TIMING



Note: Refer to Figure 14-3 for load conditions.

FIGURE 15-13: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD vs. VDD (-40°C TO +125°C)

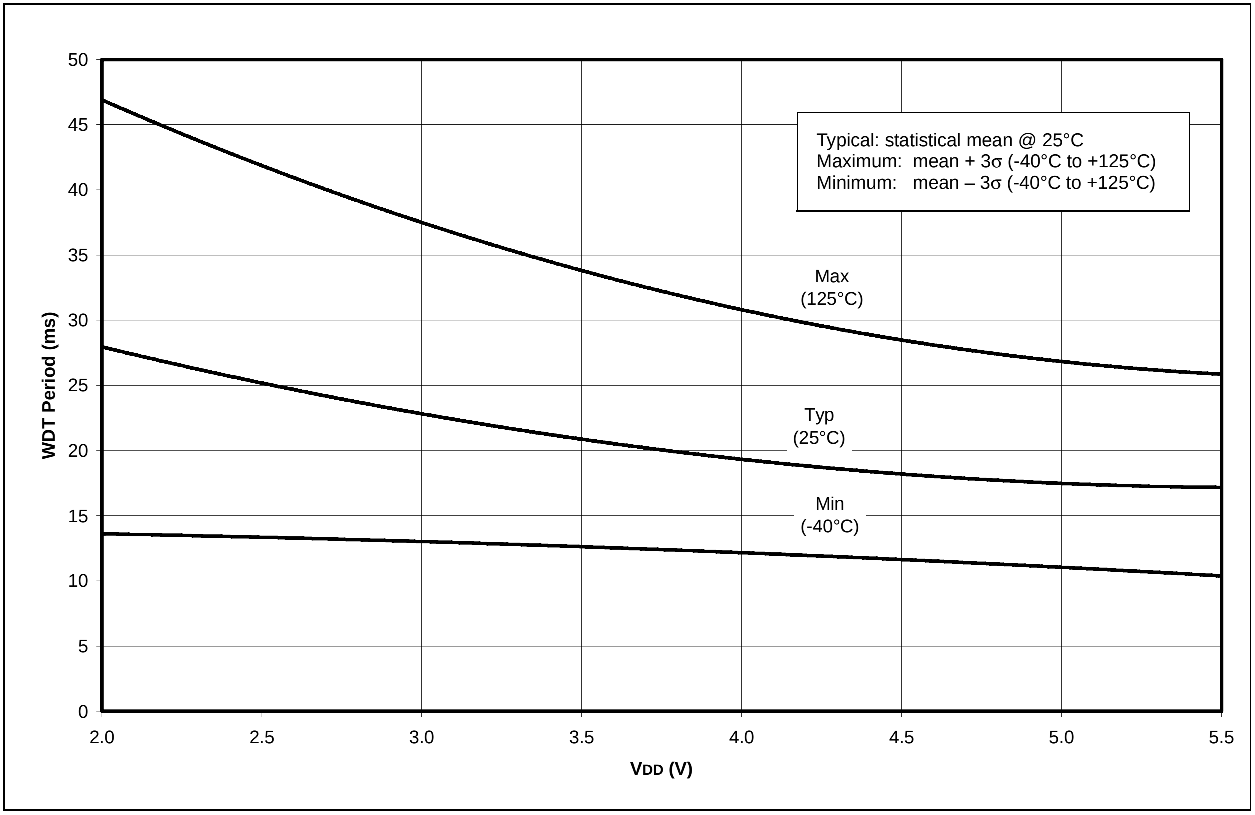
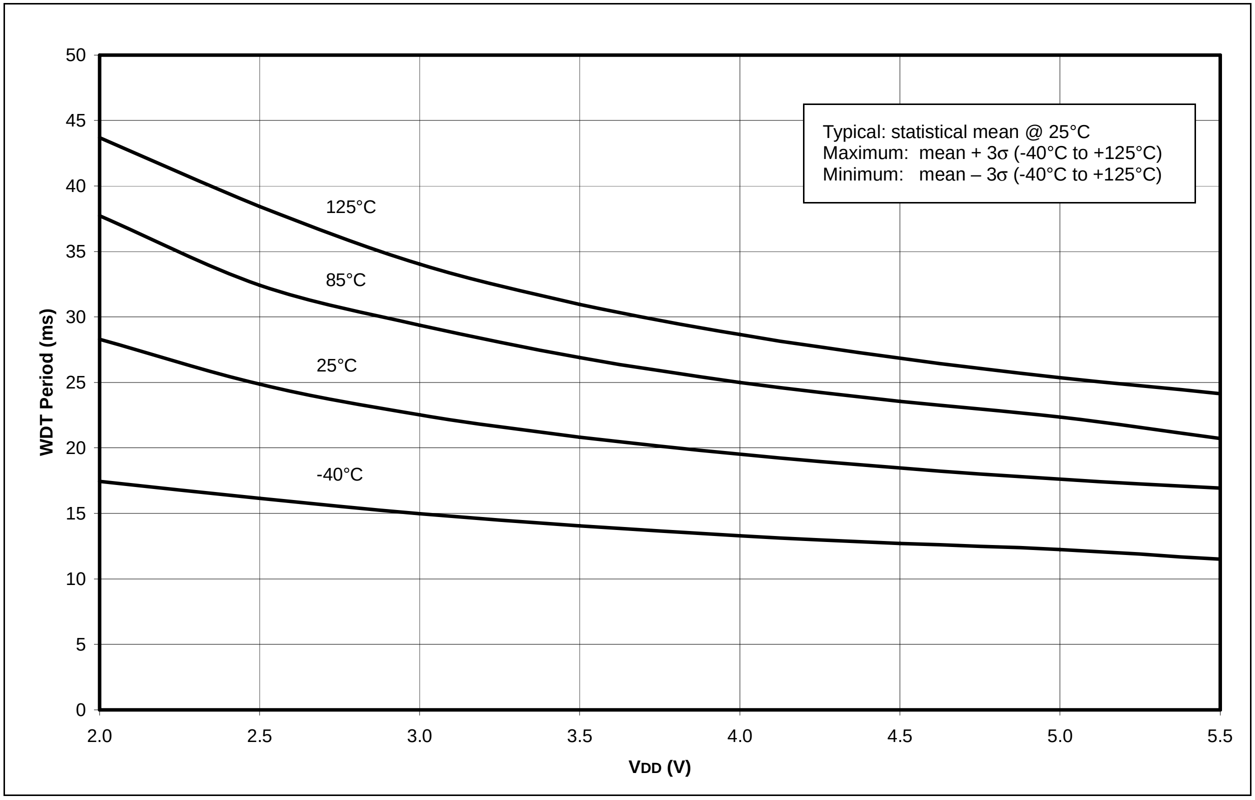
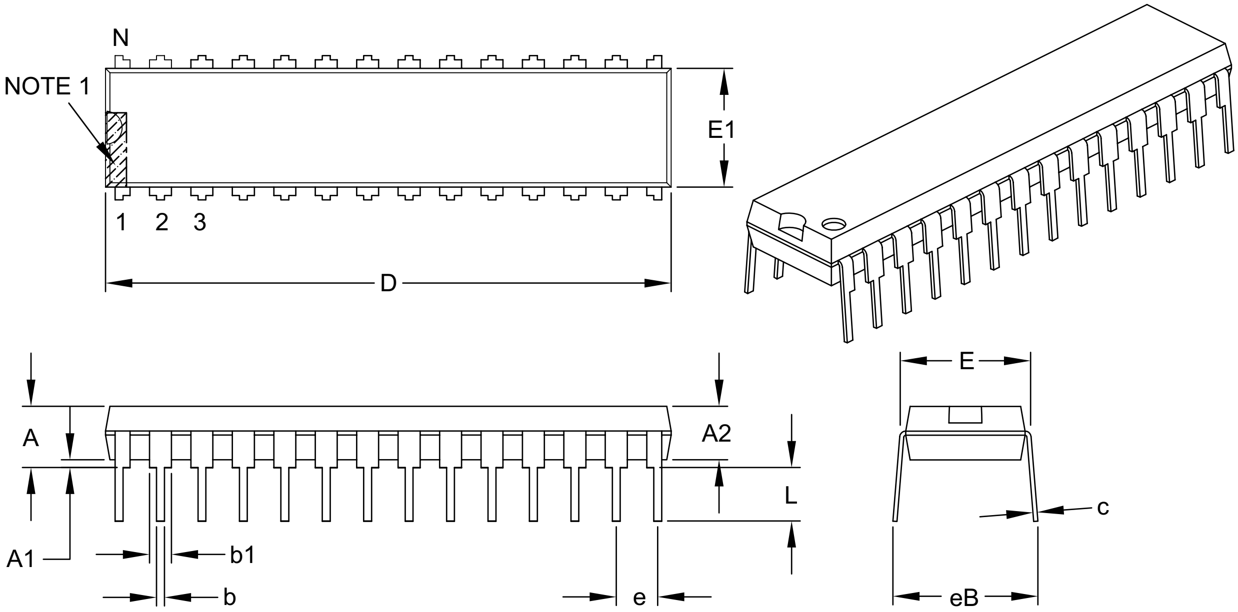


FIGURE 15-14: AVERAGE WDT PERIOD vs. VDD OVER TEMPERATURE (-40°C TO +125°C)



28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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