Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2144afa20v

Item	Page	Revision (See Manual for Details)
26.3.4 A/D Conversion Characteristics Table 26.27 A/D Conversion Characteristics (CIN15 to CIN0 Input: 134/266-State Conversion)	831	Note *4 added to table condition Condition C: V_{CC} = 3.0 V to 3.6V*4, AV_{CC} = 3.0 V to 3.6 V*4, AV_{ref} = 3.0 V to AV_{CC}*4, $V_{CC}B$ = 3.0 V to 5.5 V*4, ...
		Note 4 amended Note: 4. When using CIN, the applicable range is V_{CC} = 3.0 V to 3.6 V, ...
26.3.6 Flash Memory Characteristics Table 26.29 Flash Memory Characteristics (Programming/erasing operating range)	833	Table 26.29 amended Item amended (Before) Wait time after dummy write → (After) Wait time after H'FF dummy write Symbol of wait time after SWE-bit clear (Before) Θ → (After) θ

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reprogramming count	N_{WEC}	100*9	10000*9	—	Times	
Data retention time*10	t_{DRP}	10	—	—	Years	
Programming Wait time after SWE-bit setting*1	x	1	—	—	µs	

	834	Notes 8 to 10 added Notes: 8. Minimum number of times for which all characteristics are guaranteed after rewriting (Guarantee range is 1 to minimum value). 9. Reference value for 25°C (as a guideline, rewriting should normally function up to this value). 10. Data retention characteristic when rewriting is performed within the specification range, including the minimum value.
26.4.3 AC Characteristics Table 26.35 Control Signal Timing	849	Unit of t_{NMIH} amended (Before) — → (After) ns
Table 26.37 Timing of On-Chip Supporting Modules (1)	854, 855	Units of t_{PRS}, t_{PRH}, t_{FTIS}, t_{FTCS}, t_{TMRS}, t_{TMCS} amended (Before) — → (After) ns Units of t_{FTCWL}, t_{TMCWL}, synchronous t_{Scyc} amended (Before) — → (After) t_{cyc} Unit of t_{SCKf} amended (Before) 1.5 → (After) t_{cyc}
26.4.4 A/D Conversion Characteristics Table 26.41 A/D Conversion Characteristics (CIN15 to CIN0 Input: 134/266-State Conversion)	860	Table condition amended Table condition A (Before) ..., Ta = –20 to +75°C (regular specifications), Ta = –40 to +85°C (wide-range specifications) → (After) ... Ta = –20 to +75°C

Table 1.2 (b) H8S/2147N Pin Functions in Each Operating Mode

	Pin Name			
Pin No.	**Expanded Modes**		**Single-Chip Modes**	
FP-100B TFP-100B	**Mode 1**	**Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)**	**Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)**	**Flash Memory Writer Mode**
1	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
2	XTAL	XTAL	XTAL	XTAL
3	EXTAL	EXTAL	EXTAL	EXTAL
4	VCCB	VCCB	VCCB	VCC
5	MD1	MD1	MD1	VSS
6	MD0	MD0	MD0	VSS
7	NMI	NMI	NMI	FA9
8	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	VCC
9	VCC2	VCC2	VCC2	VCC
10	PA7/CIN15/ $\overline{\text{KIN15}}$/PS2CD	A23/PA7/CIN15/ $\overline{\text{KIN15}}$/PS2CD	PA7/CIN15/ $\overline{\text{KIN15}}$/PS2CD	NC
11	PA6/CIN14/ $\overline{\text{KIN14}}$/PS2CC	A22/PA6/CIN14/ $\overline{\text{KIN14}}$/PS2CC	PA6/CIN14/ $\overline{\text{KIN14}}$/PS2CC	NC
12	P52/SCK0/SCL0	P52/SCK0/SCL0	P52/SCK0/SCL0	NC
13	P51/RxD0	P51/RxD0	P51/RxD0	FA17
14	P50/TxD0	P50/TxD0	P50/TxD0	NC
15	VSS	VSS	VSS	VSS
16	P97/$\overline{\text{WAIT}}$/SDA0	P97/$\overline{\text{WAIT}}$/SDA0	P97/SDA0	VCC
17	ϕ/P96/EXCL	ϕ/P96/EXCL	P96/ϕ/EXCL	NC
18	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	P95/$\overline{\text{CS1}}$	FA16
19	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	P94/$\overline{\text{IOW}}$	FA15
20	PA5/CIN13/ $\overline{\text{KIN13}}$/PS2BD	A21/PA5/CIN13/ $\overline{\text{KIN13}}$/PS2BD	PA5/CIN13/ $\overline{\text{KIN13}}$/PS2BD	NC
21	PA4/CIN12/ $\overline{\text{KIN12}}$/PS2BC	A20/PA4/CIN12/ $\overline{\text{KIN12}}$/PS2BC	PA4/CIN12/ $\overline{\text{KIN12}}$/PS2BC	NC
22	$\overline{\text{RD}}$	$\overline{\text{RD}}$	P93/$\overline{\text{IOR}}$	$\overline{\text{WE}}$
23	P92/$\overline{\text{IRQ0}}$	P92/$\overline{\text{IRQ0}}$	P92/$\overline{\text{IRQ0}}$	VSS
24	P91/$\overline{\text{IRQ1}}$	P91/$\overline{\text{IRQ1}}$	P91/$\overline{\text{IRQ1}}$	VCC

Type	Symbol	Pin No. FP-100B TFP-100B	I/O	Name and Function
Bus control	$\overline{\text{WAIT}}$	16	Input	**Wait:** Requests insertion of a wait state in the bus cycle when accessing external 3-state address space.
	$\overline{\text{RD}}$	22	Output	**Read:** When this pin is low, it indicates that the external address space is being read.
	$\overline{\text{HWR}}$	19	Output	**High write:** When this pin is low, it indicates that the external address space is being written to. The upper half of the data bus is valid.
	$\overline{\text{LWR}}$	25	Output	**Low write:** When this pin is low, it indicates that the external address space is being written to. The lower half of the data bus is valid.
	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	18	Output	**Address strobe:** When this pin is low, it indicates that address output on the address bus is valid.
Interrupt signals	NMI	7	Input	**Nonmaskable interrupt:** Requests a nonmaskable interrupt.
	$\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$	23 to 25, 97 to 99, 34, 35	Input	**Interrupt request 0 to 7:** These pins request a maskable interrupt.
16-bit free-running timer (FRT)	FTCI	26	Input	**FRT counter clock input:** Input pin for an external clock signal for the free-running counter (FRC).
	FTOA	27	Output	**FRT output compare A output:** The output compare A output pin.
	FTOB	34	Output	**FRT output compare B output:** The output compare B output pin.
	FTIA	28	Input	**FRT input capture A input:** The input capture A input pin.
	FTIB	29	Input	**FRT input capture B input:** The input capture B input pin.
	FTIC	32	Input	**FRT input capture C input:** The input capture C input pin.
	FTID	33	Input	**FRT input capture D input:** The input capture D input pin.

6.1.3 Pin Configuration

Table 6.1 summarizes the pins of the bus controller.

Table 6.1 Bus Controller Pins

Name	Symbol	I/O	Function
Address strobe	$\overline{AS}$	Output	Strobe signal indicating that address output on address bus is enabled (when IOSE bit is 0)
I/O select	$\overline{IOS}$	Output	I/O select signal (when IOSE bit is 1)
Read	$\overline{RD}$	Output	Strobe signal indicating that external space is being read
High write	$\overline{HWR}$	Output	Strobe signal indicating that external space is being written to, and that the upper data bus (D15 to D8) is enabled
Low write	$\overline{LWR}$	Output	Strobe signal indicating that external space is being written to, and that the lower data bus (D7 to D0) is enabled
Wait	$\overline{WAIT}$	Input	Wait request signal when external 3-state access space is accessed

6.1.4 Register Configuration

Table 6.2 summarizes the registers of the bus controller.

Table 6.2 Bus Controller Registers

Name	Abbreviation	R/W	Initial Value	Address*
Bus control register	BCR	R/W	H'D7	H'FFC6
Wait state control register	WSCR	R/W	H'33	H'FFC7

Note: * Lower 16 bits of the address.

Bits 3 and 2—DTC Mode (MD1, MD0): These bits specify the DTC transfer mode.

Bit 3	Bit 2	
MD1	**MD0**	**Description**
0	0	Normal mode
	1	Repeat mode
1	0	Block transfer mode
	1	—

Bit 1—DTC Transfer Mode Select (DTS): Specifies whether the source side or the destination side is set to be a repeat area or block area, in repeat mode or block transfer mode.

Bit 1	
DTS	**Description**
0	Destination side is repeat area or block area
1	Source side is repeat area or block area

Bit 0—DTC Data Transfer Size (Sz): Specifies the size of data to be transferred.

Bit 0	
Sz	**Description**
0	Byte-size transfer
1	Word-size transfer

7.3.9 Operation Timing

Figures 7.10 to 7.12 show examples of DTC operation timing.

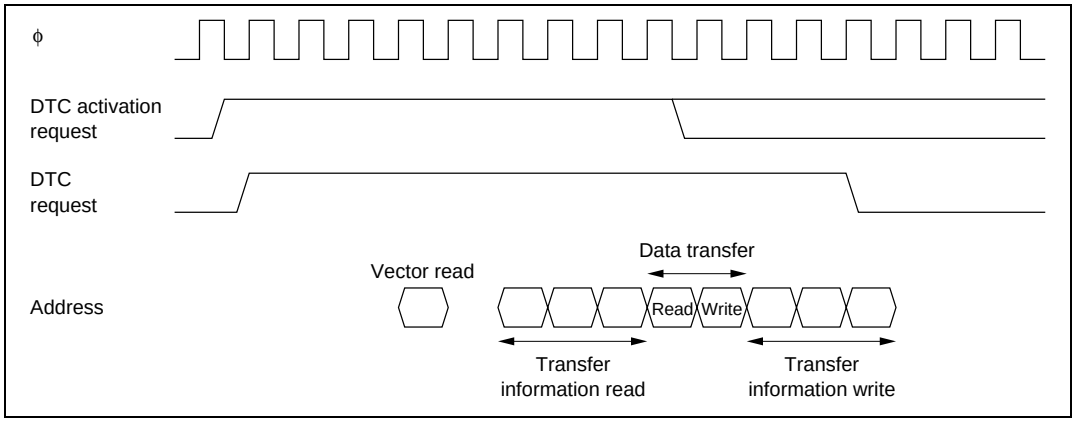


Figure 7.10 DTC Operation Timing (Normal Mode or Repeat Mode)

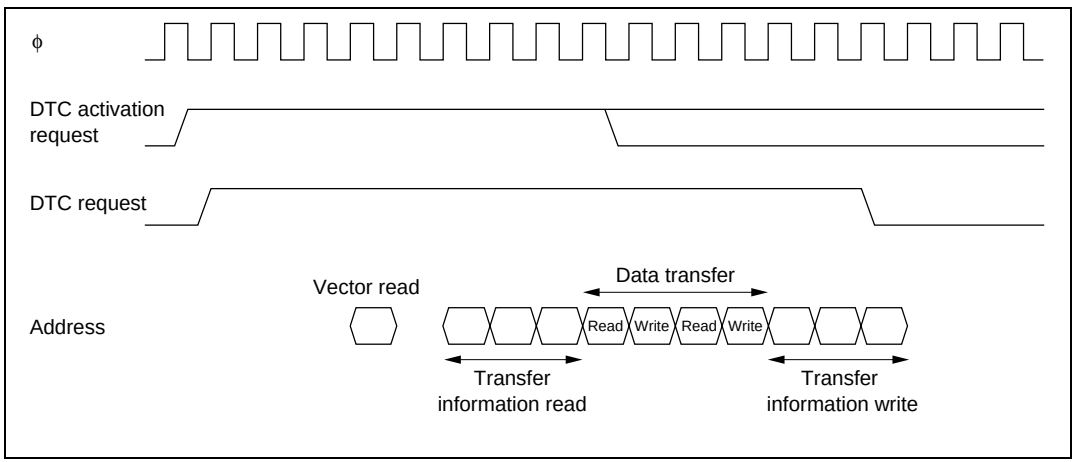


Figure 7.11 DTC Operation Timing (Block Transfer Mode, with Block Size of 2)

Pin	Selection Method and Pin Functions

PB4/D4

The pin function is switched as shown below according to the combination of the operating mode, bit PB4DDR, and bit ABW in WSCR.

Operating mode	Modes 1, 2, 3 (EXPE = 1)			Modes 2, 3 (EXPE = 0)	
ABW	0	1		—	
PB4DDR	—	0	1	0	1
Pin function	D4 I/O pin	PB4 input pin	PB4 output pin	PB4 input pin	PB4 output pin

PB3/D3/$\overline{CS4}$

The pin function is switched as shown below according to the combination of the operating mode, bits HI12E and CS4E in SYSCR2, bit ABW in WSCR, and bit PB3DDR.

Operating mode	Modes 1, 2, 3 (EXPE = 1)			Modes 2, 3 (EXPE = 0)		
HI12E	—			Either cleared to 0		1
CS4E	—					1
ABW	0	1		—		—
PB3DDR	—	0	1	0	1	—
Pin function	D3 I/O pin	PB3 input pin	PB3 output pin	PB3 input pin	PB3 output pin	$\overline{CS4}$ input pin

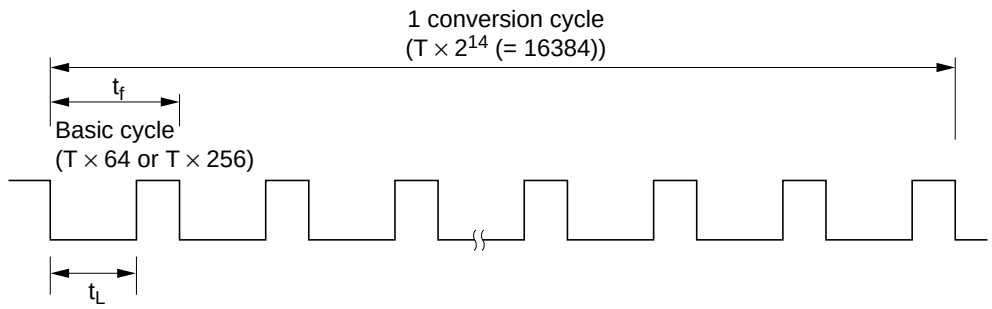
PB2/D2/$\overline{CS3}$

The pin function is switched as shown below according to the combination of the operating mode, bits HI12E and CS3E in SYSCR2, bit ABW in WSCR, and bit PB2DDR.

Operating mode	Modes 1, 2, 3 (EXPE = 1)			Modes 2, 3 (EXPE = 0)		
HI12E	—			Either cleared to 0		1
CS3E	—					1
ABW	0	1		—		—
PB2DDR	—	0	1	0	1	—
Pin function	D2 I/O pin	PB2 input pin	PB2 output pin	PB2 input pin	PB2 output pin	$\overline{CS3}$ input pin

10.4 Operation

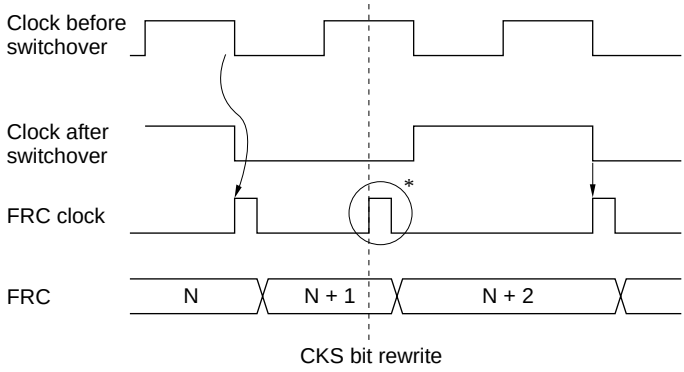
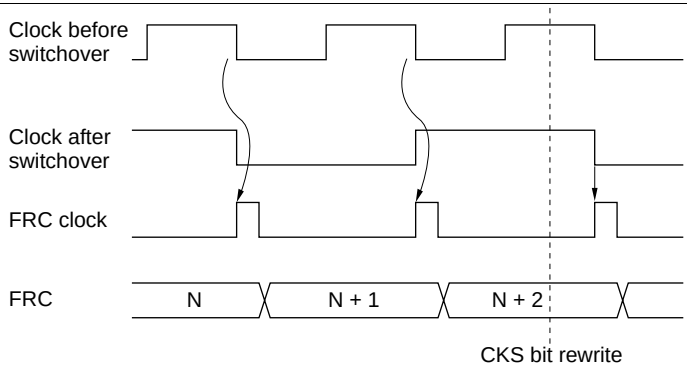
A PWM waveform like the one shown in figure 10.3 is output from the PWMX pin. When OS = 0, the value in DADR corresponds to the total width (T_L) of the low (0) pulses output in one conversion cycle (256 pulses when CFS = 0, 64 pulses when CFS = 1). When OS = 1, the output waveform is inverted and the DADR value corresponds to the total width (T_H) of the high (1) output pulses. Figure 10.4 shows the types of waveform output available.



Legend:
T: Resolution
$T_L = \sum_{n=1}^{m} t_{Ln}$ (when OS = 0)
(When CFS = 0, m = 256; when CFS = 1, m = 64)

Figure 10.3 PWM D/A Operation

Table 10.4 summarizes the relationships of the CKS, CFS, and OS bit settings to the resolution, base cycle, and conversion cycle. The PWM output remains flat unless DADR contains at least a certain minimum value. Table 10.4 indicates the range of DADR settings that give an output waveform like the one in figure 10.3, and lists the conversion cycle length when low-order DADR bits are kept cleared to 0, reducing the conversion precision to 12 bits or 10 bits.

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	FRC Operation
3	Switching from high to low	
4	Switching from high to high	

Note: * Generated on the assumption that the switchover is a falling edge; FRC is incremented.

12.2.4 Timer Control Register (TCR)

Bit	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCR is an 8-bit readable/writable register that selects the clock source and the time at which TCNT is cleared, and enables interrupts.

TCR is initialized to H'00 by a reset and in hardware standby mode.

For details of the timing, see section 12.3, Operation.

Bit 7—Compare-Match Interrupt Enable B (CMIEB): Selects whether the CMFB interrupt request (CMIB) is enabled or disabled when the CMFB flag in TCSR is set to 1.

Note that a CMIB interrupt is not requested by TMRX, regardless of the CMIEB value.

Bit 7

CMIEB	Description	
0	CMFB interrupt request (CMIB) is disabled	(Initial value)
1	CMFB interrupt request (CMIB) is enabled	

Bit 6—Compare-Match Interrupt Enable A (CMIEA): Selects whether the CMFA interrupt request (CMIA) is enabled or disabled when the CMFA flag in TCSR is set to 1.

Note that a CMIA interrupt is not requested by TMRX, regardless of the CMIEA value.

Bit 6

CMIEA	Description	
0	CMFA interrupt request (CMIA) is disabled	(Initial value)
1	CMFA interrupt request (CMIA) is enabled	

	Operating Frequency ϕ (MHz)											
	ϕ = 14 MHz			ϕ = 14.7456 MHz			ϕ = 16 MHz			ϕ = 17.2032 MHz		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	64	0.70	3	70	0.03	3	75	0.48
150	2	181	0.16	2	191	0.00	2	207	0.16	2	223	0.00
300	2	90	0.16	2	95	0.00	2	103	0.16	2	111	0.00
600	1	181	0.16	1	191	0.00	1	207	0.16	1	223	0.00
1200	1	90	0.16	1	95	0.00	1	103	0.16	1	111	0.00
2400	0	181	0.16	0	191	0.00	0	207	0.16	0	223	0.00
4800	0	90	0.16	0	95	0.00	0	103	0.16	0	111	0.00
9600	0	45	–0.93	0	47	0.00	0	51	0.16	0	55	0.00
19200	0	22	–0.93	0	23	0.00	0	25	0.16	0	27	0.00
31250	0	13	0.00	0	14	–1.70	0	15	0.00	0	16	1.20
38400	—	—	—	0	11	0.00	0	12	0.16	0	13	0.00

	Operating Frequency ϕ (MHz)								
	ϕ = 18 MHz			ϕ = 19.6608 MHz			ϕ = 20 MHz		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	79	–0.12	3	86	0.31	3	88	–0.25
150	2	233	0.16	2	255	0.00	3	64	0.16
300	2	116	0.16	2	127	0.00	2	129	0.16
600	1	233	0.16	1	255	0.00	2	64	0.16
1200	1	116	0.16	1	127	0.00	1	129	0.16
2400	0	233	0.16	0	255	0.00	1	64	0.16
4800	0	116	0.16	0	127	0.00	0	129	0.16
9600	0	58	–0.69	0	63	0.00	0	64	0.16
19200	0	28	1.02	0	31	0.00	0	32	–1.36
31250	0	17	0.00	0	19	–1.70	0	19	0.00
38400	0	14	–2.34	0	15	0.00	0	15	1.73

Bit 1—Host Interface Enable (HIE): Enables or disables CPU access to the host interface registers. When enabled, the host interface registers (HICR, IDR1, ODR1, STR1, IDR2, ODR2, and STR2) can be accessed.

Bit 1

HIE	Description
0	Host interface register (HICR, IDR1, ODR1, STR1, IDR2, ODR2, STR2), CPU access is disabled (Initial value)
1	Host interface register (HICR, IDR1, ODR1, STR1, IDR2, ODR2, STR2), CPU access is enabled

18.2.2 System Control Register 2 (SYSCR2)

Bit	7	6	5	4	3	2	1	0
	KWUL1	KWUL0	P6PUE	—	SDE	CS4E	CS3E	HI12E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W

SYSCR2 is an 8-bit readable/writable register which controls chip operations. Host interface functions are enabled or disabled by the HI12E bit in SYSCR2. The number of channels that can be used can be extended to a maximum of four by means of the CS3E bit and CS4E bit. SYSCR2 is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 and 6—Key Wakeup Level 1 and 0 (KWUL1, KWUL0): The port 6 input level can be set and changed by software. For details see section 8, I/O Ports.

Bit 5—Port 6 Input Pull-Up Extra (P6PUE): Controls and selects the current specification for the port 6 MOS input pull-up function connected by means of KMPCR settings. For details see section 8, I/O Ports.

Bit 4—Reserved: Do not write 1 to this bit.

22.6.1 Boot Mode

When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. The channel 1 SCI to be used is set to asynchronous mode.

When a reset-start is executed after this group MCU's pins have been set to boot mode, the boot program built into the MCU is started and the programming control program prepared in the host is serially transmitted to the MCU via the SCI. In the MCU, the programming control program received via the SCI is written into the programming control program area in on-chip RAM. After the transfer is completed, control branches to the start address of the programming control program area and the programming control program execution state is entered (flash memory programming is performed).

The transferred programming control program must therefore include coding that follows the programming algorithm given later.

The system configuration in boot mode is shown in figure 22.7, and the boot program mode execution procedure in figure 22.8.

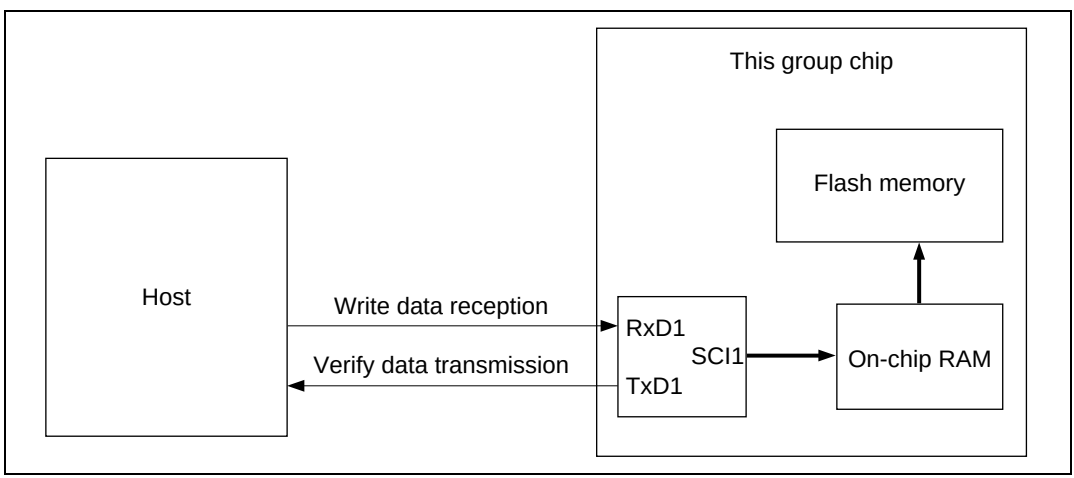


Figure 22.7 System Configuration in Boot Mode

Table 26.25 I²C Bus Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{CC} = 2.7 V to 3.6 V (3 V version), V_{SS} = 0 V,
ϕ = 5 MHz to maximum operating frequency

		Ratings					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Notes**
SCL input cycle time	t_{SCL}	12	—	—	t_{cyc}		Figure 26.28
SCL input high pulse width	t_{SCLH}	3	—	—	t_{cyc}		
SCL input low pulse width	t_{SCLL}	5	—	—	t_{cyc}		
SCL, SDA input rise time	t_{Sr}	—	—	7.5*	t_{cyc}		
SCL, SDA input fall time	t_{Sf}	—	—	300	ns		
SCL, SDA output fall time	t_{of}	20 + 0.1 Cb	—	250	ns		
SCL, SDA input spike pulse elimination time	t_{SP}	—	—	1	t_{cyc}		
SDA input bus free time	t_{BUF}	5	—	—	t_{cyc}		
Start condition input hold time	t_{STAH}	3	—	—	t_{cyc}		
Retransmission start condition input setup time	t_{STAS}	3	—	—	t_{cyc}		
Stop condition input setup time	t_{STOS}	3	—	—	t_{cyc}		
Data input setup time	t_{SDAS}	0.5	—	—	t_{cyc}		
Data input hold time	t_{SDAH}	0	—	—	ns		
SCL, SDA capacitive load	C_b	—	—	400	pF		

Note: * $17.5t_{cyc}$ can be set according to the clock selected for use by the I²C module. For details, see section 16.4, Usage Notes.

Lower Address	Register Name	H8S/2148 Group Register Selection Conditions		H8S/2147N Register Selection Conditions		H8S/2144 Group Register Selection Conditions	Module Name
H'FEF3	DTVECR	No conditions		—		—	DTC
H'FEF4	ABRKCR	No conditions		No conditions		No conditions	Interrupt controller
H'FEF5	BARA						
H'FEF6	BARB						
H'FEF7	BARC						
H'FF80	FLMCR1	FLSHE = 1 in STCR		FLSHE = 1 in STCR		FLSHE = 1 in STCR	Flash memory
H'FF81	FLMCR2						
H'FF82	PCSR	FLSHE = 0 in STCR		FLSHE = 0 in STCR		—	PWM
	EBR1	FLSHE = 1 in STCR		FLSHE = 1 in STCR		FLSHE = 1 in STCR	Flash memory
H'FF83	SYSCR2	FLSHE = 0 in STCR		FLSHE = 0 in STCR		—	HIF
	EBR2	FLSHE = 1 in STCR		FLSHE = 1 in STCR		FLSHE = 1 in STCR	Flash memory
H'FF84	SBYCR	FLSHE = 0 in STCR		FLSHE = 0 in STCR		FLSHE = 0 in STCR	System
H'FF85	LPWRCR						
H'FF86	MSTPCRH						
H'FF87	MSTPCRL						
H'FF88	SMR1	MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR	SCI1
	ICCR1	MSTP3 = 0, IICE = 1 in STCR		MSTP3 = 0, IICE = 1 in STCR		—	IIC1
H'FF89	BRR1	MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR	SCI1
	ICSR1	MSTP3 = 0, IICE = 1 in STCR		MSTP3 = 0, IICE = 1 in STCR		—	IIC1
H'FF8A	SCR1	MSTP6 = 0		MSTP6 = 0		MSTP6 = 0	SCI1
H'FF8B	TDR1						
H'FF8C	SSR1						
H'FF8D	RDR1						
H'FF8E	SCMR1	MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR	
	ICDR1	MSTP3 = 0, IICE = 1 in STCR	ICE = 1 in ICCR1	MSTP3 = 0, IICE = 1 in STCR	ICE = 1 in ICCR1	—	IIC1
	SARX1		ICE = 0 in ICCR1		ICE = 0 in ICCR1		
H'FF8F	ICMR1		ICE = 1 in ICCR1		ICE = 1 in ICCR1		
	SAR1		ICE = 0 in ICCR1		ICE = 0 in ICCR1		
H'FF90	TIER	MSTP13 = 0		MSTP13 = 0		MSTP13 = 0	FRT
H'FF91	TCSR						
H'FF92	FRCH						
H'FF93	FRCL						

FRC—Free-Running Counter **H'FF92** **FRT**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value

OCRA/OCRB—Output Compare Register A/B **H'FF94** **FRT**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Constantly compared with FRC value; OCF is set when OCR = FRC

P8DR—Port 8 Data Register **H'FFBF** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	P86DR	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output data for port 8 pins

P9DDR—Port 9 Data Direction Register **H'FFC0** **Port 9**

Bit	7	6	5	4	3	2	1	0
	P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	P91DDR	P90DDR
Mode 1								
Initial value	0	1	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Modes 2 and 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specification of input or output for port 9 pins

P9DR—Port 9 Data Register **H'FFC1** **Port 9**

Bit	7	6	5	4	3	2	1	0
	P97DR	P96DR	P95DR	P94DR	P93DR	P92DR	P91DR	P90DR
Initial value	0	—*	0	0	0	0	0	0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Output data for port 9 pins

Note: * Determined by state of pin P96.

TCORA0—Time Constant Register A0	**H'FFCC**	**TMR0**
TCORA1—Time Constant Register A1	**H'FFCD**	**TMR1**
TCORB0—Time Constant Register B0	**H'FFCE**	**TMR0**
TCORB1—Time Constant Register B1	**H'FFCF**	**TMR1**
TCORAY—Time Constant Register AY	**H'FFF2**	**TMRY**
TCORBY—Time Constant Register BY	**H'FFF3**	**TMRY**
TCORC—Time Constant Register C	**H'FFF5**	**TMRX**
TCORAX—Time Constant Register AX	**H'FFF6**	**TMRX**
TCORBX—Time Constant Register BX	**H'FFF7**	**TMRX**

TCORA0
TCORB0

TCORA1
TCORB1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Compare match flag (CMF) is set when TCOR and TCNT values match

TCORAX, TCORAY
TCORBX, TCORBY

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Compare match flag (CMF) is set when TCOR and TCNT values match

TCORC

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Compare match C signal is generated when sum of TCORC and TICR contents match TCNT value

ADCR—A/D Control Register **H'FFE9** **A/D Converter**

Bit	7	6	5	4	3	2	1	0
	TRGS1	TRGS0	—	—	—	—	—	—
Initial value	0	0	1	1	1	1	1	1
Read/Write	R/W	R/W	—	—	—	—	—	—

Timer trigger select

0	0	Start of A/D conversion by external trigger is disabled
	1	Start of A/D conversion by external trigger is disabled
1	0	Start of A/D conversion by external trigger (8-bit timer) is enabled
	1	Start of A/D conversion by external trigger pin is enabled

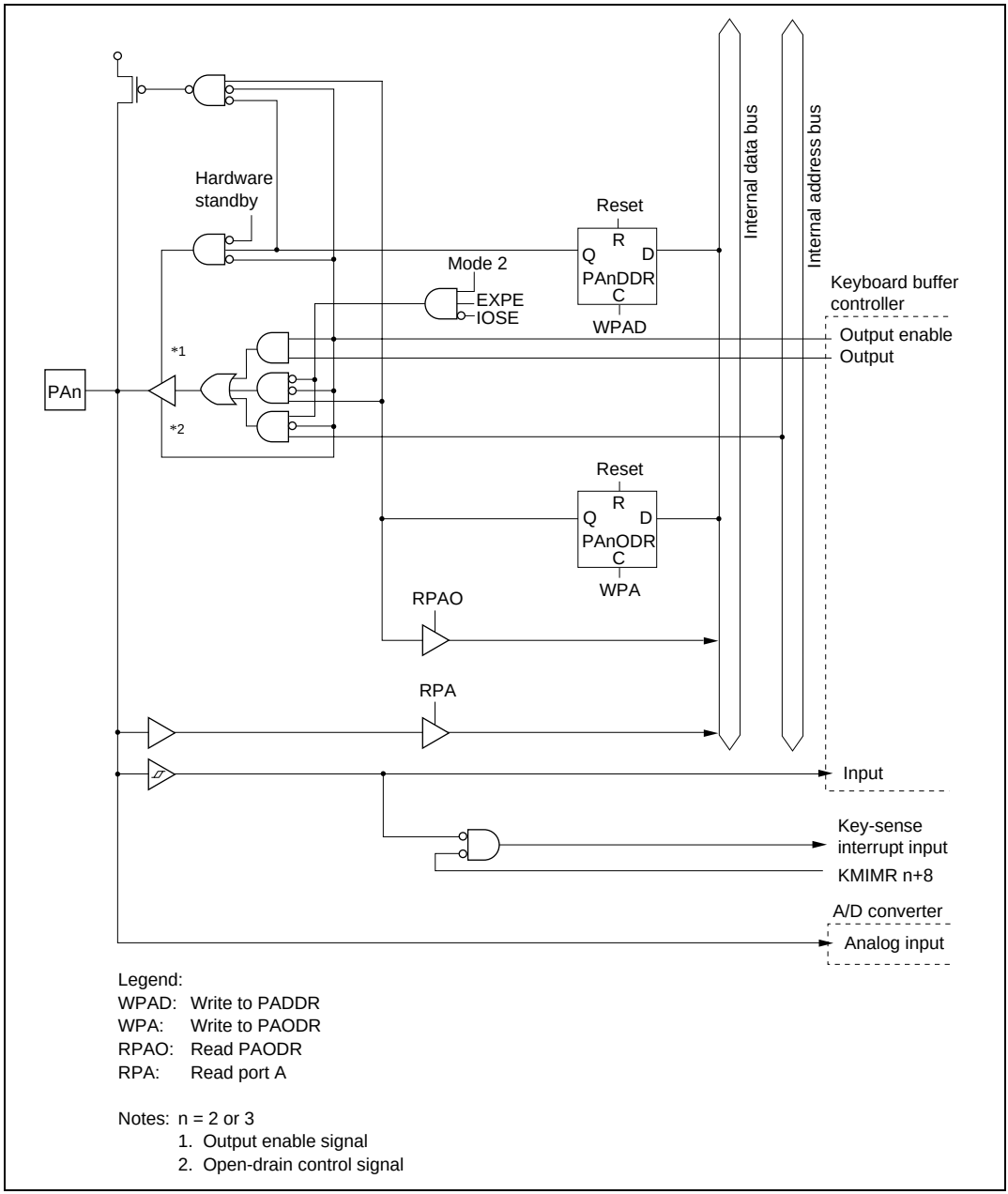


Figure C.35 Port A Block Diagram (Pins PA2, PA3)