Renesas Electronics America Inc - DF2144AVFA10V Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2144avfa10v

Item	Specifications				
Product lineup (preliminary)	Product Code[*2]				
	Group	Mask ROM Versions	F-ZTAT Versions	ROM/RAM (Bytes)	Packages
	H8S/2148	HD6432148S	HD64F2148 HD64F2148V[*2]	128 k/4 k	FP-100B, TFP-100B
		HD6432148SW[*1]	HD64F2148A HD64F2148AV[*2]		
		HD6432147S	HD64F2147A	64 k/2 k	
		HD6432147SW[*1]	HD64F2147AV[*2]		
	H8S/2147N	—	HD64F2147N HD64F2147NV[*2]	64 k/2 k	
	H8S/2144	HD6432144S	HD64F2144 HD64F2144V[*2]	128 k/4 k	
			HD64F2144A HD64F2144AV[*2]		
		HD6432143S	—	96 k/4 k	
		HD6432142	HD64F2142R HD64F2142RV[*2]	64 k/2 k	
	Notes: 1. W indicates the I^2C bus option. 2. V indicates the 3-V version. Please refer to appendix F, Product Code Lineup.				

1.2 Internal Block Diagram

An internal block diagram of the H8S/2148 Group is shown in figure 1.1 (a), an internal block diagram of the H8S/2147N is shown in figure 1.1 (b), and an internal block diagram of the H8S/2144 Group in figure 1.1 (c).

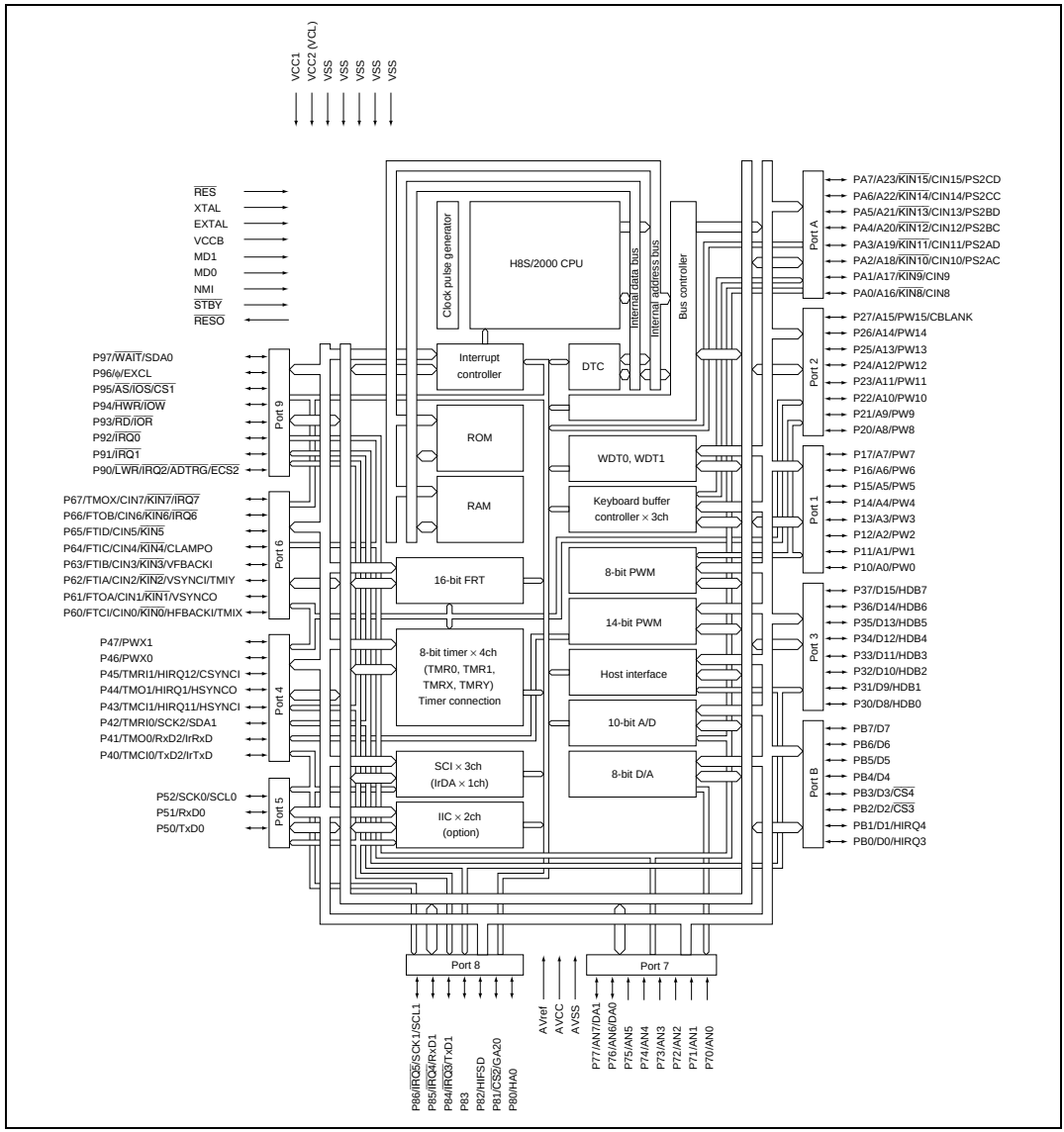
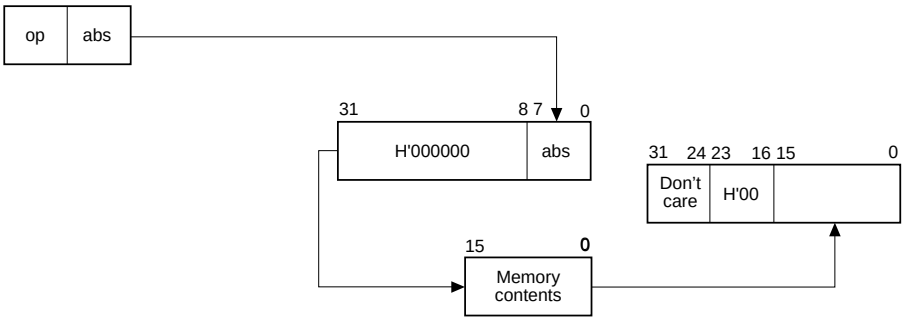


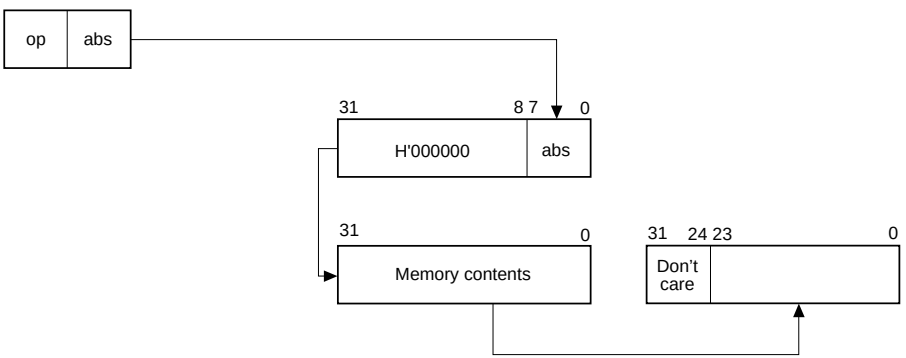
Figure 1.1 (a) Internal Block Diagram of H8S/2148 Group

No.	Addressing Mode and Instruction Format	Effective Address Calculation	Effective Address (EA)
8	Memory indirect @@aa:8		

- Normal mode



- Advanced mode



5.3 Interrupt Sources

Interrupt sources comprise external interrupts (NMI and IRQ7 to IRQ0) and internal interrupts.

5.3.1 External Interrupts

There are nine external interrupt sources from 25 input pins (23 actual pins): NMI, $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$, and $\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$. KIN15 to KIN8 share the IRQ7 interrupt source, and KIN7 to KIN0 share the IRQ6 interrupt source. Of these, NMI, IRQ7, IRQ6, and IRQ2 to IRQ0 can be used to restore the H8S/2148 Group or H8S/2144 Group chip from software standby mode.

NMI Interrupt

NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the interrupt control mode and the status of the CPU interrupt mask bits. The NMIEG bit in SYSCR can be used to select whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

The vector number for NMI interrupt exception handling is 7.

IRQ7 to IRQ0 Interrupts

Interrupts IRQ7 to IRQ0 are requested by an input signal at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$. Interrupts IRQ7 to IRQ0 have the following features:

- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.
- Enabling or disabling of interrupt requests IRQ7 to IRQ0 can be selected with IER.
- The interrupt control level can be set with ICR.
- The status of interrupt requests IRQ7 to IRQ0 is indicated in ISR. ISR flags can be cleared to 0 by software.

A block diagram of interrupts IRQ7 to IRQ0 is shown in figure 5.3.

6.5.3 Wait Control

As with the basic bus interface, either program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) of the burst ROM interface. See section 6.4.5, Wait Control.

Wait states cannot be inserted in a burst cycle.

6.6 Idle Cycle

6.6.1 Operation

When this LSI chip accesses external space, it can insert a 1-state idle cycle (T_i) between bus cycles when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, with a long output floating time, and high-speed memory, I/O interfaces, and so on.

If an external write occurs after an external read while the ICIS0 bit in BCR is set to 1, an idle cycle is inserted at the start of the write cycle. This is enabled in advanced mode and normal mode.

Figure 6.15 shows an example of the operation in this case. In this example, bus cycle A is a read cycle from ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

8.2 Port 1

8.2.1 Overview

Port 1 is an 8-bit I/O port. Port 1 pins also function as address bus output pins (A7 to A0), and as 8-bit PWM output pins (PW7 to PW0) (H8S/2148 Group and H8S/2147N only). Port 1 functions change according to the operating mode. Port 1 has a built-in MOS input pull-up function that can be controlled by software.

Figure 8.1 shows the port 1 pin configuration.

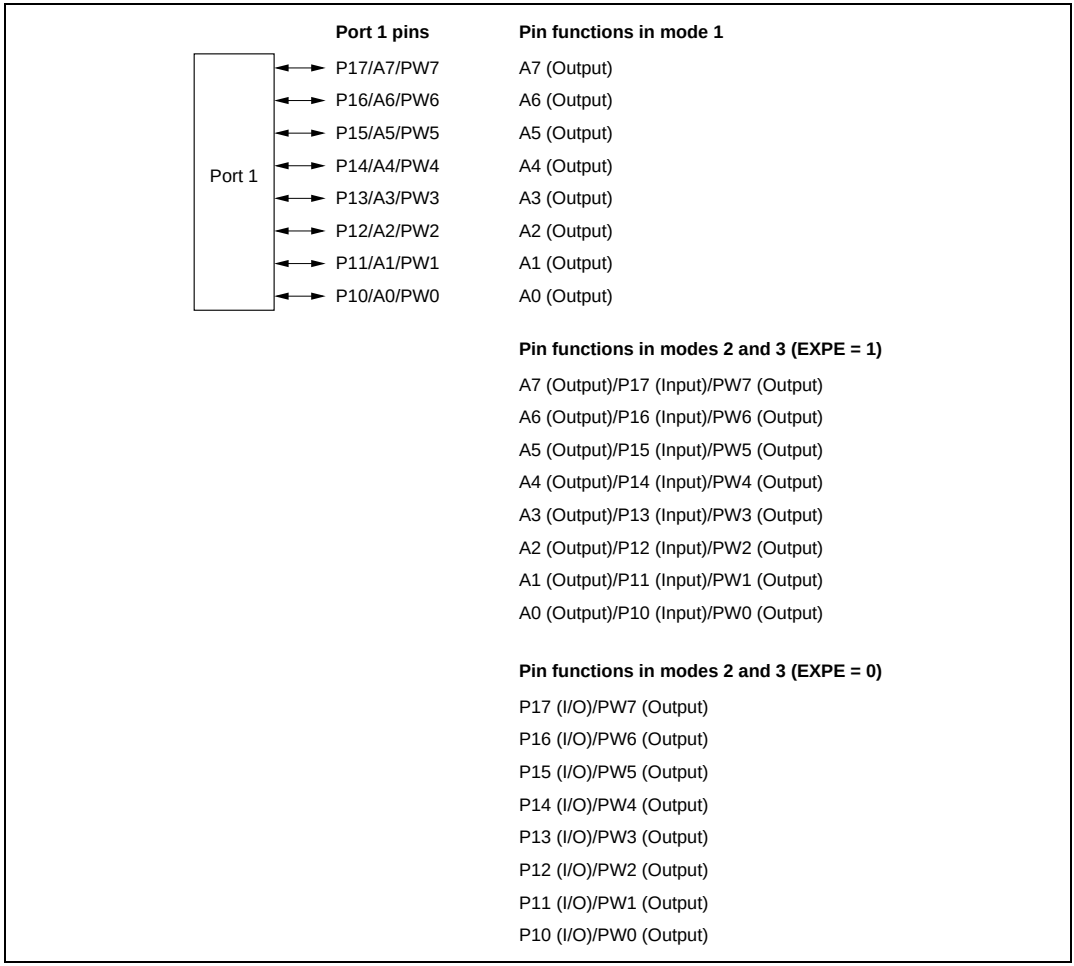
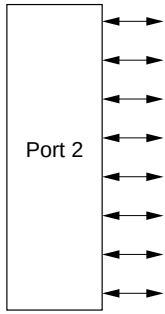


Figure 8.1 Port 1 Pin Functions



Port 2 pins	Pin functions in mode 1
P27/A15/PW15/CBLANK	A15 (Output)
P26/A14/PW14	A14 (Output)
P25/A13/PW13	A13 (Output)
P24/A12/PW12	A12 (Output)
P23/A11/PW11	A11 (Output)
P22/A10/PW10	A10 (Output)
P21/A9/PW9	A9 (Output)
P20/A8/PW8	A8 (Output)

Pin functions in modes 2 and 3 (EXPE = 1)

A15 (Output)/P27 (I/O)/PW15 (Output)/CBLANK (Output)
A14 (Output)/P26 (I/O)/PW14 (Output)
A13 (Output)/P25 (I/O)/PW13 (Output)
A12 (Output)/P24 (I/O)/PW12 (Output)
A11 (Output)/P23 (Input)/PW11 (Output)
A10 (Output)/P22 (Input)/PW10 (Output)
A9 (Output)/P21 (Input)/PW9 (Output)
A8 (Output)/P20 (Input)/PW8 (Output)

Pin functions in modes 2 and 3 (EXPE = 0)

P27 (I/O)/PW15 (Output)/CBLANK (Output)
P26 (I/O)/PW14 (Output)
P25 (I/O)/PW13 (Output)
P24 (I/O)/PW12 (Output)
P23 (I/O)/PW11 (Output)
P22 (I/O)/PW10 (Output)
P21 (I/O)/PW9 (Output)
P20 (I/O)/PW8 (Output)

Figure 8.5 Port 2 Pin Functions

8.12.4 MOS Input Pull-Up Function

Port B has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 1, 2 and 3 (EXPE = 1) with the ABW bit in WSCR set to 1, and in modes 2 and 3 (EXPE = 0), and can be specified as on or off on a bit-by-bit basis.

When a PBDDR bit is cleared to 0, setting the corresponding PBODR bit to 1 turns on the MOS input pull-up for that pin. When a pin is designated as an on-chip supporting module output pin, the MOS input pull-up is always off.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 8.27 summarizes the MOS input pull-up states.

Table 8.27 MOS Input Pull-Up States (Port B)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 3 (EXPE = 1) with ABW in WSCR = 0	Off	Off	Off	Off
1, 2, 3 (EXPE = 1) with ABW in WSCR = 1, and 2, 3 (EXPE = 0)			On/Off	On/Off

Legend:

Off: MOS input pull-up is always off.

On/Off: On when PBDDR = 0 and PBODR = 1; otherwise off.

11.3.7 Setting of FRC Overflow Flag (OVF)

The FRC overflow flag (OVF) is set to 1 when FRC overflows (changes from H'FFFF to H'0000). Figure 11.13 shows the timing of this operation.

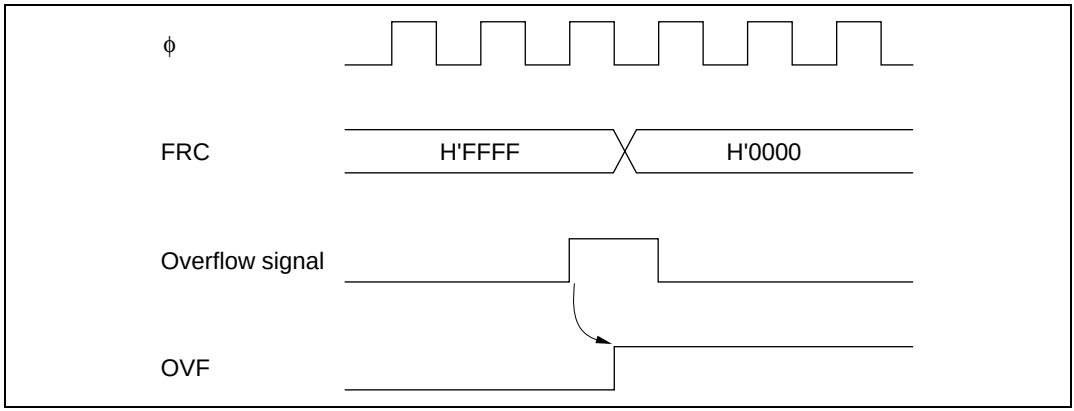


Figure 11.13 Setting of Overflow Flag (OVF)

11.3.8 Automatic Addition of OCRA and OCRAR/OCRAF

When the OCRAMS bit in TOCR is set to 1, the contents of OCRAR and OCRAF are automatically added to OCRA alternately, and when an OCRA compare-match occurs a write to OCRA is performed. The OCRA write timing is shown in figure 11.14.

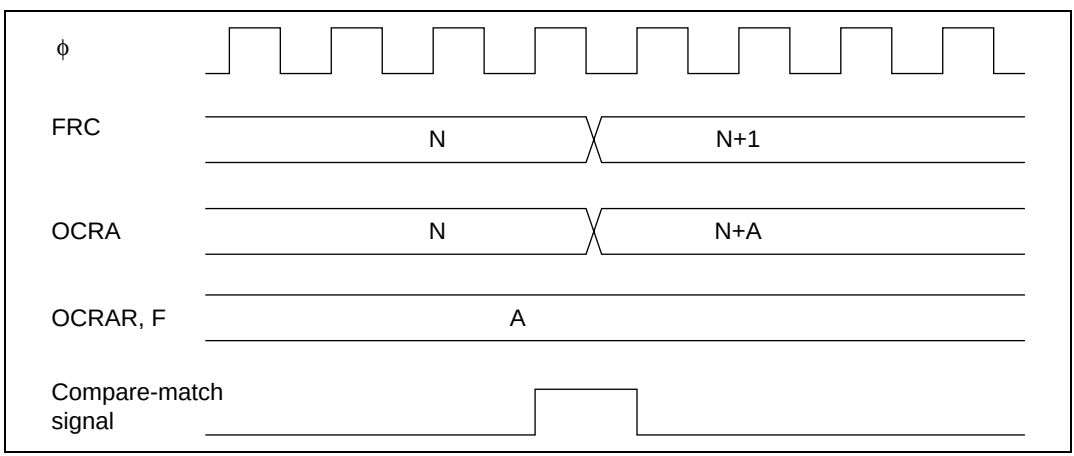


Figure 11.14 OCRA Automatic Addition Timing

12.2.7 System Control Register (SYSCR)

Bit	7	6	5	4	3	2	1	0
	CS2E	IOSE	INTM1	INTM0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R	R/W	R	R/W	R/W	R/W

Only bit 1 is described here. For details on functions not related to the 8-bit timers, see sections 3.2.2 and 5.2.1, System Control Register (SYSCR), and the descriptions of the relevant modules.

Bit 1—Host Interface Enable (HIE): Controls CPU access to 8-bit timer (channel X and Y) data registers and control registers, and timer connection control registers.

Bit 1

HIE	Description
0	CPU access to 8-bit timer (channel X and Y) data registers and control registers, and timer connection control registers, is enabled (Initial value)
1	CPU access to 8-bit timer (channel X and Y) data registers and control registers, and timer connection control registers, is disabled

12.2.8 Timer Connection Register S (TCONRS)

Bit	7	6	5	4	3	2	1	0
	TMRX/Y	ISGENE	HOMOD1	HOMOD0	VOMOD1	VOMOD0	CLMOD1	CLMOD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCONRS is an 8-bit readable/writable register that controls access to the TMRX and TMRY registers and timer connection operation.

TCONRS is initialized to H'00 by a reset and in hardware standby mode.

Figure 15.13 shows an example of SCI operation for multiprocessor format reception.

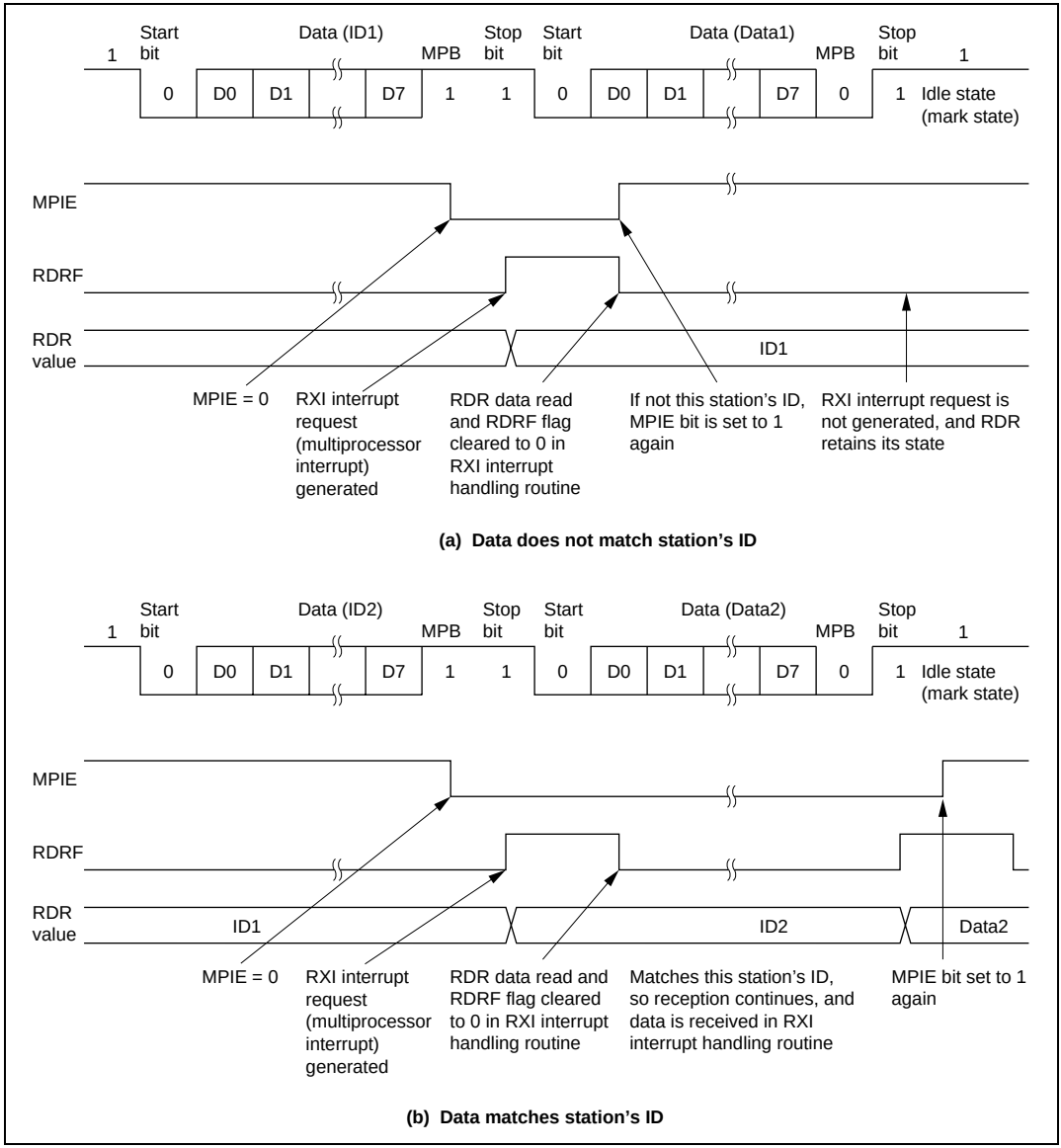


Figure 15.13 Example of SCI Operation in Reception (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

16.2.2 Slave Address Register (SAR)

Bit	7	6	5	4	3	2	1	0
	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SAR is an 8-bit readable/writable register that stores the slave address and selects the communication format. When the chip is in slave mode (and the addressing format is selected), if the upper 7 bits of SAR match the upper 7 bits of the first frame received after a start condition, the chip operates as the slave device specified by the master device. SAR is assigned to the same address as ICMR, and can be written and read only when the ICE bit is cleared to 0 in ICCR.

SAR is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 1—Slave Address (SVA6 to SVA0): Set a unique address in bits SVA6 to SVA0, differing from the addresses of other slave devices connected to the I²C bus.

Bit 0—Format Select (FS): Used together with the FSX bit in SARX and the SW bit in DDCSWR to select the communication format.

- I²C bus format: addressing format with acknowledge bit
- Synchronous serial format: non-addressing format without acknowledge bit, for master mode only
- Formatless mode (channel 0 only): non-addressing format with or without acknowledge bit, slave mode only, start/stop conditions not detected

The FS bit also specifies whether or not SAR slave address recognition is performed in slave mode.

16.3.11 Initialization of Internal State

The IIC has a function for forcible initialization of its internal state if a deadlock occurs during communication.

Initialization is executed by (1) setting bits CLR3 to CLR0 in the DDCSWR register or (2) clearing the ICE bit. For details of settings for bits CLR3 to CLR0, see section 16.2.8, DDC Switch Register (DDCSWR).

Scope of Initialization:
The initialization executed by this function covers the following items:

- TDRE and RDRF internal flags
- Transmit/receive sequencer and internal operating clock counter
- Internal latches for retaining the output state of the SCL and SDA pins (wait, clock, data output, etc.)

The following items are not initialized:

- Actual register values (ICDR, SAR, SARX, ICMR, ICCR, ICSR, DDCSWR, STCR)
- Internal latches used to retain register read information for setting/clearing flags in the ICMR, ICCR, ICSR, and DDCSWR registers
- The value of the ICMR register bit counter (BC2 to BC0)
- Generated interrupt sources (interrupt sources transferred to the interrupt controller)

Notes on Initialization:
- Interrupt flags and interrupt sources are not cleared, and so flag clearing measures must be taken as necessary.
- Basically, other register flags are not cleared either, and so flag clearing measures must be taken as necessary.
- When initialization is performed by means of the DDCSWR register, the write data for bits CLR3 to CLR0 is not retained. To perform IIC clearance, bits CLR3 to CLR0 must be written to simultaneously using an MOV instruction. Do not use a bit-manipulation instruction such as BCLR. Similarly, when clearing is required again, all the bits must be written to simultaneously in accordance with the setting.
- If a flag clearing setting is made during transmission/reception, the IIC module will stop transmitting/receiving at that point and the SCL and SDA pins will be released. When transmission/reception is started again, register initialization, etc., must be carried out as necessary to enable correct communication as a system.

17.1.3 Input/Output Pins

Table 17.1 lists the input/output pins used by the keyboard buffer controller.

Table 17.1 Keyboard Buffer Controller Input/Output Pins

Channel	Name	Abbreviation*	I/O	Function
0	KBC clock I/O pin (KCLK0)	PS2AC	I/O	KBC clock input/output
	KBC data I/O pin (KD0)	PS2AD	I/O	KBC data input/output
1	KBC clock I/O pin (KCLK1)	PS2BC	I/O	KBC clock input/output
	KBC data I/O pin (KD1)	PS2BD	I/O	KBC data input/output
2	KBC clock I/O pin (KCLK2)	PS2CC	I/O	KBC clock input/output
	KBC data I/O pin (KD2)	PS2CD	I/O	KBC data input/output

Note: * These are the external I/O pin names. In the text, clock I/O pins are referred to as KCLK and data I/O pins as KD, omitting the channel designations.

17.1.4 Register Configuration

Table 17.2 lists the registers of the keyboard buffer controller.

Table 17.2 Keyboard Buffer Controller Registers

Channel	Name	Abbreviation	R/W	Initial Value	Address*1
0	Keyboard control register H	KBCRH0	R/(W)*2	H'70	H'FED8
	Keyboard control register L	KBCRL0	R/W	H'70	H'FED9
	Keyboard data buffer register	KBBR0	R	H'00	H'FEDA
1	Keyboard control register H	KBCRH1	R/(W)*2	H'70	H'FEDC
	Keyboard control register L	KBCRL1	R/W	H'70	H'FEDD
	Keyboard data buffer register	KBBR1	R	H'00	H'FEDE
2	Keyboard control register H	KBCRH2	R/(W)*2	H'70	H'FEE0
	Keyboard control register L	KBCRL2	R/W	H'70	H'FEE1
	Keyboard data buffer register	KBBR2	R	H'00	H'FEE2
Common	Module stop control register	MSTPCRH	R/W	H'3F	H'FF86
		MSTPCRL	R/W	H'FF	H'FF87

Notes: 1. Lower 16 bits of the address.
2. Only 0 can be written in bits 2 and 1, to clear the flags.

Section 18 Host Interface

Provided in the H8S/2148 Group and H8S/2147N; not provided in the H8S/2144 Group.

18.1 Overview

The H8S/2148 Group and H8S/2147N have an on-chip host interface (HIF) that enables connection to an ISA bus, widely used as the internal bus in personal computers. The host interface provides a four-channel parallel interface between the on-chip CPU and a host processor. The host interface is available only when the HI12E bit is set to 1 in SYSCR2. This mode is called slave mode, because it is designed for a master-slave communication system in which the H8S/2148 Group and H8S/2147N chip is slaved to a host processor.

18.1.1 Features

The features of the host interface are summarized below.

The host interface consists of 8-byte data registers, 4-byte status registers, a 2-byte control register, fast A20 gate logic, and a host interrupt request circuit. Communication is carried out via seven control signals from the host processor ($\overline{CS1}$, $\overline{CS2}$ or $\overline{ECS2}$, $\overline{CS3}$, $\overline{CS4}$, HA0, $\overline{IOR}$, and $\overline{IOW}$), six output signals to the host processor (GA20, HIRQ1, HIRQ11, HIRQ12, HIRQ3, and HIRQ4), and an 8-bit bidirectional command/data bus (HDB7 to HDB0). The $\overline{CS1}$, $\overline{CS2}$ (or $\overline{ECS2}$), $\overline{CS3}$, and $\overline{CS4}$ signals select one of the four interface channels.

20.2.3 A/D Control Register (ADCR)

Bit	7	6	5	4	3	2	1	0
	TRGS1	TRGS0	—	—	—	—	—	—
Initial value	0	0	1	1	1	1	1	1
Read/Write	R/W	R/W	—	—	—	—	—	—

ADCR is an 8-bit readable/writable register that enables or disables external triggering of A/D conversion operations.

ADCR is initialized to H'3F by a reset, and in standby mode, watch mode, subactive mode, subsleep mode, and module stop mode.

Bits 7 and 6—Timer Trigger Select 1 and 0 (TRGS1, TRGS0): These bits select enabling or disabling of the start of A/D conversion by a trigger signal. Only set bits TRGS1 and TRGS0 while conversion is stopped.

Bit 7	Bit 6		
TRGS1	**TRGS0**	**Description**	
0	0	Start of A/D conversion by external trigger is disabled	(Initial value)
	1	Start of A/D conversion by external trigger is disabled	
1	0	Start of A/D conversion by external trigger (8-bit timer) is enabled	
	1	Start of A/D conversion by external trigger pin is enabled	

Bits 5 to 0—Reserved: Should always be written with 1.

Note: Some of these bits are readable/writable in products other than the HD64F2148, HD64F2147N, HD64F2144, HD64F2142R and HD6432142, however, when writing, be sure to write 1 here for software compatibility.

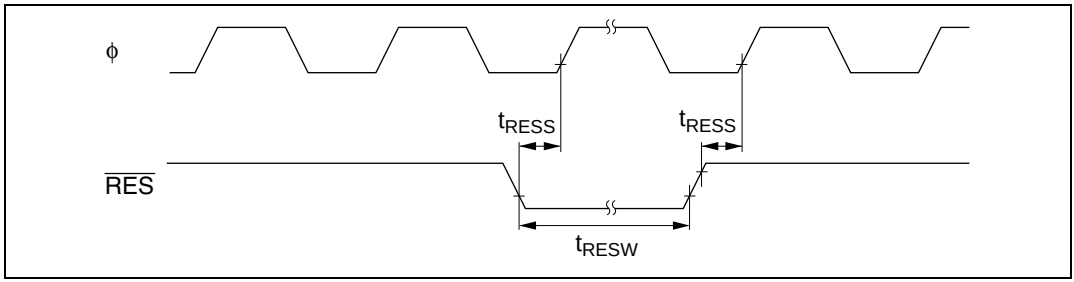


Figure 26.8 Reset Input Timing

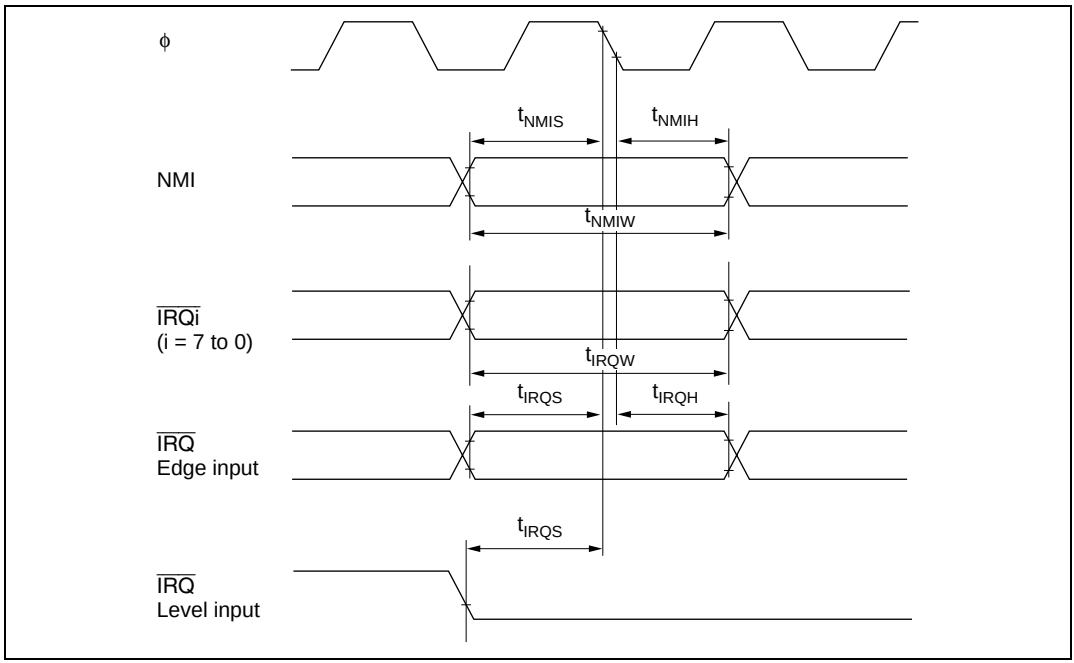


Figure 26.9 Interrupt Input Timing

TCSRX—Timer Control/Status Register X H'FFF1 TMRX

TCSRX

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	ICF	OS3	OS2	OS1	OS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W

Output select 1 and 0

0	0	No change at compare match A
	1	0 output at compare match A
1	0	1 output at compare match A
	1	Output inverted at compare match A (toggle output)

Output select 3 and 2

0	0	No change at compare match B
	1	0 output at compare match B
1	0	1 output at compare match B
	1	Output inverted at compare match B (toggle output)

Input capture flag

0	[Clearing condition] When 0 is written in ICF after reading ICF = 1
1	[Setting condition] When a rising edge followed by a falling edge is detected in the external reset signal after the ICST bit in TCONRI has been set to 1

Timer overflow flag

0	[Clearing condition] When 0 is written in OVF after reading OVF = 1
1	[Setting condition] When TCNT overflows from H'FF to H'00

Compare match flag A

0	[Clearing conditions] • When 0 is written in CMFA after reading CMFA = 1 • When the DTC is activated by a CMIA interrupt
1	[Setting condition] When TCNT = TCORA

Compare match flag B

0	[Clearing conditions] • When 0 is written in CMFB after reading CMFB = 1 • When the DTC is activated by a CMIB interrupt
1	[Setting condition] When TCNT = TCORB

Note: * Only 0 can be written in bits 7 to 4, to clear the flags.

TCONRI—Timer Connection Register I **H'FFFC** **Timer Connection**

Bit	7	6	5	4	3	2	1	0
	SIMOD1	SIMOD0	SCONE	ICST	HFINV	VFINV	HIINV	VIINV
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Input synchronization signal inversion

0	The VSYNCI pin state is used directly as the VSYNCI input
1	The VSYNCI pin state is inverted before use as the VSYNCI input

Input synchronization signal inversion

0	The HSYNCI and CSYNCI pin states are used directly as the HSYNCI and CSYNCI inputs
1	The HSYNCI and CSYNCI pin states are inverted before use as the HSYNCI and CSYNCI inputs

Input synchronization signal inversion

0	The VFBACKI pin state is used directly as the VFBACKI input
1	The VFBACKI pin state is inverted before use as the VFBACKI input

Input synchronization signal inversion

0	The HFBACKI pin state is used directly as the HFBACKI input
1	The HFBACKI pin state is inverted before use as the HFBACKI input

Input capture start bit

0	The TICRR and TICRF input capture functions are stopped [Clearing condition] When a rising edge followed by a falling edge is detected on TMRIX
1	The TICRR and TICRF input capture functions are operating (Waiting for detection of a rising edge followed by a falling edge on TMRIX) [Setting condition] When 1 is written in ICST after reading ICST = 0

Synchronization signal connection enable

SCONE	Mode	FTIA	FTIB	FTIC	FTID	TMCI1	TMRI1
0	Normal connection	FTIA input	FTIB input	FTIC input	FTID input	TMCI1 input	TMRI1 input
1	Synchronization signal connection mode	IVI signal	TMO1 signal	VFBACKI input	IHI signal	IHI signal	IVI inverse signal

Input synchronization mode select 1 and 0

SIMOD1	SIMOD0	Mode	IHI signal	IVI signal
0	0	No signal	HFBACKI input	VFBACKI input
	1	S-on-G mode	CSYNCI input	PDC input
1	0	Composite mode	HSYNCI input	PDC input
	1	Separate mode	HSYNCI input	VSYNCI input

C.9 Port 9 Block Diagrams

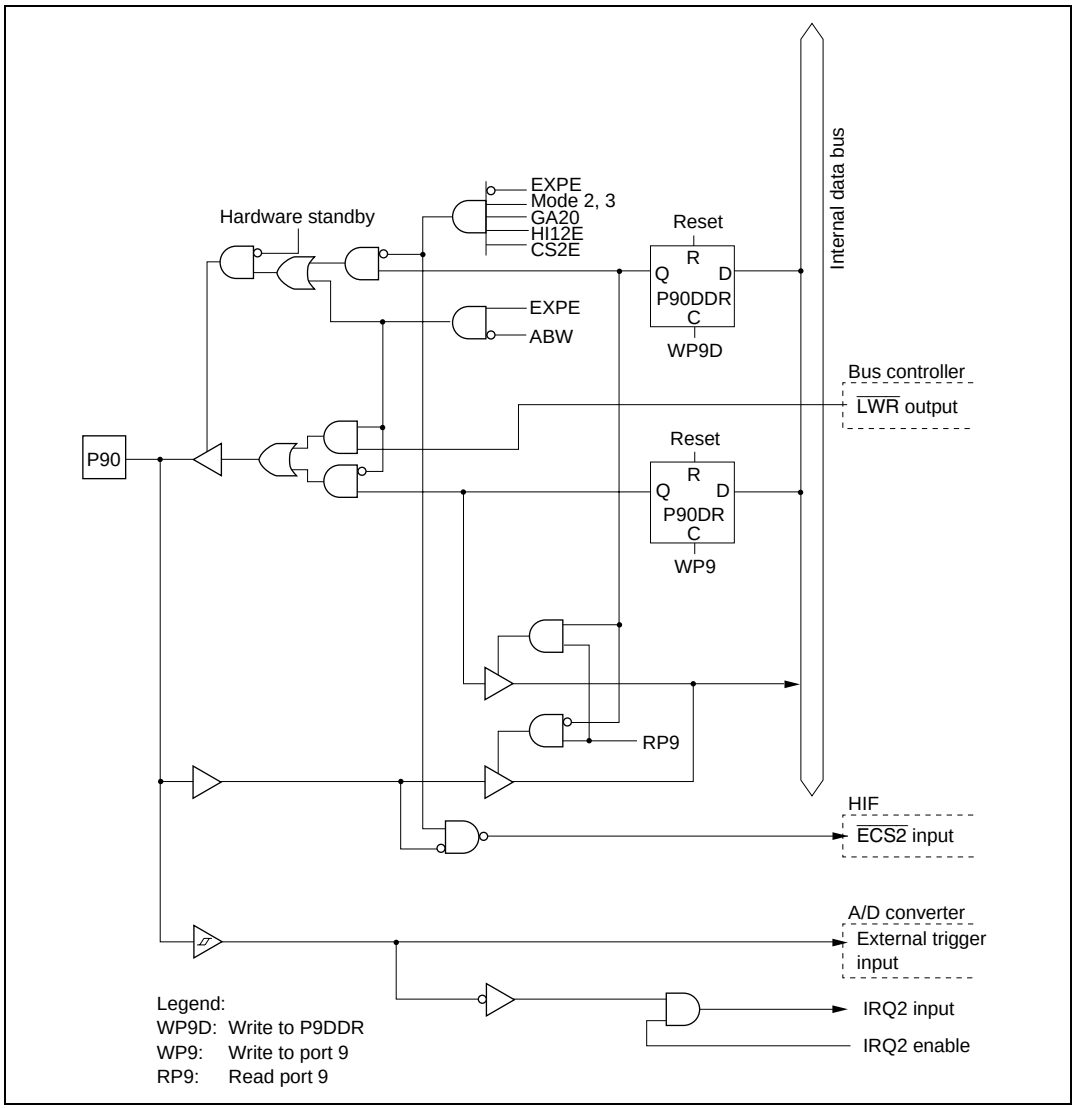


Figure C.29 Port 9 Block Diagram (Pin P90)