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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2144avte10v

8.3.3 Pin Functions in Each Mode

Mode 1

In mode 1, port 2 pins automatically function as address outputs. The port 2 pin functions are shown in figure 8.6.

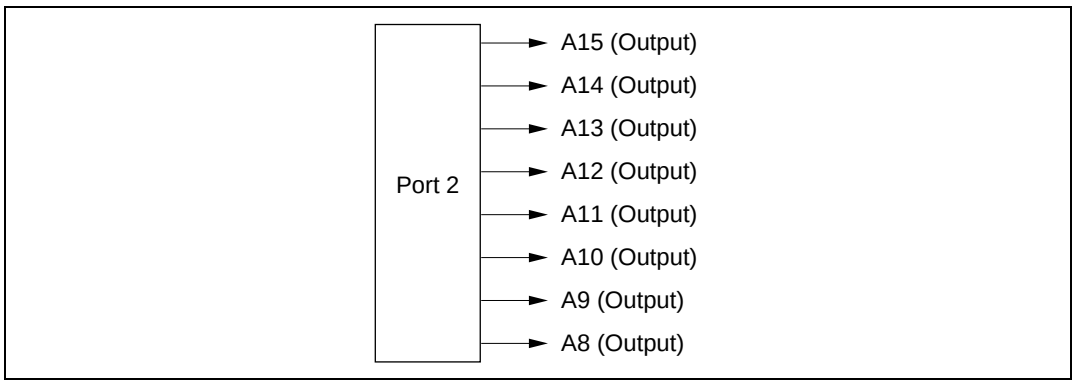

Figure 8.6 Port 2 Pin Functions (Mode 1)

Modes 2 and 3 (EXPE = 1)

In modes 2 and 3 (when EXPE = 1), port 2 pins function as address outputs, PWM outputs, or I/O ports, and input or output can be specified on a bit-by-bit basis. When a bit in P2DDR is set to 1, the corresponding pin functions as an address output or PWM output, and when cleared to 0, as an input port. P27 to P24 are switched from address outputs to output ports by setting the IOSE bit to 1. P27 can be used as an on-chip supporting module output pin regardless of the P27DDR setting, but to ensure normal access to external space, P27 should not be set as an on-chip supporting module output pin when port 2 pins are used as address output pins.

The port 2 pin functions are shown in figure 8.7.

8.4.3 Pin Functions in Each Mode

Modes 1, 2, and 3 (EXPE = 1)

In modes 1, 2, and 3 (when EXPE = 1), port 3 pins automatically function as data I/O pins. The port 3 pin functions are shown in figure 8.10.

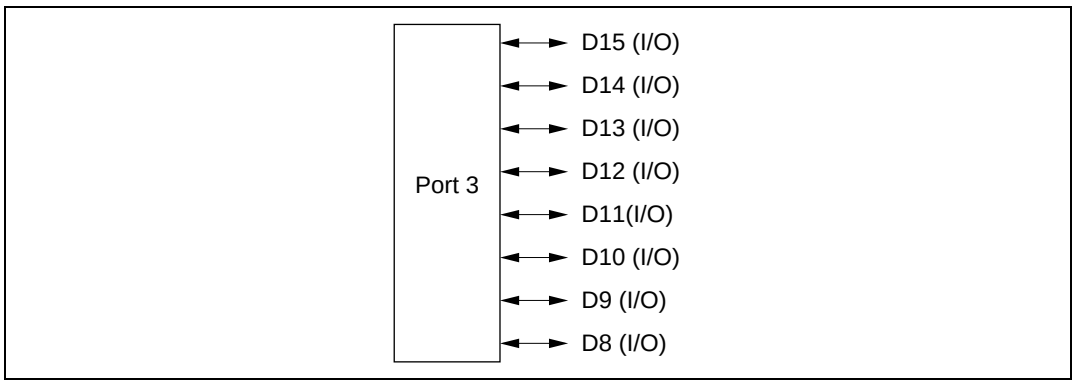

Figure 8.10 Port 3 Pin Functions (Modes 1, 2, and 3 (EXPE = 1))

Modes 2 and 3 (EXPE = 0)

In modes 2 and 3 (when EXPE = 0), port 3 functions as host interface data bus I/O pins (HDB7 to HDB0) or as I/O ports. When the HI12E bit is set to 1 in SYSCR2 and a transition is made to slave mode, port 3 functions as the host interface data bus. In slave mode, P3DR and P3DDR should be cleared to H'00. When the HI12E bit is cleared to 0, port 3 functions as an I/O port, and input or output can be specified on a bit-by-bit basis. When a bit in P3DDR is set to 1, the corresponding pin functions as an output port, and when cleared to 0, as an input port.

The port 3 pin functions are shown in figure 8.11.

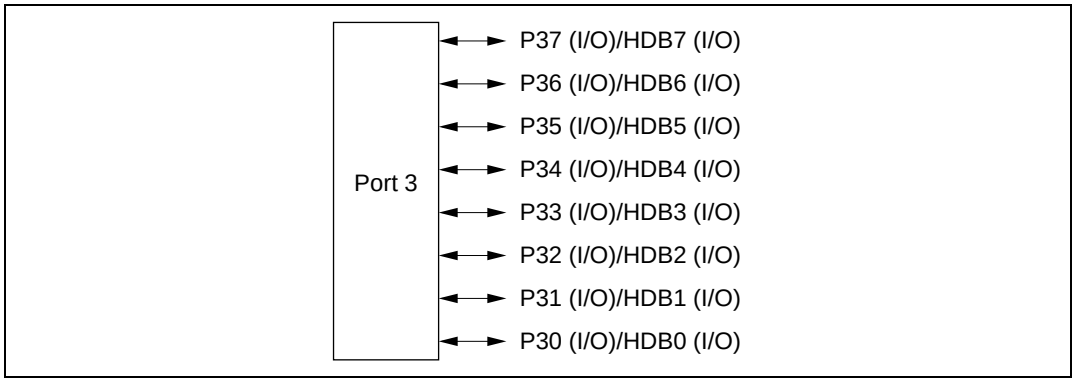

Figure 8.11 Port 3 Pin Functions (Modes 2 and 3 (EXPE = 0))

8.4.4 MOS Input Pull-Up Function

Port 3 has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 2 and 3 (when EXPE = 0), and can be specified as on or off on a bit-by-bit basis.

When a P3DDR bit is cleared to 0 in mode 2 or 3 (when EXPE = 0), setting the corresponding P3PCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 8.9 summarizes the MOS input pull-up states.

Table 8.9 MOS Input Pull-Up States (Port 3)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 3 (EXPE = 1)	Off	Off	Off	Off
2, 3 (EXPE = 0)	Off	Off	On/Off	On/Off

Legend:
Off: MOS input pull-up is always off.
On/Off: On when P3DDR = 0 and P3PCR = 1; otherwise off.

If automatic addition of OCRAR/OCRAF to OCRA is selected, and a compare-match occurs in the cycle following the OCRA, OCRAR and OCRAF write cycle, the OCRA, OCRAR and OCRAF write takes priority and the compare-match signal is inhibited. Consequently, the result of the automatic addition is not written to OCRA.

Figure 11.21 shows this type of contention.

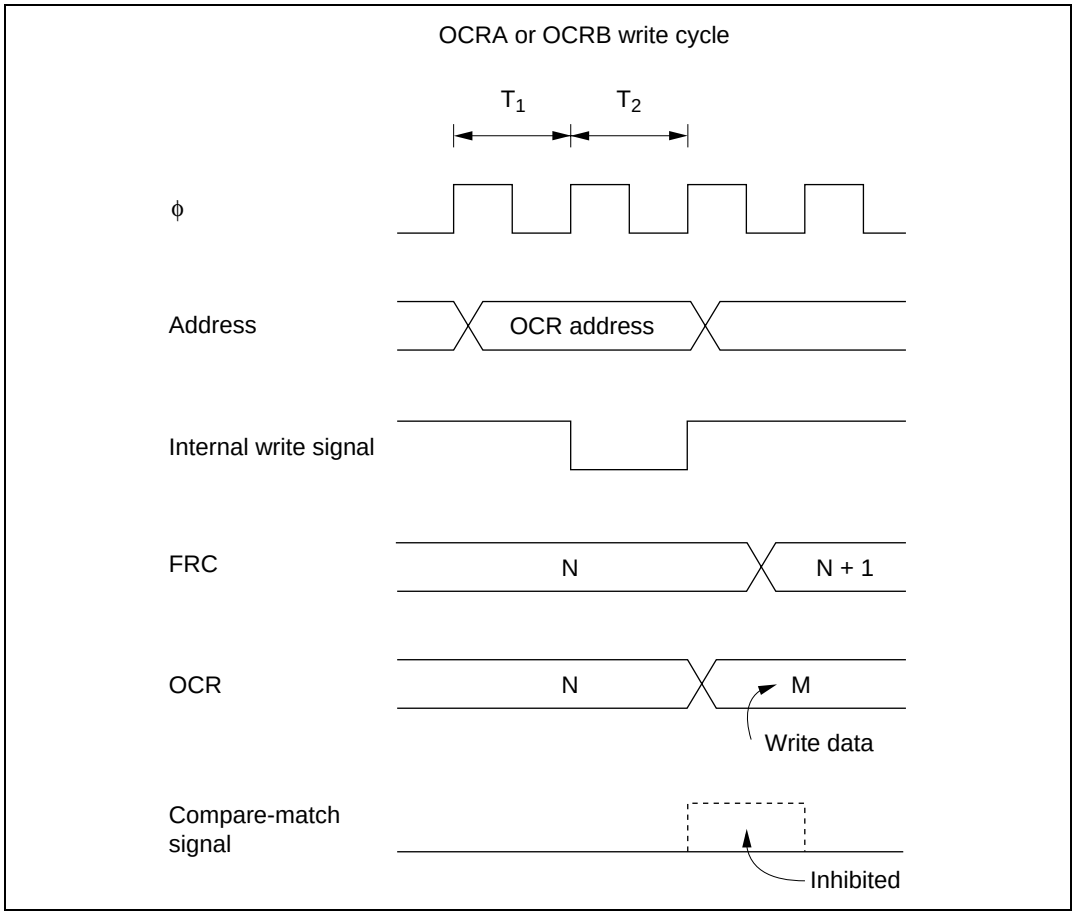

Figure 11.20 Contention between OCR Write and Compare-Match (When Automatic Addition Function Is Not Used)

Bit 1

IRIC	Description
0	Waiting for transfer, or transfer in progress (Initial value) [Clearing conditions] 1. When 0 is written in IRIC after reading IRIC = 1 2. When ICDR is written or read by the DTC (When the TDRE or RDRF flag is cleared to 0) (This is not always a clearing condition; see the description of DTC operation for details)
1	Interrupt requested [Setting conditions] • I²C bus format master mode 1. When a start condition is detected in the bus line state after a start condition is issued (when the TDRE flag is set to 1 because of first frame transmission) 2. When a wait is inserted between the data and acknowledge bit when WAIT = 1 3. At the end of data transfer (at the rise of the 9th transmit/receive clock pulse when no wait is inserted, (WAIT=0) and, when a wait is inserted (WAIT=1), at the fall of the 8th transmit/receive clock pulse) 4. When a slave address is received after bus arbitration is lost (when the AL flag is set to 1) 5. When 1 is received as the acknowledge bit when the ACKE bit is 1 (when the ACKB bit is set to 1) • I²C bus format slave mode 1. When the slave address (SVA, SVAX) matches (when the AAS and AASX flags are set to 1) and at the end of data transfer up to the subsequent retransmission start condition or stop condition detection (when the TDRE or RDRF flag is set to 1) 2. When the general call address is detected (when FS = 0 and the ADZ flag is set to 1) and at the end of data transfer up to the subsequent retransmission start condition or stop condition detection (when the TDRE or RDRF flag is set to 1) 3. When 1 is received as the acknowledge bit when the ACKE bit is 1 (when the ACKB bit is set to 1) 4. When a stop condition is detected (when the STOP or ESTP flag is set to 1) • Synchronous serial format, and formatless mode 1. At the end of data transfer (when the TDRE or RDRF flag is set to 1) 2. When a start condition is detected with serial format selected 3. When the SW bit is set to 1 in DDCSWR Except the above, when the conditions to set the TDRE or RDRF internal flag to 1 is generated

Bit 7—Error Stop Condition Detection Flag (ESTP): Indicates that a stop condition has been detected during frame transfer in I²C bus format slave mode.

Bit 7

ESTP	Description	
0	No error stop condition [Clearing conditions] 1. When 0 is written in ESTP after reading ESTP = 1 2. When the IRIC flag is cleared to 0	(Initial value)
1	• In I²C bus format slave mode Error stop condition detected [Setting condition] When a stop condition is detected during frame transfer • In other modes No meaning	

Bit 6—Normal Stop Condition Detection Flag (STOP): Indicates that a stop condition has been detected after completion of frame transfer in I²C bus format slave mode.

Bit 6

STOP	Description	
0	No normal stop condition [Clearing conditions] 1. When 0 is written in STOP after reading STOP = 1 2. When the IRIC flag is cleared to 0	(Initial value)
1	• In I²C bus format slave mode Normal stop condition detected [Setting condition] When a stop condition is detected after completion of frame transfer • In other modes No meaning	

Bit 5—I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag (IRTR): Indicates that the I²C bus interface has issued an interrupt request to the CPU, and the source is completion of reception/transmission of one frame in continuous transmission/reception for which DTC activation is possible. When the IRTR flag is set to 1, the IRIC flag is also set to 1 at the same time.

Bit 3—Arbitration Lost (AL): This flag indicates that arbitration was lost in master mode. The I²C bus interface monitors the bus. When two or more master devices attempt to seize the bus at nearly the same time, if the I²C bus interface detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been taken by another master.

AL is cleared by reading AL after it has been set to 1, then writing 0 in AL. In addition, AL is reset automatically by write access to ICDR in transmit mode, or read access to ICDR in receive mode.

Bit 3

AL	Description
0	Bus arbitration won (Initial value) [Clearing conditions] 1. When ICDR data is written (transmit mode) or read (receive mode) 2. When 0 is written in AL after reading AL = 1
1	Arbitration lost [Setting conditions] 1. If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode 2. If the internal SCL line is high at the fall of SCL in master transmit mode

Bit 2—Slave Address Recognition Flag (AAS): In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or if the general call address (H'00) is detected.

AAS is cleared by reading AAS after it has been set to 1, then writing 0 in AAS. In addition, AAS is reset automatically by write access to ICDR in transmit mode, or read access to ICDR in receive mode.

16.3.7 Automatic Switching from Formatless Mode to I²C Bus Format

Setting the SW bit to 1 in DDCSWR enables formatless mode to be selected as the IIC0 operating mode. Switching from formatless mode to the I²C bus format (slave mode) is performed automatically when a falling edge is detected on the SCL pin.

The following four preconditions are necessary for this operation:

- A common data pin (SDA) for formatless and I²C bus format operation
- Separate clock pins for formatless operation (VSYNCI) and I²C bus format operation (SCL)
- A fixed 1 level for the SCL pin during formatless operation (the SCL pin does not output a low level)
- Settings of bits other than TRS in ICCR that allow I²C bus format operation

Automatic switching is performed from formatless mode to the I²C bus format when the SW bit in DDCSWR is automatically cleared to 0 on detection of a falling edge on the SCL pin. Switching from the I²C bus format to formatless mode is achieved by having software set the SW bit in DDCSWR to 1.

In formatless mode, bits (such as MSL and TRS) that control the I²C bus interface operating mode must not be modified. When switching from the I²C bus format to formatless mode, set the TRS bit to 1 or clear it to 0 according to the transmit data (transmission or reception) in formatless mode, then set the SW bit to 1. After automatic switching from formatless mode to the I²C bus format (slave mode), in order to wait for slave address reception, the TRS bit is automatically cleared to 0.

If a falling edge is detected on the SCL pin during formatless operation, the I²C bus interface operating mode is switched to the I²C bus format without waiting for a stop condition to be detected.

Section 20 A/D Converter

20.1 Overview

This LSI incorporate a 10-bit successive-approximations A/D converter that allows up to eight analog input channels to be selected.

In addition to the eight analog input channels, up to 16 channels of digital input can be selected for A/D conversion. Since the conversion precision falls when digital input is selected, digital input is ideal for use by a comparator identifying multi-valued inputs, for example.

20.1.1 Features

A/D converter features are listed below.

- 10-bit resolution
- Eight (analog) or 16 (digital) input channels
- Settable analog conversion voltage range
  - The analog conversion voltage range is set using the reference power supply voltage pin (AVref) as the analog reference voltage
- High-speed conversion
  - Minimum conversion time: 6.7 µs per channel (at 20-MHz operation)
- Choice of single mode or scan mode
  - Single mode: Single-channel A/D conversion
  - Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  - Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Three kinds of conversion start
  - Choice of software or timer conversion start trigger (8-bit timer), or $\overline{\text{ADTRG}}$ pin
- A/D conversion end interrupt generation
  - An A/D conversion end interrupt (ADI) request can be generated at the end of A/D conversion

Table 22.11 Settings for Each Operating Mode in Programmer Mode

	Pin Names				
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**FO0 to FO7**	**FA0 to FA17**
Read	L	L	H	Data output	Ain
Output disable	L	H	H	Hi-Z	X
Command write	L	H	L	Data input	Ain*2
Chip disable*1	H	X	X	Hi-Z	X

Notes: 1. Chip disable is not a standby state; internally, it is an operation state.
2. Ain indicates that there is also address input in auto-program mode.

Table 22.12 Programmer Mode Commands

	Number	1st Cycle			2nd Cycle		
Command Name	**of Cycles**	**Mode**	**Address**	**Data**	**Mode**	**Address**	**Data**
Memory read mode	1 + n	Write	X	H'00	Read	RA	Dout
Auto-program mode	129	Write	X	H'40	Write	WA	Din
Auto-erase mode	2	Write	X	H'20	Write	X	H'20
Status read mode	2	Write	X	H'71	Write	X	H'71

Notes: 1. In auto-program mode, 129 cycles are required for command writing by a simultaneous 128-byte write.
2. In memory read mode, the number of cycles depends on the number of address write cycles (n).

22.10.4 Memory Read Mode

- After the end of an auto-program, auto-erase, or status read operation, the command wait state is entered. To read memory contents, a transition must be made to memory read mode by means of a command write before the read is executed.
- Command writes can be performed in memory read mode, just as in the command wait state.
- Once memory read mode has been entered, consecutive reads can be performed.
- After power-on, memory read mode is entered.

24.4 Duty Adjustment Circuit

When the oscillator frequency is 5 MHz or higher, the duty adjustment circuit adjusts the duty cycle of the clock signal from the oscillator to generate the system clock (ϕ).

24.5 Medium-Speed Clock Divider

The medium-speed clock divider divides the system clock to generate ϕ/2, ϕ/4, ϕ/8, ϕ/16, and ϕ/32 clocks.

24.6 Bus Master Clock Selection Circuit

The bus master clock selection circuit selects the system clock (ϕ) or one of the medium-speed clocks (ϕ/2, ϕ/4, ϕ/8, ϕ/16, or ϕ/32) to be supplied to the bus master, according to the settings of bits SCK2 to SCK0 in SBYCR.

24.7 Subclock Input Circuit

The subclock input circuit controls the subclock input from the EXCL pin.

Inputting the Subclock

When a subclock is used, a 32.768 kHz external clock should be input from the EXCL pin. In this case, clear bit P96DDR to 0 in P9DDR and set bit EXCLE to 1 in LPWRCR.

The subclock input conditions are shown in table 24.6 and figure 24.8.

Table 24.6 Subclock Input Conditions

		V_{cc} = 2.7 to 5.5 V				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Subclock input low pulse width	t_{EXCLL}	—	15.26	—	µs	Figure 24.8
Subclock input high pulse width	t_{EXCLH}	—	15.26	—	µs	
Subclock input rise time	t_{EXCLr}	—	—	10	ns	
Subclock input fall time	t_{EXCLf}	—	—	10	ns	

(2) Control Signal Timing

Table 26.21 shows the control signal timing. The only external interrupts that can operate on the subclock (φ = 32.768 kHz) are NMI and IRQ0, 1, 2, 6, and 7.

Table 26.21 Control Signal Timing

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, φ = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, φ = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 3.6 V, $V_{CC}B$ = 2.7 V to 5.5 V, V_{SS} = 0 V, φ = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C

		Condition A		Condition B		Condition C			
		20 MHz		16 MHz		10 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	300	—	ns	Figure 26.8
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	20	—	t_{cyc}	
NMI setup time (NMI)	t_{NMIS}	150	—	150	—	250	—	ns	Figure 26.9
NMI hold time (NMI)	t_{NMIH}	10	—	10	—	10	—		
NMI pulse width (exiting software standby mode)	t_{NMIW}	200	—	200	—	200	—	ns	
IRQ setup time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQS}	150	—	150	—	250	—	ns	
IRQ hold time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQH}	10	—	10	—	10	—	ns	
IRQ pulse width ($\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ2}$ to $\overline{IRQ0}$) (exiting software standby mode)	t_{IRQW}	200	—	200	—	200	—	ns	

Table 26.29 Flash Memory Characteristics (Programming/erasing operating range)

Conditions (5 V version): V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)
(3 V version): V_{CC} = 3.0 V to 3.6V, V_{SS} = 0 V, T_a = –20 to 75°C

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Programming time*1 *2 *4		tP	—	10	200	ms/ 128 bytes	
Erase time*1 *3 *6		tE	—	100	1200	ms/ block	
Reprogramming count		N_{WEC}	100*8	10000*9	—	Times	
Data retention time*10		t_{DRP}	10	—	—	Years	
Programming	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after PSU-bit setting*1	y	50	—	—	µs	
	Wait time after P-bit setting*1 *4	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional writing
	Wait time after P-bit clear*1	α	5	—	—	µs	
	Wait time after PSU-bit clear*1	β	5	—	—	µs	
	Wait time after PV-bit setting*1	γ	4	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after PV-bit clear*1	η	2	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum programming count*1 *4 *5	N	—	—	1000	Times	
Erase	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after ESU-bit setting*1	y	100	—	—	µs	
	Wait time after E-bit setting*1 *6	z	10	—	100	ms	
	Wait time after E-bit clear*1	α	10	—	—	µs	
	Wait time after ESU-bit clear*1	β	10	—	—	µs	
	Wait time after EV-bit setting*1	γ	20	—	—	µs	
	Wait time after H'FF dummy write*1	ε	2	—	—	µs	
	Wait time after EV-bit clear*1	η	4	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum erase count*1 *6 *7	N	—	—	120	Times	

Mnemonic		Size	Addressing Mode and Instruction Length (Bytes)										Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d,ERn)	@-ERn/@ERn+	@aa	@(d,PC)	@@aa				I	H	N	Z	V	C	Normal	Advanced
BTST	BTST #xx:3,Rd	B		2									¬ (#xx:3 of Rd8)→Z	—	—	—	↕	—	—	1	
	BTST #xx:3,@ERd	B			4								¬ (#xx:3 of @ERd)→Z	—	—	—	↕	—	—	3	
	BTST #xx:3,@aa:8	B						4					¬ (#xx:3 of @aa:8)→Z	—	—	—	↕	—	—	3	
	BTST #xx:3,@aa:16	B						6					¬ (#xx:3 of @aa:16)→Z	—	—	—	↕	—	—	4	
	BTST #xx:3,@aa:32	B						8					¬ (#xx:3 of @aa:32)→Z	—	—	—	↕	—	—	5	
	BTST Rn,Rd	B		2									¬ (Rn8 of Rd8)→Z	—	—	—	↕	—	—	1	
	BTST Rn,@ERd	B			4								¬ (Rn8 of @ERd)→Z	—	—	—	↕	—	—	3	
	BTST Rn,@aa:8	B						4					¬ (Rn8 of @aa:8)→Z	—	—	—	↕	—	—	3	
	BTST Rn,@aa:16	B						6					¬ (Rn8 of @aa:16)→Z	—	—	—	↕	—	—	4	
	BTST Rn,@aa:32	B						8					¬ (Rn8 of @aa:32)→Z	—	—	—	↕	—	—	5	
BLD	BLD #xx:3,Rd	B		2									(#xx:3 of Rd8)→C	—	—	—	—	—	↕	1	
	BLD #xx:3,@ERd	B			4								(#xx:3 of @ERd)→C	—	—	—	—	—	↕	3	
	BLD #xx:3,@aa:8	B						4					(#xx:3 of @aa:8)→C	—	—	—	—	—	↕	3	
	BLD #xx:3,@aa:16	B						6					(#xx:3 of @aa:16)→C	—	—	—	—	—	↕	4	
	BLD #xx:3,@aa:32	B						8					(#xx:3 of @aa:32)→C	—	—	—	—	—	↕	5	
BILD	BILD #xx:3,Rd	B		2									¬ (#xx:3 of Rd8)→C	—	—	—	—	—	↕	1	
	BILD #xx:3,@ERd	B			4								¬ (#xx:3 of @ERd)→C	—	—	—	—	—	↕	3	
	BILD #xx:3,@aa:8	B						4					¬ (#xx:3 of @aa:8)→C	—	—	—	—	—	↕	3	
	BILD #xx:3,@aa:16	B						6					¬ (#xx:3 of @aa:16)→C	—	—	—	—	—	↕	4	
	BILD #xx:3,@aa:32	B						8					¬ (#xx:3 of @aa:32)→C	—	—	—	—	—	↕	5	
BST	BST #xx:3,Rd	B		2									C→(#xx:3 of Rd8)	—	—	—	—	—	—	1	
	BST #xx:3,@ERd	B			4								C→(#xx:3 of @ERd)	—	—	—	—	—	—	4	
	BST #xx:3,@aa:8	B						4					C→(#xx:3 of @aa:8)	—	—	—	—	—	—	4	
	BST #xx:3,@aa:16	B						6					C→(#xx:3 of @aa:16)	—	—	—	—	—	—	5	
	BST #xx:3,@aa:32	B						8					C→(#xx:3 of @aa:32)	—	—	—	—	—	—	6	
BIST	BIST #xx:3,Rd	B		2									¬ C→(#xx:3 of Rd8)	—	—	—	—	—	—	1	
	BIST #xx:3,@ERd	B			4								¬ C→(#xx:3 of @ERd)	—	—	—	—	—	—	4	
	BIST #xx:3,@aa:8	B						4					¬ C→(#xx:3 of @aa:8)	—	—	—	—	—	—	4	
	BIST #xx:3,@aa:16	B						6					¬ C→(#xx:3 of @aa:16)	—	—	—	—	—	—	5	
	BIST #xx:3,@aa:32	B						8					¬ C→(#xx:3 of @aa:32)	—	—	—	—	—	—	6	

Lower Address	Register Name	H8S/2148 Group Register Selection Conditions		H8S/2147N Register Selection Conditions		H8S/2144 Group Register Selection Conditions		Module Name
H'FF94	OCRAH	MSTP13 = 0	OCRS = 0 in TOCR	MSTP13 = 0	OCRS = 0 in TOCR	MSTP13 = 0	OCRS = 0 in TOCR	FRT
	OCRBH		OCRS = 1 in TOCR		OCRS = 1 in TOCR		OCRS = 1 in TOCR	
H'FF95	OCRAL		OCRS = 0 in TOCR		OCRS = 0 in TOCR		OCRS = 0 in TOCR	
	OCRBL		OCRS = 1 in TOCR		OCRS = 1 in TOCR		OCRS = 1 in TOCR	
H'FF96	TCR							
H'FF97	TOCR							
H'FF98	ICRAH		ICRS = 0 in TOCR		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRARH		ICRS = 1 in TOCR		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF99	ICRAL		ICRS = 0 in TOCR		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRARL		ICRS = 1 in TOCR		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9A	ICRBH		ICRS = 0 in TOCR		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRAFH		ICRS = 1 in TOCR		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9B	ICRBL		ICRS = 0 in TOCR		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRAFL		ICRS = 1 in TOCR		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9C	ICRCH		ICRS = 0 in TOCR		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRDMH		ICRS = 1 in TOCR		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9D	ICRCL		ICRS = 0 in TOCR		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRDML		ICRS = 1 in TOCR		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9E	ICRDH							
H'FF9F	ICRDL							
H'FFA0	SMR2	MSTP5 = 0, IICE = 0 in STCR		MSTP5 = 0, IICE = 0 in STCR		MSTP5 = 0, IICE = 0 in STCR		SCI2
	DADRAH	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/ DADRB	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/ DADRB	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/ DADRB	PWMX
	DACR		REGS = 1 in DACNT/ DADRB		REGS = 1 in DACNT/ DADRB		REGS = 1 in DACNT/ DADRB	

KBCRL0—Keyboard Control Register L0 **H'FED9** **Keyboard Buffer Controller**
KBCRL1—Keyboard Control Register L1 **H'FEDD** **Keyboard Buffer Controller**
KBCRL2—Keyboard Control Register L2 **H'FEE1** **Keyboard Buffer Controller**

Bit	7	6	5	4	3	2	1	0
	KBE	KCLKO	KDO	—	RXCR3	RXCR2	RXCR1	RXCR0
Initial value	0	1	1	1	0	0	0	0
Read/Write	R/W	R/W	R/W	—	R	R	R	R

Receive counter

RXCR3	RXCR2	RXCR1	RXCR0	Receive data contents
0	0	0	0	—
			1	Start bit
		1	0	KB0
			1	KB1
	1	0	0	KB2
			1	KB3
		1	0	KB4
			1	KB5
1	0	0	0	KB6
			1	KB7
		1	0	Parity bit
			1	—
	1	—	—	—

Keyboard data out

0	Keyboard buffer controller data I/O pin is low
1	Keyboard buffer controller data I/O pin is high

Keyboard clock out

0	Keyboard buffer controller clock I/O pin is low
1	Keyboard buffer controller clock I/O pin is high

Keyboard enable

0	Loading of receive data into KBBR is disabled
1	Loading of receive data into KBBR is enabled

SMR1—Serial Mode Register 1 **H'FF88** **SCI1**
SMR2—Serial Mode Register 2 **H'FFA0** **SCI2**
SMR0—Serial Mode Register 0 **H'FFD8** **SCI0**

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock select 1 and 0

0	0	φ clock
	1	φ/4 clock
1	0	φ/16 clock
	1	φ/64 clock

Multiprocessor mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop bit length

0	1 stop bit
1	2 stop bits

Parity mode

0	Even parity
1	Odd parity

Parity enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted. Also, LSB-first/ MSB-first selection is not available.

Communication mode

0	Asynchronous mode
1	Synchronous mode

TCSR0—Timer Control/Status Register 0 H'FFCA TMR0

TCSR0

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W	R/W

Output select 1 and 0

0	0	No change at compare match A
	1	0 output at compare match A
1	0	1 output at compare match A
	1	Output inverted at compare match A (toggle output)

Output select 3 and 2

0	0	No change at compare match B
	1	0 output at compare match B
1	0	1 output at compare match B
	1	Output inverted at compare match B (toggle output)

A/D trigger enable

0	A/D converter start requests by compare match A are disabled
1	A/D converter start requests by compare match A are enabled

Timer overflow flag

0	[Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
1	[Setting condition] When TCNT overflows from H'FF to H'00

Compare match flag A

0	[Clearing conditions] • Read CMFA when CMFA = 1, then write 0 in CMFA • When the DTC is activated by a CMIA interrupt
1	[Setting condition] When TCNT = TCORA

Compare match flag B

0	[Clearing conditions] • Read CMFB when CMFB = 1, then write 0 in CMFB • When the DTC is activated by a CMIB interrupt
1	[Setting condition] When TCNT = TCORB

Note: * Only 0 can be written in bits 7 to 5, to clear the flags.

PWSL—PWM Register Select **H'FFD6** **PWM**

Bit	7	6	5	4	3	2	1	0
	PWCKE	PWCKS	—	—	RS3	RS2	RS1	RS0
Initial value	0	0	1	0	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

Register Select

0	0	0	0	PWDR0 selected
			1	PWDR1 selected
		1	0	PWDR2 selected
			1	PWDR3 selected
	1	0	0	PWDR4 selected
			1	PWDR5 selected
		1	0	PWDR6 selected
			1	PWDR7 selected
1	0	0	0	PWDR8 selected
			1	PWDR9 selected
		1	0	PWDR10 selected
			1	PWDR11 selected
	1	0	0	PWDR12 selected
			1	PWDR13 selected
		1	0	PWDR14 selected
			1	PWDR15 selected

PWM clock enable, PWM clock select

PWSL		PCSR		Description
Bit 7	Bit 6	Bit 2	Bit 1	
PWCKE	PWCKS	PWCKB	PWCKA	
0	—	—	—	Clock input disabled
1	0	—	—	ϕ (system clock) selected
	1	0	0	ϕ/2 selected
			1	ϕ/4 selected
		1	0	ϕ/8 selected
			1	ϕ/16 selected