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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

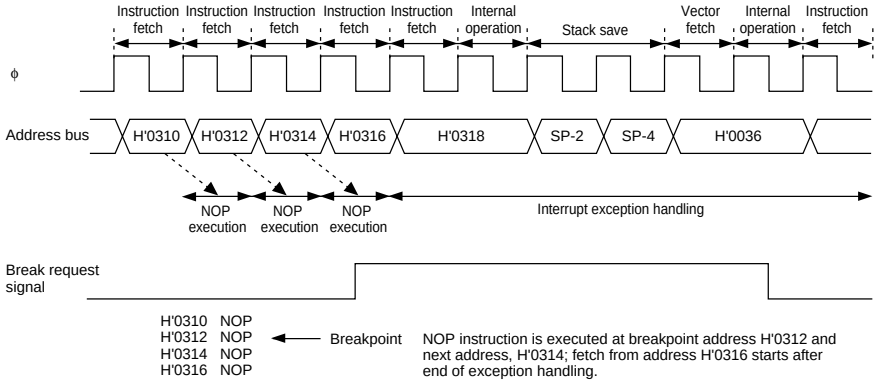
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8S/2000 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | IrDA, SCI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 74 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BFQFP |
| Supplier Device Package | 100-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df2144fa20iv |

| Pin No. | Pin Name | | | |
|---|---|---|---|---|
| | Expanded Modes | | Single-Chip Modes | |
| FP-100B TFP-100B | Mode 1 | Mode 2 (EXPE = 1) Mode 3 (EXPE = 1) | Mode 2 (EXPE = 0) Mode 3 (EXPE = 0) | Flash Memory Writer Mode |
| 22 | $\overline{RD}$ | $\overline{RD}$ | P93/$\overline{IOR}$ | $\overline{WE}$ |
| 23 | P92/$\overline{IRQ0}$ | P92/$\overline{IRQ0}$ | P92/$\overline{IRQ0}$ | VSS |
| 24 | P91/$\overline{IRQ1}$ | P91/$\overline{IRQ1}$ | P91/$\overline{IRQ1}$ | VCC |
| 25 | $\overline{LWR}$/P90/$\overline{IRQ2}$/ $\overline{ADTRG}$ | $\overline{LWR}$/P90/$\overline{IRQ2}$/ $\overline{ADTRG}$ | P90/$\overline{IRQ2}$/$\overline{ADTRG}$/ $\overline{ECS2}$ | VCC |
| 26 | P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI | P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI | P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI | NC |
| 27 | P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO | P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO | P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO | NC |
| 28 | P62/FTIA/CIN2/ $\overline{KIN2}$/TMIY/ VSYNCI | P62/FTIA/CIN2/ $\overline{KIN2}$/TMIY/ VSYNCI | P62/FTIA/CIN2/ $\overline{KIN2}$/TMIY/ VSYNCI | NC |
| 29 | P63/FTIB/CIN3/ $\overline{KIN3}$/VFBACKI | P63/FTIB/CIN3/ $\overline{KIN3}$/VFBACKI | P63/FTIB/CIN3/ $\overline{KIN3}$/VFBACKI | NC |
| 30 | PA3/CIN11/ $\overline{KIN11}$/PS2AD | A19/PA3/CIN11/ $\overline{KIN11}$/PS2AD | PA3/CIN11/ $\overline{KIN11}$/PS2AD | NC |
| 31 | PA2/CIN10/ $\overline{KIN10}$/PS2AC | A18/PA2/CIN10/ $\overline{KIN10}$/PS2AC | PA2/CIN10/ $\overline{KIN10}$/PS2AC | NC |
| 32 | P64/FTIC/CIN4/ $\overline{KIN4}$/CLAMPO | P64/FTIC/CIN4/ $\overline{KIN4}$/CLAMPO | P64/FTIC/CIN4/ $\overline{KIN4}$/CLAMPO | NC |
| 33 | P65/FTID/CIN5/ $\overline{KIN5}$ | P65/FTID/CIN5/ $\overline{KIN5}$ | P65/FTID/CIN5/ $\overline{KIN5}$ | NC |
| 34 | P66/FTOB/CIN6/ $\overline{KIN6}$/$\overline{IRQ6}$ | P66/FTOB/CIN6/ $\overline{KIN6}$/$\overline{IRQ6}$ | P66/FTOB/CIN6/ $\overline{KIN6}$/$\overline{IRQ6}$ | NC |
| 35 | P67/TMOX/CIN7/ $\overline{KIN7}$/$\overline{IRQ7}$ | P67/TMOX/CIN7/ $\overline{KIN7}$/$\overline{IRQ7}$ | P67/TMOX/CIN7/ $\overline{KIN7}$/$\overline{IRQ7}$ | VSS |
| 36 | AVref | AVref | AVref | VCC |
| 37 | AVCC | AVCC | AVCC | VCC |
| 38 | P70/AN0 | P70/AN0 | P70/AN0 | NC |
| 39 | P71/AN1 | P71/AN1 | P71/AN1 | NC |
| 40 | P72/AN2 | P72/AN2 | P72/AN2 | NC |
| 41 | P73/AN3 | P73/AN3 | P73/AN3 | NC |

| Type | Instruction | Size*1 | Function |
|---|---|---|---|
| Arithmetic operations | DIVXS | B/W | Rd ÷ Rs → Rd<br>Performs signed division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder. |
| | CMP | B/W/L | Rd – Rs, Rd – #IMM<br>Compares data in a general register with data in another general register or with immediate data, and sets CCR bits according to the result. |
| | NEG | B/W/L | 0 – Rd → Rd<br>Takes the two's complement (arithmetic complement) of data in a general register. |
| | EXTU | W/L | Rd (zero extension) → Rd<br>Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by padding with zeros on the left. |
| | EXTS | W/L | Rd (sign extension) → Rd<br>Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by extending the sign bit. |
| | TAS | B | @ERd – 0, 1 → (<bit 7> of @ERd)*2<br>Tests memory contents, and sets the most significant bit (bit 7) to 1. |

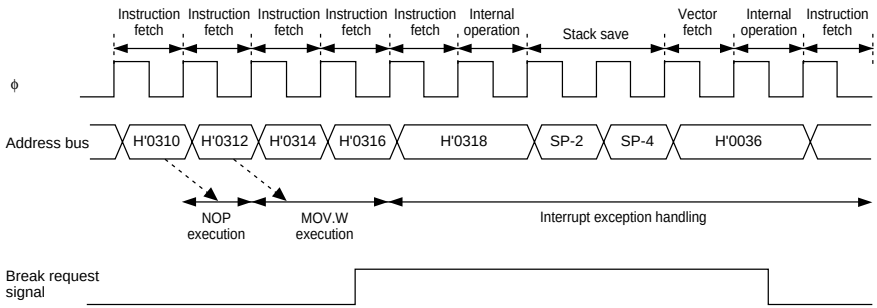
- Program area in on-chip memory, 1-state execution instruction at specified break address




H'0310 NOP
H'0312 NOP ← Breakpoint
H'0314 NOP
H'0316 NOP

NOP instruction is executed at breakpoint address H'0312 and next address, H'0314; fetch from address H'0316 starts after end of exception handling.

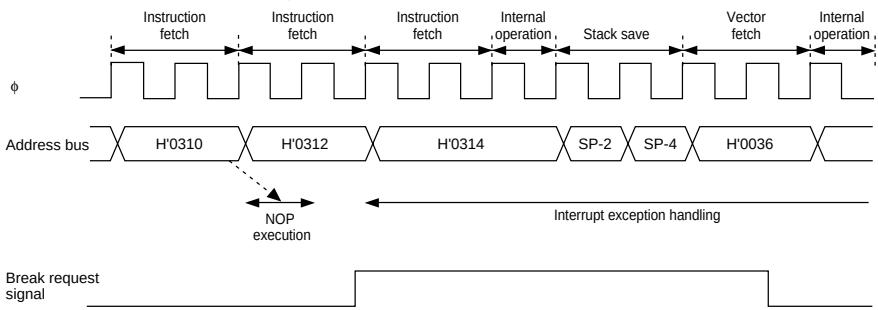
- Program area in on-chip memory, 2-state execution instruction at specified break address




H'0310 NOP
H'0312 MOV.W #xx:16,Rd ← Breakpoint
H'0316 NOP
H'0318 NOP

MOV instruction is executed at breakpoint address H'0312, NOP instruction at next address, H'0316, is not executed; fetch from address H'0316 starts after end of exception handling.

- Program area in external memory (2-state access, 16-bit-bus access), 1-state execution instruction at specified break address




H'0310 NOP
H'0312 NOP ← Breakpoint
H'0314 NOP
H'0316 NOP

NOP instruction at breakpoint address H'0312 is not executed; fetch from address H'0312 starts after end of exception handling.

**Figure 5.6 Examples of Address Break Timing**

### 5.5.5 Interrupt Response Times

This LSI are capable of fast word access to on-chip memory, and high-speed processing can be achieved by providing the program area in on-chip ROM and the stack area in on-chip RAM.

Table 5.8 shows interrupt response times—the interval between generation of an interrupt request and execution of the first instruction in the interrupt handling routine. The symbols used in table 5.8 are explained in table 5.9.

**Table 5.8 Interrupt Response Times**

| | | Number of States | |
|---|---|---|---|
| **No.** | **Item** | **Normal Mode** | **Advanced Mode** |
| 1 | Interrupt priority determination*1 | 3 | 3 |
| 2 | Number of wait states until executing instruction ends*2 | 1 to 19+2·$S_I$ | 1 to 19+2·$S_I$ |
| 3 | PC, CCR stack save | 2·$S_K$ | 2·$S_K$ |
| 4 | Vector fetch | $S_I$ | 2·$S_I$ |
| 5 | Instruction fetch*3 | 2·$S_I$ | 2·$S_I$ |
| 6 | Internal processing*4 | 2 | 2 |
| Total (using on-chip memory) | | 11 to 31 | 12 to 32 |

Notes: 1. Two states in case of internal interrupt.
2. Refers to MULXS and DIVXS instructions.
3. Prefetch after interrupt acceptance and interrupt handling routine prefetch.
4. Internal processing after interrupt acceptance and internal processing after vector fetch.

**Table 5.9 Number of States in Interrupt Handling Routine Execution**

| | | Object of Access | | | | |
|---|---|---|---|---|---|---|
| | | | External Device | | | |
| | | | 8-Bit Bus | | 16-Bit Bus | |
| | **Symbol** | **Internal Memory** | **2-State Access** | **3-State Access** | **2-State Access** | **3-State Access** |
| Instruction fetch | $S_I$ | 1 | 4 | 6+2m | 2 | 3+m |
| Branch address read | $S_J$ | | | | | |
| Stack manipulation | $S_K$ | | | | | |

Legend:
m: Number of wait states in an external device access

**2. OS = 1 (DADR corresponds to $T_H$)**

**a. CFS = 0 [base cycle = resolution (T) × 64]**

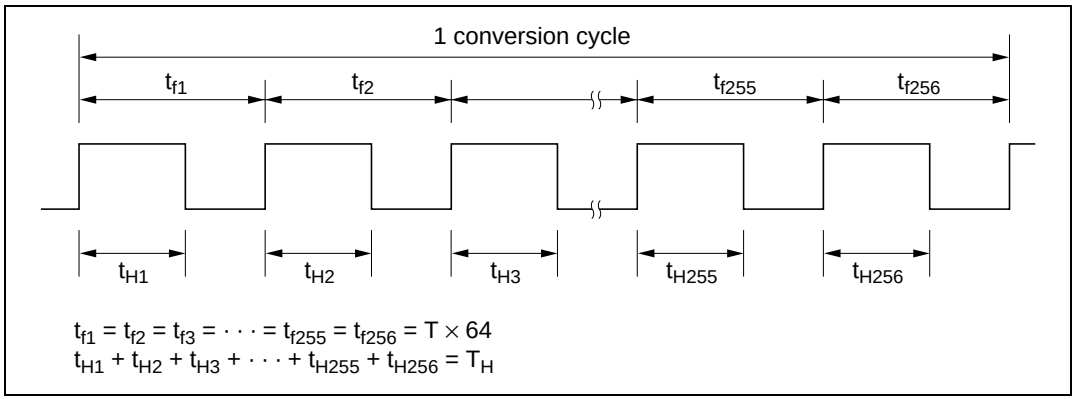



**Figure 10.4 (3) Output Waveform**

**b. CFS = 1 [base cycle = resolution (T) × 256]**

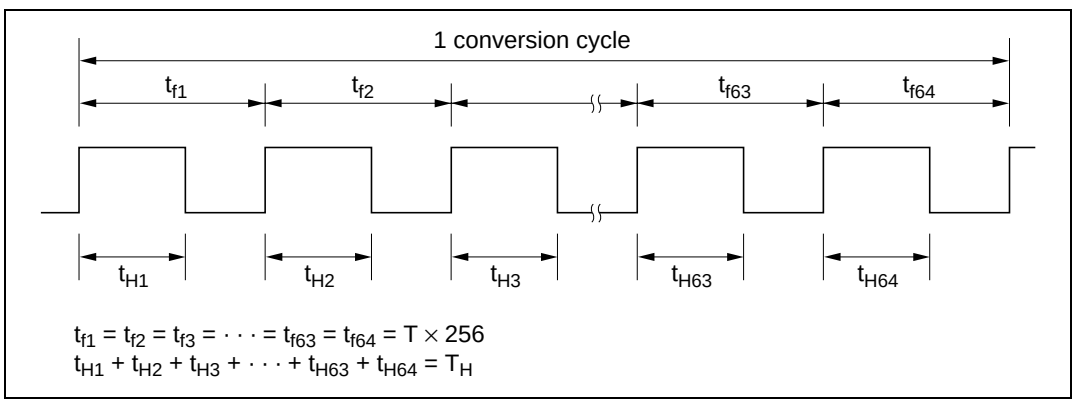



**Figure 10.4 (4) Output Waveform**

When ICRC or ICRD is used as a buffer register, its input capture flag is set by the selected transition of its input capture signal. For example, if ICRC is used to buffer ICRA, when the edge transition selected by the IEDGC bit occurs on the FTIC input capture line, ICFC will be set, and if the ICIEC bit is set, an interrupt will be requested. The FRC value will not be transferred to ICRC, however.

In buffered input capture, if the upper byte of either of the two registers to which data will be transferred (ICRA and ICRC, or ICRB and ICRD) is being read when the input signal arrives, input capture is delayed by one system clock (ϕ) period. Figure 11.10 shows the timing when BUFEA = 1.

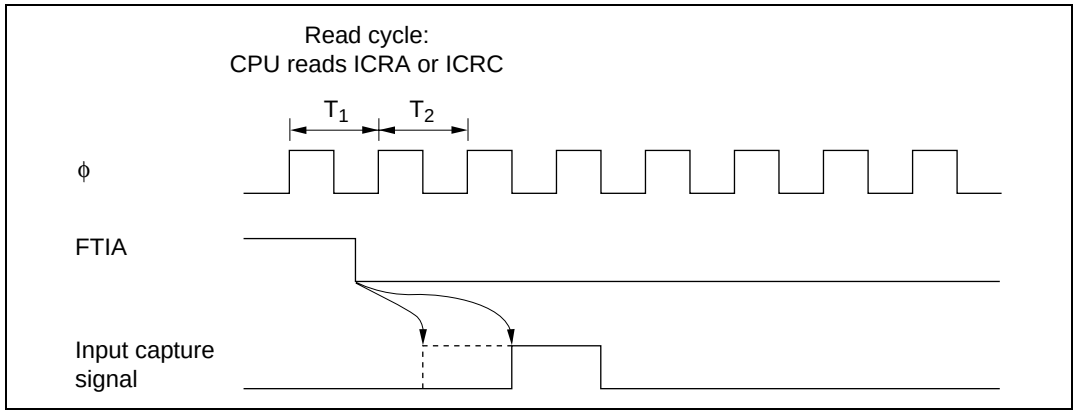



**Figure 11.10 Buffered Input Capture Timing (Input Capture Input when ICRA or ICRC Is Read)**

### 11.3.5 Timing of Input Capture Flag (ICF) Setting

The input capture flag ICFx (x = A, B, C, D) is set to 1 by the internal input capture signal. The FRC value is simultaneously transferred to the corresponding input capture register (ICRx). Figure 11.11 shows the timing of this operation.

# Section 12 8-Bit Timers

## 12.1 Overview

This LSI include an 8-bit timer module with two channels (TMR0 and TMR1). Each channel has an 8-bit counter (TCNT) and two time constant registers (TCORA and TCORB) that are constantly compared with the TCNT value to detect compare-matches. The 8-bit timer module can be used as a multifunction timer in a variety of applications, such as generation of a rectangular-wave output with an arbitrary duty cycle.

The H8S/2148 Group also has two similar 8-bit timer channels (TMRX and TMRY), and the H8S/2144 Group and H8S/2147N has one (TMRY). These channels can be used in a connected configuration using the timer connection function. TMRX and TMRY have greater input/output and interrupt function related restrictions than TMR0 and TMR1.

### 12.1.1 Features

- Selection of clock sources
  - TMR0, TMR1: The counter input clock can be selected from six internal clocks and an external clock (enabling use as an external event counter).
  - TMRX, TMRY: The counter input clock can be selected from three internal clocks and an external clock (enabling use as an external event counter).
- Selection of three ways to clear the counters
  - The counters can be cleared on compare-match A or B, or by an external reset signal.
- Timer output controlled by two compare-match signals
  - The timer output signal in each channel is controlled by two independent compare-match signals, enabling the timer to be used for various applications, such as the generation of pulse output or PWM output with an arbitrary duty cycle.
    (Note: TMRY does not have a timer output pin.)
- Cascading of the two channels (TMR0, TMR1)
  - Operation as a 16-bit timer can be performed using channel 0 as the upper half and channel 1 as the lower half (16-bit count mode).
  - Channel 1 can be used to count channel 0 compare-match occurrences (compare-match count mode).
- Multiple interrupt sources for each channel
  - TMR0, TMR1, TMRY: Two compare-match interrupts and one overflow interrupt can be requested independently.
  - TMRX: One input capture source is available.

**Bit 0**

| CBOINV | Description | |
|---|---|---|
| 0 | The CBLANK signal is used directly as the CBLANK output | (Initial value) |
| 1 | The CBLANK signal is inverted before use as the CBLANK output | |

### 13.2.3 Timer Connection Register S (TCONRS)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TMRX/Y | ISGENE | HOMOD1 | HOMOD0 | VOMOD1 | VOMOD0 | CLMOD1 | CLMOD0 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

TCONRS is an 8-bit readable/writable register that selects 8-bit timer TMRX/TMRY access and the synchronization signal output signal source and generation method.

TCONRS is initialized to H'00 by a reset and in hardware standby mode.

**Bit 7—TMRX/TMRY Access Select (TMRX/Y):** The TMRX and TMRY registers can only be accessed when the HIE bit in SYSCR is cleared to 0. In the H8S/2148 Group, some of the TMRX registers and the TMRY registers are assigned to the same memory space addresses (H'FFF0 to H'FFF5), and the TMRX/Y bit determines which registers are accessed. In the H8S/2144 Group and H8S/2147N, there is no control of TMRY register access by this bit.

**Bit 7**

| TMRX/Y | Description | |
|---|---|---|
| 0 | The TMRX registers are accessed at addresses H'FFF0 to H'FFF5 | (Initial value) |
| 1 | The TMRY registers are accessed at addresses H'FFF0 to H'FFF5 | |

**Bit 6—Internal Synchronization Signal Select (ISGENE):** Selects internal synchronization signals (IHG, IVG, and CL4 signals) as the signal sources for the IHO, IVO, and CLO signals.

# Section 15 Serial Communication Interface (SCI, IrDA)

## 15.1 Overview

This LSI are equipped with a 3-channel serial communication interface (SCI). The SCI can handle both asynchronous and clocked synchronous serial communication. A function is also provided for serial communication between processors (multiprocessor communication function).

One of the three SCI channels can transmit and receive IrDA communication waveforms based on IrDA specification version 1.0.

### 15.1.1 Features

SCI features are listed below.

- Choice of asynchronous or synchronous serial communication mode

  Asynchronous mode:

  — Serial data communication is executed using an asynchronous system in which synchronization is achieved character by character

  Serial data communication can be carried out with standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA)

  — A multiprocessor communication function is provided that enables serial data communication with a number of processors

  — Choice of 12 serial data transfer formats

  | | |
  |---|---|
  | Data length: | 7 or 8 bits |
  | Stop bit length: | 1 or 2 bits |
  | Parity: | Even, odd, or none |
  | Multiprocessor bit: | 1 or 0 |

  — Receive error detection: Parity, overrun, and framing errors

  — Break detection: Break can be detected by reading the RxD pin level directly in case of a framing error

| Bit 2 | Bit 1 | Bit 0 | Bits/Frame | | |
|---|---|---|---|---|---|
| BC2 | BC1 | BC0 | Synchronous Serial Format | I²C Bus Format | |
| 0 | 0 | 0 | 8 | 9 | (Initial value) |
| | | 1 | 1 | 2 | |
| | 1 | 0 | 2 | 3 | |
| | | 1 | 3 | 4 | |
| 1 | 0 | 0 | 4 | 5 | |
| | | 1 | 5 | 6 | |
| | 1 | 0 | 6 | 7 | |
| | | 1 | 7 | 8 | |

### 16.2.5 I²C Bus Control Register (ICCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ICE | IEIC | MST | TRS | ACKE | BBSY | IRIC | SCP |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/(W)* | W |

Note: * Only 0 can be written, to clear the flag.

ICCR is an 8-bit readable/writable register that enables or disables the I²C bus interface, enables or disables interrupts, selects master or slave mode and transmission or reception, enables or disables acknowledgement, confirms the I²C bus interface bus status, issues start/stop conditions, and performs interrupt flag confirmation.

ICCR is initialized to H'01 by a reset and in hardware standby mode.

**Bit 7—I²C Bus Interface Enable (ICE):** Selects whether or not the I²C bus interface is to be used. When ICE is set to 1, port pins function as SCL and SDA input/output pins and transfer operations are enabled. When ICE is cleared to 0, the I²C bus interface module is halted and its internal states are cleared.

The SAR and SARX registers can be accessed when ICE is 0. The ICMR and ICDR registers can be accessed when ICE is 1.

**Bit 2**

| BBSY | Description | |
|---|---|---|
| 0 | Bus is free | (Initial value) |
| | [Clearing condition] | |
| | When a stop condition is detected | |
| 1 | Bus is busy | |
| | [Setting condition] | |
| | When a start condition is detected | |

**Bit 1—I²C Bus Interface Interrupt Request Flag (IRIC):** Indicates that the I²C bus interface has issued an interrupt request to the CPU. IRIC is set to 1 at the end of a data transfer, when a slave address or general call address is detected in slave receive mode, when bus arbitration is lost in master transmit mode, and when a stop condition is detected. IRIC is set at different times depending on the FS bit in SAR and the WAIT bit in ICMR. See section 16.3.6, IRIC Setting Timing and SCL Control. The conditions under which IRIC is set also differ depending on the setting of the ACKE bit in ICCR.

IRIC is cleared by reading IRIC after it has been set to 1, then writing 0 in IRIC.

When the DTC is used, IRIC is cleared automatically and transfer can be performed continuously without CPU intervention.

### 20.1.4 Register Configuration

Table 20.2 summarizes the registers of the A/D converter.

**Table 20.2 A/D Converter Registers**

| Name | Abbreviation | R/W | Initial Value | Address*1 |
|---|---|---|---|---|
| A/D data register AH | ADDRAH | R | H'00 | H'FFE0 |
| A/D data register AL | ADDRAL | R | H'00 | H'FFE1 |
| A/D data register BH | ADDRBH | R | H'00 | H'FFE2 |
| A/D data register BL | ADDRBL | R | H'00 | H'FFE3 |
| A/D data register CH | ADDRCH | R | H'00 | H'FFE4 |
| A/D data register CL | ADDRCL | R | H'00 | H'FFE5 |
| A/D data register DH | ADDRDH | R | H'00 | H'FFE6 |
| A/D data register DL | ADDRDL | R | H'00 | H'FFE7 |
| A/D control/status register | ADCSR | R/(W)*2 | H'00 | H'FFE8 |
| A/D control register | ADCR | R/W | H'3F | H'FFE9 |
| Module stop control register | MSTPCRH | R/W | H'3F | H'FF86 |
| | MSTPCRL | R/W | H'FF | H'FF87 |
| Keyboard comparator control register | KBCOMP | R/W | H'00 | H'FEE4 |

Notes: 1. Lower 16 bits of the address.
2. Only 0 can be written in bit 7, to clear the flag.

## 20.2 Register Descriptions

### 20.2.1 A/D Data Registers A to D (ADDRA to ADDRD)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | — | — | — | — | — | — |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

There are four 16-bit read-only ADDR registers, ADDRA to ADDRD, used to store the results of A/D conversion.

## 22.9 Interrupt Handling when Programming/Erasing Flash Memory

All interrupts, including NMI input is disabled when flash memory is being programmed or erased (when the P or E bit is set in FLMCR1), and while the boot program is executing in boot mode*1, to give priority to the program or erase operation. There are three reasons for this:

1. Interrupt during programming or erasing might cause a violation of the programming or erasing algorithm, with the result that normal operation could not be assured.
2. In the interrupt exception handling sequence during programming or erasing, the vector would not be read correctly*2, possibly resulting in MCU runaway.
3. If interrupt occurred during boot program execution, it would not be possible to execute the normal boot mode sequence.

For these reasons, in on-board programming mode alone there are conditions for disabling interrupt, as an exception to the general rule. However, this provision does not guarantee normal erasing and programming or MCU operation. All interrupt requests, including NMI input, must therefore be disabled inside and outside the MCU when programming or erasing flash memory. Interrupt is also disabled in the error-protection state while the P or E bit remains set in FLMCR1.

Notes: 1. Interrupt requests must be disabled inside and outside the MCU until the programming control program has completed programming.

2. The vector may not be read correctly in this case for the following two reasons:
   - If flash memory is read while being programmed or erased (while the P or E bit is set in FLMCR1), correct read data will not be obtained (undetermined values will be returned).
   - If the interrupt entry in the vector table has not been programmed yet, interrupt exception handling will not be executed correctly.

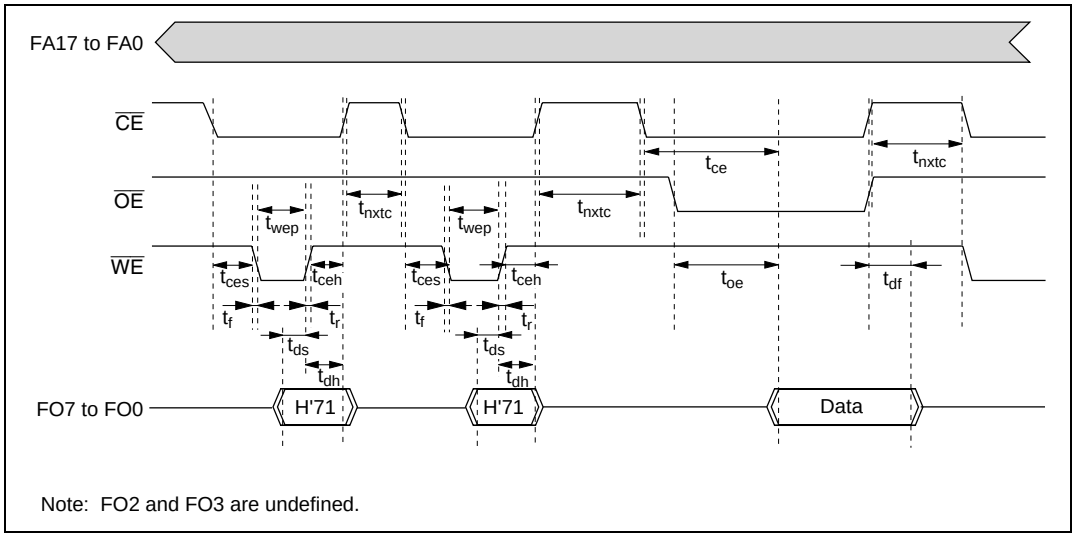



**Figure 23.22 Status Read Mode Timing Waveforms**

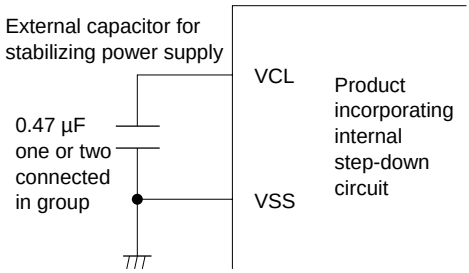
**Table 23.19 Status Read Mode Return Commands**

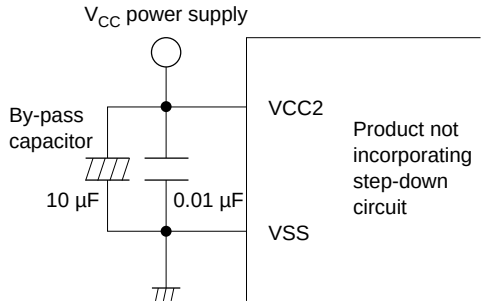
| Pin Name | FO7 | FO6 | FO5 | FO4 | FO3 | FO2 | FO1 | FO0 |
|---|---|---|---|---|---|---|---|---|
| Attribute | Normal end identification | Command error | Program-ming error | Erase error | — | — | Program-ming or erase count exceeded | Effective address error |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Indications | Normal end: 0<br>Abnormal end: 1 | Command error: 1<br>Otherwise: 0 | Program-ming error: 1<br>Otherwise: 0 | Erase error: 1<br>Otherwise: 0 | — | — | Count exceeded: 1<br>Otherwise: 0 | Effective address error: 1<br>Otherwise: 0 |

Note: FO2 and FO3 are undefined.

### 23.10.8 Status Polling

- The FO7 status polling flag indicates the operating status in auto-program or auto-erase mode.
- The FO6 status polling flag indicates a normal or abnormal end in auto-program or auto-erase mode.




For products incorporating an internal step-down circuit, do not connect the VCL pin to the VCC power supply. (The VCC1 pin must be connected to the VCC power supply as usual.)

The power supply stabilization capacitor must be connected to the VCL pin. Use a monolithic ceramic capacitor of 0.47 µF(one or two connected in group) and locate it near the pins.

In case the power supply voltage is lower than 3.6 V, connect the capacitor in the same way as the case with no step-down circuit incorporated.

<Products incorporating internal step-down circuit>

HD6432148S, HD6432148SW,
HD6432147S, HD6432147SW
HD6432144S, HD6432143S,
HD64F2148A, HD64F2147A,
HD64F2144A

The location of the VCC2 ($V_{CC}$ power supply) pin in the product not incorporating an internal step-down circuit, is the same as the VCL pin in a product incorporating an internal step-down circuit.

It is recommended that the by-pass capacitors are connected to the power supply terminal (these are reference values).

<Products not incorporating internal step-down circuit>

HD64F2148(V), HD64F2147N(V),
HD64F2144(V), HD64F2142(V),
HD6432142,
HD6432148SV, HD6432148SVW,
HD6432147SV, HD6432147SVW,
HD6432144SV, HD6432143SV,
HD64F2148AV, HD64F2147AV,
HD64F2144AV

**Figure 26.3 Connection of External Capacitor (Mask ROM Type Incorporating Step-Down Circuit and Product Not Incorporating Step-Down Circuit)**

**Table 26.18 Permissible Output Currents**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | SCL1, SCL0, SDA1, SDA0, PS2AC to PS2CC, PS2AD to PS2CD, PA7 to PA4 (bus drive function selected) | $I_{OL}$ | — | — | 20 | mA |
| | Ports 1, 2, 3 | | — | — | 10 | mA |
| | $\overline{\text{RESO}}$ | | — | — | 3 | mA |
| | Other output pins | | — | — | 2 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\sum I_{OL}$ | — | — | 80 | mA |
| | Total of all output pins, including the above | | — | — | 120 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\sum -I_{OH}$ | — | — | 40 | mA |

**Table 26.31 DC Characteristics (2)**

Conditions: $V_{CC}$ = 3.0 V to 5.5 V*11, $V_{CC}B$ = 3.0 V to 5.5 V, $AV_{CC}$*1 = 3.0 V to 5.5 V, $AV_{ref}$ = 3.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$*1 = 0 V, $T_a$ = –20 to +75°C*11

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60(KWUL = 00)*2*6, $\overline{KIN15}$ to $\overline{KIN8}$*7*8, $\overline{IRQ2}$ to $\overline{IRQ0}$*3, $\overline{IRQ5}$ to $\overline{IRQ3}$ | (1) | $V_T^-$ | $V_{CC} \times 0.2$<br>$V_{CC}B \times 0.2$ | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$<br>$V_{CC}B \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$<br>$V_{CC}B \times 0.05$ | — | — | V | |
| Schmitt trigger input voltage (in level swiching)*6 | P67 to P60 (KWUL = 01) | | $V_T^-$ | $V_{CC} \times 0.3$ | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$ | — | — | | |
| | P67 to P60 (KWUL = 10) | | $V_T^-$ | $V_{CC} \times 0.4$ | — | — | | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.8$ | | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.03$ | — | — | | |
| | P67 to P60 (KWUL = 11) | | $V_T^-$ | $V_{CC} \times 0.45$ | — | — | | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.9$ | | |
| | | | $V_T^+ - V_T^-$ | 0.05 | — | — | | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC} \times 0.9$ | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | PA7 to PA0*7 | | | $V_{CC}B \times 0.7$ | — | $V_{CC}B$ +0.3 | V | |
| | Port 7 | | | $V_{CC} \times 0.7$ | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | Test |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Conditions |
| Read data access time 1 | $t_{ACC1}$ | — | 1.0 × $t_{cyc}$ –30 | — | 1.0 × $t_{cyc}$ –40 | — | 1.0 × $t_{cyc}$ –60 | ns | Figure 26.10 to figure 26.14 |
| Read data access time 2 | $t_{ACC2}$ | — | 1.5 × $t_{cyc}$ –25 | — | 1.5 × $t_{cyc}$ –35 | — | 1.5 × $t_{cyc}$ –50 | ns | |
| Read data access time 3 | $t_{ACC3}$ | — | 2.0 × $t_{cyc}$ –30 | — | 2.0 × $t_{cyc}$ –40 | — | 2.0 × $t_{cyc}$ –60 | ns | |
| Read data access time 4 | $t_{ACC4}$ | — | 2.5 × $t_{cyc}$ –25 | — | 2.5 × $t_{cyc}$ –35 | — | 2.5 × $t_{cyc}$ –50 | ns | |
| Read data access time 5 | $t_{ACC5}$ | — | 3.0 × $t_{cyc}$ –30 | — | 3.0 × $t_{cyc}$ –40 | — | 3.0 × $t_{cyc}$ –60 | ns | |
| $\overline{WR}$ delay time 1 | $t_{WRD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ delay time 2 | $t_{WRD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ pulse width 1 | $t_{WSW1}$ | 1.0 × $t_{cyc}$ –20 | — | 1.0 × $t_{cyc}$ –30 | — | 1.0 × $t_{cyc}$ –40 | — | ns | |
| $\overline{WR}$ pulse width 2 | $t_{WSW2}$ | 1.5 × $t_{cyc}$ –20 | — | 1.5 × $t_{cyc}$ –30 | — | 1.5 × $t_{cyc}$ –40 | — | ns | |
| Write data delay time | $t_{WDD}$ | — | 30 | — | 45 | — | 60 | ns | |
| Write data setup time | $t_{WDS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Write data hold time | $t_{WDH}$ | 10 | — | 15 | — | 20 | — | ns | |
| $\overline{WAIT}$ setup time | $t_{WTS}$ | 30 | — | 45 | — | 60 | — | ns | |
| $\overline{WAIT}$ hold time | $t_{WTH}$ | 5 | — | 5 | — | 10 | — | ns | |

| Address | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Module Name | Bus Width |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H'FFBE | P7PIN (read) | P77PIN | P76PIN | P75PIN | P74PIN | P73PIN | P72PIN | P71PIN | P70PIN | Ports | 8 |
| | PBDDR (write) | PB7DDR | PB6DDR | PB5DDR | PB4DDR | PB3DDR | PB2DDR | PB1DDR | PB0DDR | | |
| H'FFBF | P8DR | — | P86DR | P85DR | P84DR | P83DR | P82DR | P81DR | P80DR | | |
| H'FFC0 | P9DDR | P97DDR | P96DDR | P95DDR | P94DDR | P93DDR | P92DDR | P91DDR | P90DDR | | |
| H'FFC1 | P9DR | P97DR | P96DR | P95DR | P94DR | P93DR | P92DR | P91DR | P90DR | | |
| H'FFC2 | IER | IRQ7E | IRQ6E | IRQ5E | IRQ4E | IRQ3E | IRQ2E | IRQ1E | IRQ0E | Interrupt controller | 8 |
| H'FFC3 | STCR | IICS | IICX1 | IICX0 | IICE | FLSHE | — | ICKS1 | ICKS0 | System | 8 |
| H'FFC4 | SYSCR | CS2E | IOSE | INTM1 | INTM0 | XRST | NMIEG | HIE | RAME | | |
| H'FFC5 | MDCR | EXPE | — | — | — | — | — | MDS1 | MDS0 | | |
| H'FFC6 | BCR | ICIS1 | ICIS0 | BRSTRM | BRSTS1 | BRSTS0 | — | IOS1 | IOS0 | Bus controller | 8 |
| H'FFC7 | WSCR | RAMS | RAM0 | ABW | AST | WMS1 | WMS0 | WC1 | WC0 | | |
| H'FFC8 | TCR0 | CMIEB | CMIEA | OVIE | CCLR1 | CCLR0 | CKS2 | CKS1 | CKS0 | TMR0, TMR1 | 16 |
| H'FFC9 | TCR1 | CMIEB | CMIEA | OVIE | CCLR1 | CCLR0 | CKS2 | CKS1 | CKS0 | | |
| H'FFCA | TCSR0 | CMFB | CMFA | OVF | ADTE | OS3 | OS2 | OS1 | OS0 | | |
| H'FFCB | TCSR1 | CMFB | CMFA | OVF | — | OS3 | OS2 | OS1 | OS0 | | |
| H'FFCC | TCORA0 | | | | | | | | | | |
| H'FFCD | TCORA1 | | | | | | | | | | |
| H'FFCE | TCORB0 | | | | | | | | | | |
| H'FFCF | TCORB1 | | | | | | | | | | |
| H'FFD0 | TCNT0 | | | | | | | | | | |
| H'FFD1 | TCNT1 | | | | | | | | | | |
| H'FFD2 | PWOERB | OE15 | OE14 | OE13 | OE12 | OE11 | OE10 | OE9 | OE8 | PWM | 8 |
| H'FFD3 | PWOERA | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 | | |
| H'FFD4 | PWDPRB | OS15 | OS14 | OS13 | OS12 | OS11 | OS10 | OS9 | OS8 | | |
| H'FFD5 | PWDPRA | OS7 | OS6 | OS5 | OS4 | OS3 | OS2 | OS1 | OS0 | | |
| H'FFD6 | PWSL | PWCKE | PWCKS | — | — | RS3 | RS2 | RS1 | RS0 | | |
| H'FFD7 | PWDR0 to PWDR15 | | | | | | | | | | |
| H'FFD8 | SMR0 | C/$\overline{A}$ | CHR | PE | O/$\overline{E}$ | STOP | MP | CKS1 | CKS0 | SCI0 | 8 |
| | ICCR0 | ICE | IEIC | MST | TRS | ACKE | BBSY | IRIC | SCP | IIC0 | |
| H'FFD9 | BRR0 | | | | | | | | | SCI0 | |
| | ICSR0 | ESTP | STOP | IRTR | AASX | AL | AAS | ADZ | ACKB | IIC0 | |

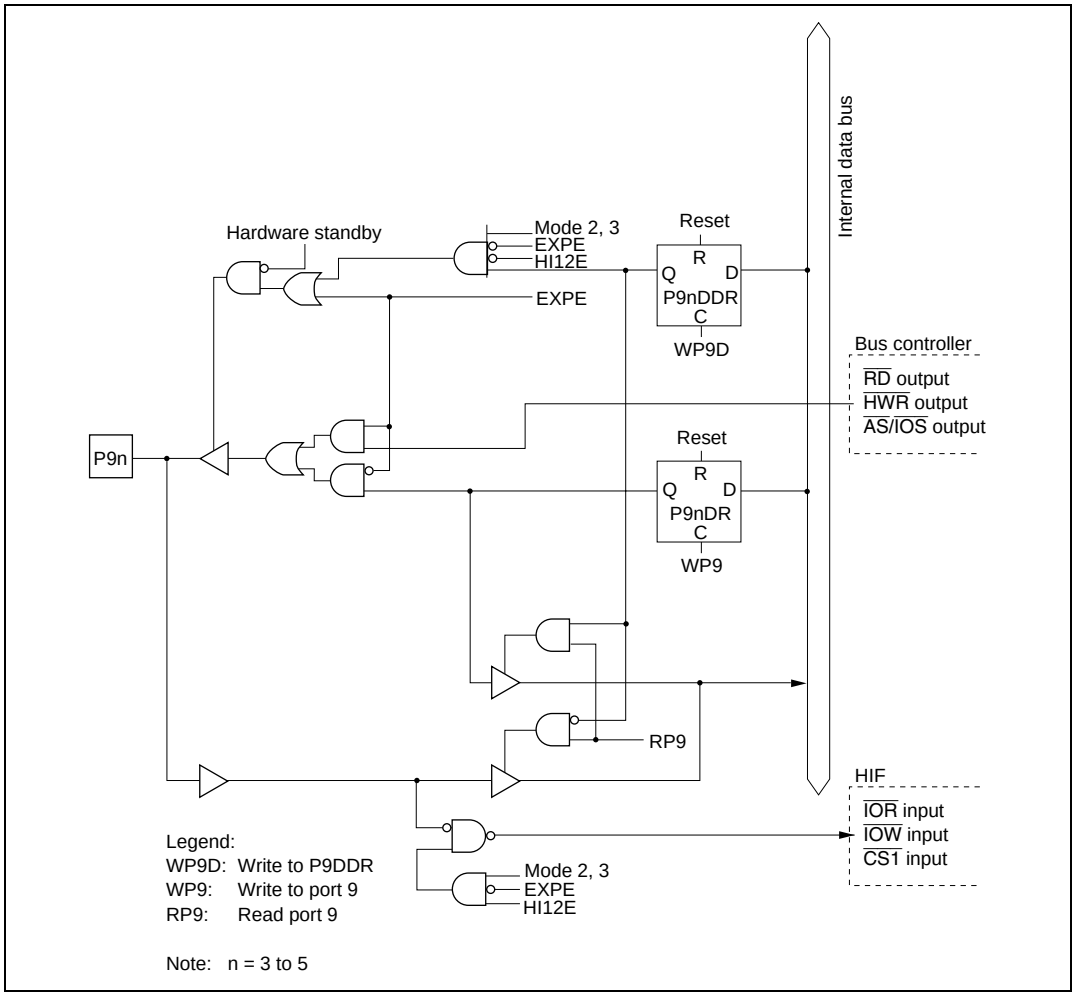



**Figure C.31 Port 9 Block Diagram (Pins P93 to P95)**