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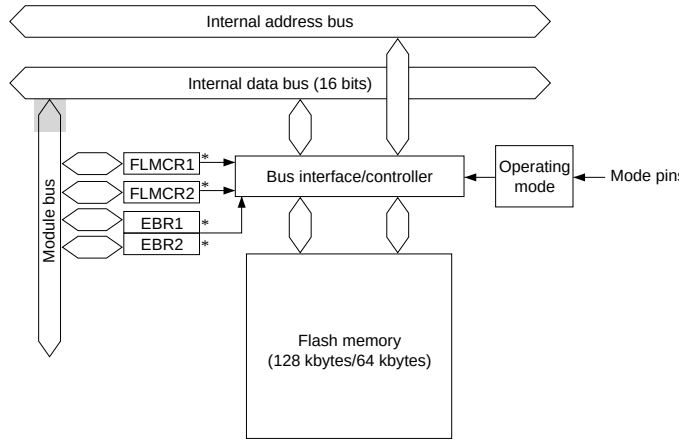
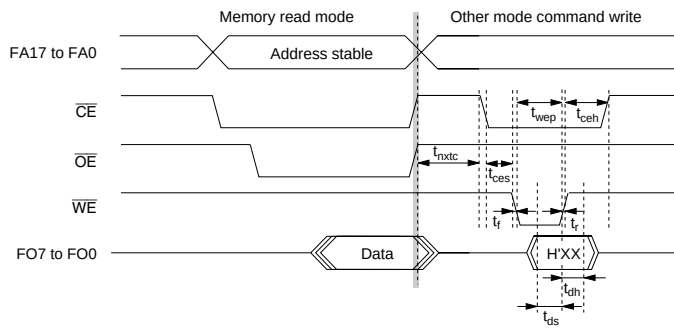
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8S/2000 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | IrDA, SCI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 74 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BFQFP |
| Supplier Device Package | 100-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df2144fa20v |

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| 22.4.2 Block Diagram<br>Figure 22.2 Block Diagram of Flash Memory | 643 | Figure 22.2 amended<br>  |
| 22.5.3 Erase Block Registers 1 and 2 (EBR1, EBR2) | 653 | Bit figure amended<br>Read/Write description of bits 7 to 2 (Before) — *2 → (After) — |
| 22.10.1 Programmer Mode Setting | 671 | Note amended<br>In programmer mode, ... Renesas Technology microcomputer device types with 128-kbyte*1*3 or 64-kbyte*2*3 on-chip flash memory. ...<br>Note: 3. Use products other than the A-mask version of the H8S/2148, H8S/2147N, H8S/2144, and H8S/2142 ... |
| 22.10.4 Memory Read Mode<br>Figure 22.17 Timing Waveforms when Entering Another Mode from Memory Read Mode | 675 | Figure 22.17 amended<br>  |

| Pin No. | Pin Name | | | |
|---|---|---|---|---|
| | Expanded Modes | | Single-Chip Modes | |
| FP-100B TFP-100B | Mode 1 | Mode 2 (EXPE = 1) Mode 3 (EXPE = 1) | Mode 2 (EXPE = 0) Mode 3 (EXPE = 0) | Flash Memory Writer Mode |
| 22 | $\overline{RD}$ | $\overline{RD}$ | P93/$\overline{IOR}$ | $\overline{WE}$ |
| 23 | P92/$\overline{IRQ0}$ | P92/$\overline{IRQ0}$ | P92/$\overline{IRQ0}$ | VSS |
| 24 | P91/$\overline{IRQ1}$ | P91/$\overline{IRQ1}$ | P91/$\overline{IRQ1}$ | VCC |
| 25 | $\overline{LWR}$/P90/$\overline{IRQ2}$/ $\overline{ADTRG}$ | $\overline{LWR}$/P90/$\overline{IRQ2}$/ $\overline{ADTRG}$ | P90/$\overline{IRQ2}$/$\overline{ADTRG}$/ $\overline{ECS2}$ | VCC |
| 26 | P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI | P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI | P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI | NC |
| 27 | P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO | P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO | P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO | NC |
| 28 | P62/FTIA/CIN2/ $\overline{KIN2}$/TMIY/ VSYNCI | P62/FTIA/CIN2/ $\overline{KIN2}$/TMIY/ VSYNCI | P62/FTIA/CIN2/ $\overline{KIN2}$/TMIY/ VSYNCI | NC |
| 29 | P63/FTIB/CIN3/ $\overline{KIN3}$/VFBACKI | P63/FTIB/CIN3/ $\overline{KIN3}$/VFBACKI | P63/FTIB/CIN3/ $\overline{KIN3}$/VFBACKI | NC |
| 30 | PA3/CIN11/ $\overline{KIN11}$/PS2AD | A19/PA3/CIN11/ $\overline{KIN11}$/PS2AD | PA3/CIN11/ $\overline{KIN11}$/PS2AD | NC |
| 31 | PA2/CIN10/ $\overline{KIN10}$/PS2AC | A18/PA2/CIN10/ $\overline{KIN10}$/PS2AC | PA2/CIN10/ $\overline{KIN10}$/PS2AC | NC |
| 32 | P64/FTIC/CIN4/ $\overline{KIN4}$/CLAMPO | P64/FTIC/CIN4/ $\overline{KIN4}$/CLAMPO | P64/FTIC/CIN4/ $\overline{KIN4}$/CLAMPO | NC |
| 33 | P65/FTID/CIN5/ $\overline{KIN5}$ | P65/FTID/CIN5/ $\overline{KIN5}$ | P65/FTID/CIN5/ $\overline{KIN5}$ | NC |
| 34 | P66/FTOB/CIN6/ $\overline{KIN6}$/$\overline{IRQ6}$ | P66/FTOB/CIN6/ $\overline{KIN6}$/$\overline{IRQ6}$ | P66/FTOB/CIN6/ $\overline{KIN6}$/$\overline{IRQ6}$ | NC |
| 35 | P67/TMOX/CIN7/ $\overline{KIN7}$/$\overline{IRQ7}$ | P67/TMOX/CIN7/ $\overline{KIN7}$/$\overline{IRQ7}$ | P67/TMOX/CIN7/ $\overline{KIN7}$/$\overline{IRQ7}$ | VSS |
| 36 | AVref | AVref | AVref | VCC |
| 37 | AVCC | AVCC | AVCC | VCC |
| 38 | P70/AN0 | P70/AN0 | P70/AN0 | NC |
| 39 | P71/AN1 | P71/AN1 | P71/AN1 | NC |
| 40 | P72/AN2 | P72/AN2 | P72/AN2 | NC |
| 41 | P73/AN3 | P73/AN3 | P73/AN3 | NC |

### 2.8.6 Power-Down State

The power-down state includes both modes in which the CPU stops operating and modes in which the CPU does not stop. There are five modes in which the CPU stops operating: sleep mode, software standby mode, hardware standby mode, subsleep mode, and watch mode. There are also three other power-down modes: medium-speed mode, module stop mode, and subactive mode. In medium-speed mode, the CPU and other bus masters operate on a medium-speed clock. Module stop mode permits halting of the operation of individual modules, other than the CPU. Subactive mode, subsleep mode, and watch mode are power-down modes that use subclock input. For details, refer to section 25, Power-Down State.

#### Sleep Mode

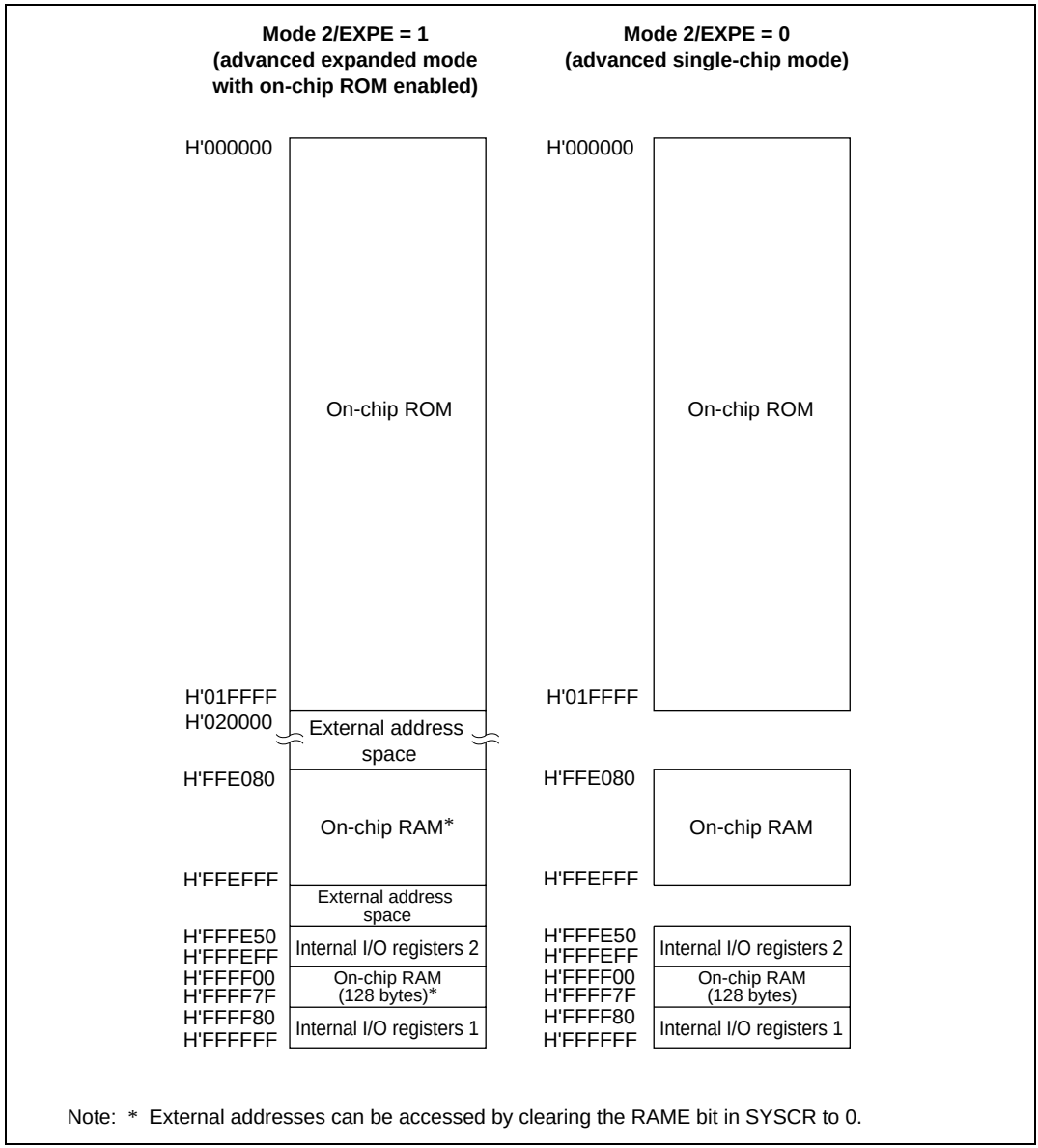
A transition to sleep mode is made if the SLEEP instruction is executed while the software standby bit (SSBY) in the standby control register (SBYCR) and the LSON bit in the low-power control register (LPWRCR) are both cleared to 0. In sleep mode, CPU operations stop immediately after execution of the SLEEP instruction. The contents of CPU registers are retained.

#### Software Standby Mode

A transition to software standby mode is made if the SLEEP instruction is executed while the SSBY bit in SBYCR is set to 1 and the LSON bit in LPWRCR and the PSS bit in the WDT1 timer control/status register (TCSR) are both cleared to 0. In software standby mode, the CPU and clock halt and all MCU operations stop. As long as a specified voltage is supplied, the contents of CPU registers and on-chip RAM are retained. The I/O ports also remain in their existing states.

#### Hardware Standby Mode

A transition to hardware standby mode is made when the $\overline{\text{STBY}}$ pin goes low. In hardware standby mode, the CPU and clock halt and all MCU operations stop. The on-chip supporting modules are reset, but as long as a specified voltage is supplied, on-chip RAM contents are retained.




Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

**Figure 3.1 H8S/2148 (Except for F-ZTAT A-Mask Version) and H8S/2144 Memory Map in Each Operating Mode (cont)**

## 5.3 Interrupt Sources

Interrupt sources comprise external interrupts (NMI and IRQ7 to IRQ0) and internal interrupts.

### 5.3.1 External Interrupts

There are nine external interrupt sources from 25 input pins (23 actual pins): NMI, $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$, and $\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$. KIN15 to KIN8 share the IRQ7 interrupt source, and KIN7 to KIN0 share the IRQ6 interrupt source. Of these, NMI, IRQ7, IRQ6, and IRQ2 to IRQ0 can be used to restore the H8S/2148 Group or H8S/2144 Group chip from software standby mode.

#### NMI Interrupt

NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the interrupt control mode and the status of the CPU interrupt mask bits. The NMIEG bit in SYSCR can be used to select whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

The vector number for NMI interrupt exception handling is 7.

#### IRQ7 to IRQ0 Interrupts

Interrupts IRQ7 to IRQ0 are requested by an input signal at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$. Interrupts IRQ7 to IRQ0 have the following features:

- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.
- Enabling or disabling of interrupt requests IRQ7 to IRQ0 can be selected with IER.
- The interrupt control level can be set with ICR.
- The status of interrupt requests IRQ7 to IRQ0 is indicated in ISR. ISR flags can be cleared to 0 by software.

A block diagram of interrupts IRQ7 to IRQ0 is shown in figure 5.3.

Figure 5.7 shows a block diagram of the priority decision circuit.

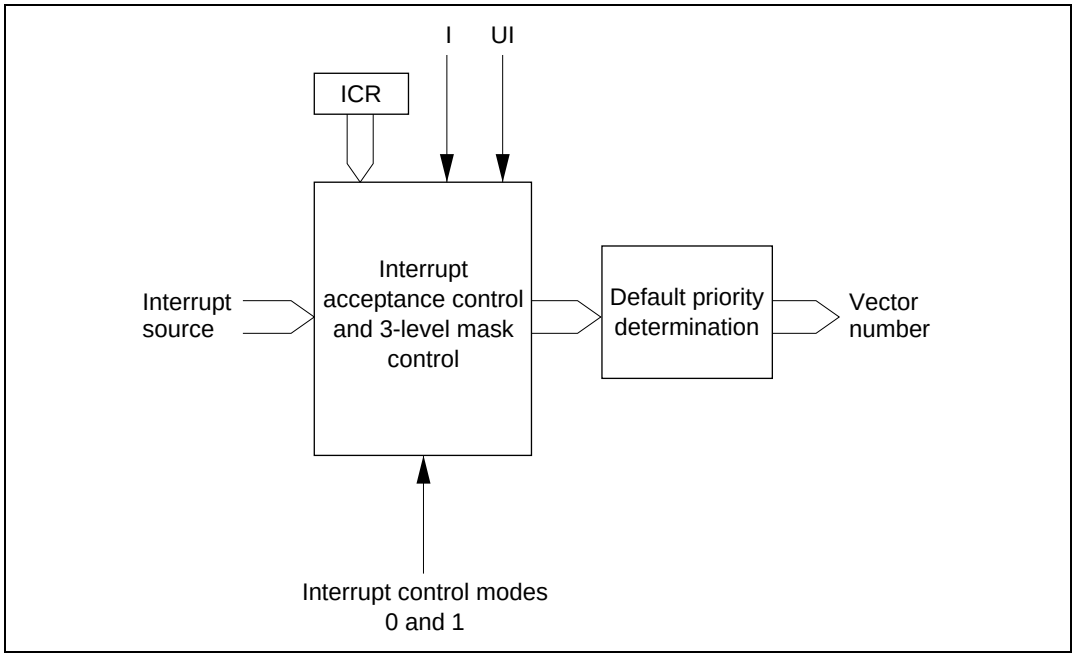



**Figure 5.7 Block Diagram of Interrupt Control Operation**

### Interrupt Acceptance Control and 3-Level Control

In interrupt control modes 0 and 1, interrupt acceptance control and 3-level mask control is performed by means of the I and UI bits in CCR, and ICR (control level).

Table 5.6 shows the interrupts selected in each interrupt control mode.

| Pin | Selection Method and Pin Functions |
|---|---|

P94/$\overline{\text{HWR}}$/$\overline{\text{IOW}}$

The pin function is switched as shown below according to the combination of operating mode, bit HI12E in SYSCR2, and bit P94DDR.

| Operating mode | Modes 1, 2, 3 (EXPE = 1) | Modes 2, 3 (EXPE = 0) | | |
|---|---|---|---|---|
| HI12E | — | 0 | | 1 |
| P94DDR | — | 0 | 1 | — |
| Pin function | $\overline{\text{HWR}}$ output pin | P94 input pin | P94 output pin | $\overline{\text{IOW}}$ input pin |

P93/$\overline{\text{RD}}$/$\overline{\text{IOR}}$

The pin function is switched as shown below according to the combination of operating mode, bit HI12E in SYSCR2, and bit P93DDR.

| Operating mode | Modes 1, 2, 3 (EXPE = 1) | Modes 2, 3 (EXPE = 0) | | |
|---|---|---|---|---|
| HI12E | — | 0 | | 1 |
| P93DDR | — | 0 | 1 | — |
| Pin function | $\overline{\text{RD}}$ output pin | P93 input pin | P93 output pin | $\overline{\text{IOR}}$ input pin |

P92/$\overline{\text{IRQ0}}$

| P92DDR | 0 | 1 |
|---|---|---|
| Pin function | P92 input pin | P92 output pin |
| | $\overline{\text{IRQ0}}$ input pin | |

When bit IRQ0E in IER is set to 1, this pin is used as the $\overline{\text{IRQ0}}$ input pin.

P91/$\overline{\text{IRQ1}}$

| P91DDR | 0 | 1 |
|---|---|---|
| Pin function | P91 input pin | P91 output pin |
| | $\overline{\text{IRQ1}}$ input pin | |

When bit IRQ1E in IER is set to 1, this pin is used as the $\overline{\text{IRQ1}}$ input pin.

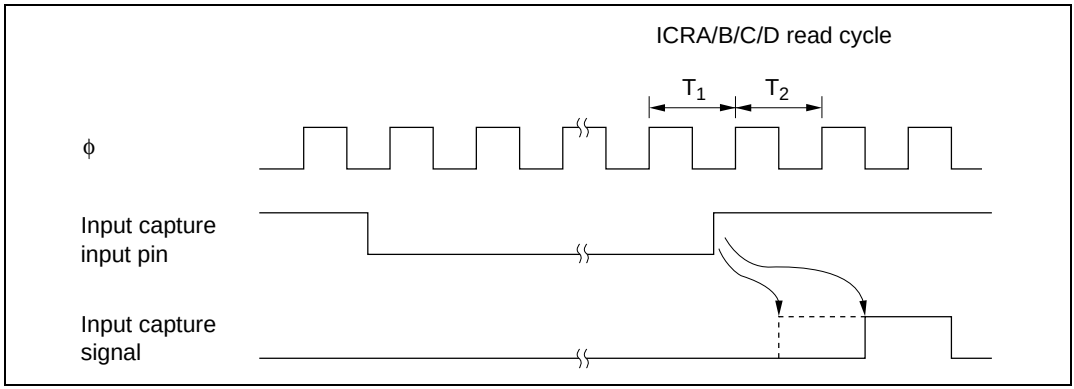



**Figure 11.8 Input Capture Signal Timing (Input Capture Input when ICRA/B/C/D Is Read)**

### Buffered Input Capture Input Timing

ICRC and ICRD can operate as buffers for ICRA and ICRB.

Figure 11.9 shows how input capture operates when ICRA and ICRC are used in buffer mode and IEDGA and IEDGC are set to different values (IEDGA = 0 and IEDGC = 1, or IEDG A = 1 and IEDGC = 0), so that input capture is performed on both the rising and falling edges of FTIA.

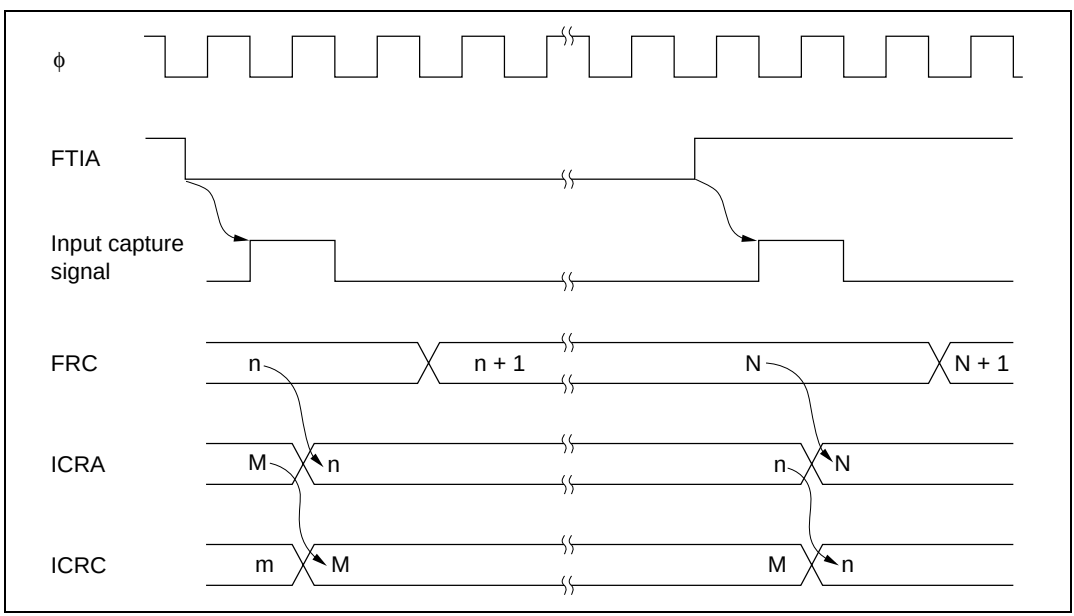



**Figure 11.9 Buffered Input Capture Timing (Usual Case)**

**Contention between FRC Write and Increment**

If an FRC increment pulse is generated during the state after an FRC write cycle, the write takes priority and FRC is not incremented.

Figure 11.19 shows this type of contention.

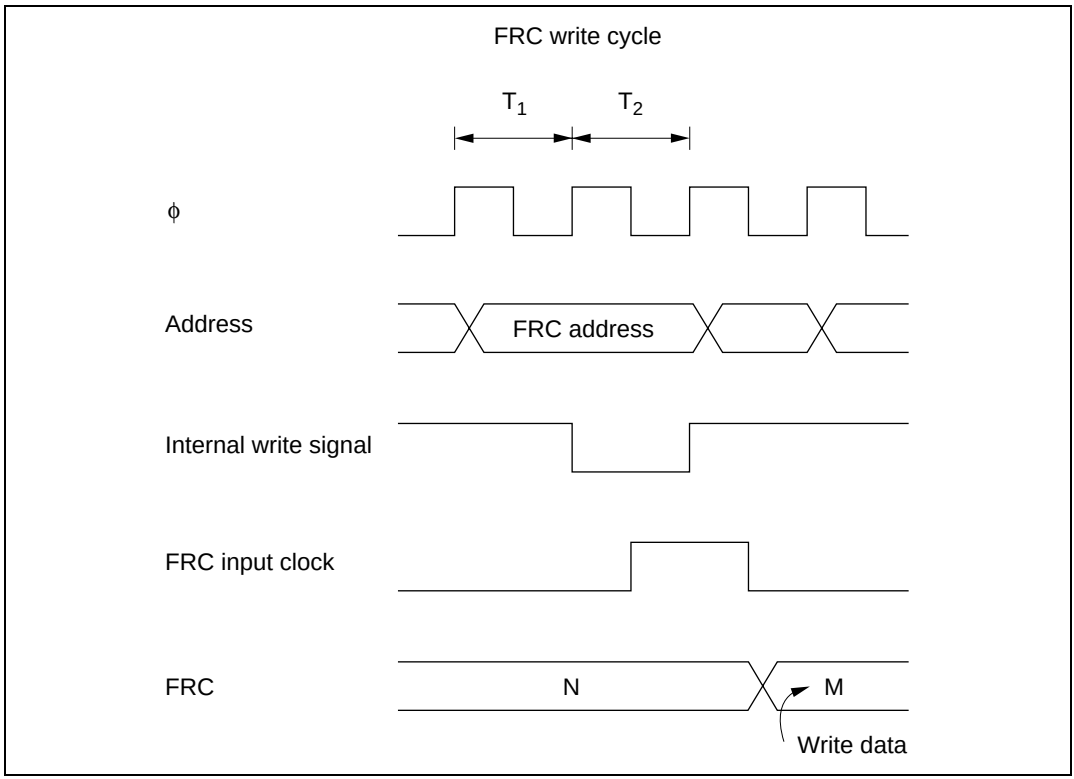



**Figure 11.19 FRC Write-Increment Contention**

**Contention between OCR Write and Compare-Match**

If a compare-match occurs during the state after an OCRA or OCRB write cycle, the write takes priority and the compare-match signal is inhibited.

Figure 11.20 shows this type of contention.

### Clock

Either an internal clock generated by the built-in baud rate generator or an external clock input at the SCK pin can be selected as the SCI's serial clock, according to the setting of the C/$\overline{A}$ bit in SMR and the CKE1 and CKE0 bits in SCR. For details of SCI clock source selection, see table 15.9.

When an external clock is input at the SCK pin, the clock frequency should be 16 times the bit rate used.

When the SCI is operated on an internal clock, the clock can be output from the SCK pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is at the center of each transmit data bit, as shown in figure 15.3.

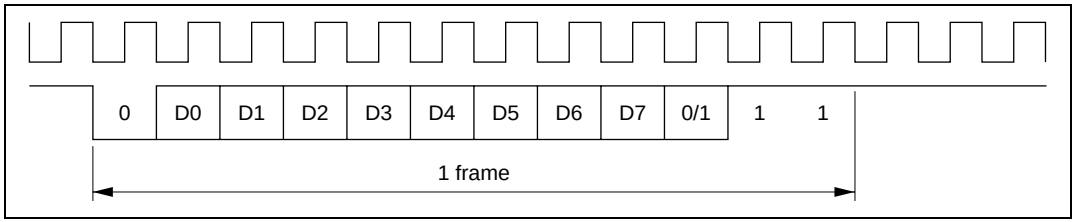



**Figure 15.3 Relation between Output Clock and Transfer Data Phase (Asynchronous Mode)**

### Data Transfer Operations

**SCI Initialization (Asynchronous Mode):** Before transmitting and receiving data, first clear the TE and RE bits in SCR to 0, then initialize the SCI as described below.

When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1 and TSR is initialized. Note that clearing the RE bit to 0 does not change the contents of the RDRF, PER, FER, and ORER flags, or the contents of RDR.

When an external clock is used the clock should not be stopped during operation, including initialization, since operation is uncertain.

ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is divided internally into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). ICDRS cannot be read or written by the CPU, ICDRR is read-only, and ICDRT is write-only. Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the status of internal flags such as TDRE and RDRF.

If IIC is in transmit mode and the next data is in ICDRT (the TDRE flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRT to ICDRS. If IIC is in receive mode and no previous data remains in ICDRR (the RDRF flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRS to ICDRR.

If the number of bits in a frame, excluding the acknowledge bit, is less than 8, transmit data and receive data are stored differently. Transmit data should be written justified toward the MSB side when MLS = 0, and toward the LSB side when MLS = 1. Receive data bits read from the LSB side should be treated as valid when MLS = 0, and bits read from the MSB side when MLS = 1.

ICDR is assigned to the same address as SARX, and can be written and read only when the ICE bit is set to 1 in ICCR.

The value of ICDR is undefined after a reset.

The TDRE and RDRF flags are set and cleared under the conditions shown below. Setting the TDRE and RDRF flags affects the status of the interrupt flags.

**Bit 7—Error Stop Condition Detection Flag (ESTP):** Indicates that a stop condition has been detected during frame transfer in I²C bus format slave mode.

**Bit 7**

| ESTP | Description | |
|---|---|---|
| 0 | No error stop condition<br>[Clearing conditions]<br>1. When 0 is written in ESTP after reading ESTP = 1<br>2. When the IRIC flag is cleared to 0 | (Initial value) |
| 1 | • In I²C bus format slave mode<br>Error stop condition detected<br>[Setting condition]<br>When a stop condition is detected during frame transfer<br>• In other modes<br>No meaning | |

**Bit 6—Normal Stop Condition Detection Flag (STOP):** Indicates that a stop condition has been detected after completion of frame transfer in I²C bus format slave mode.

**Bit 6**

| STOP | Description | |
|---|---|---|
| 0 | No normal stop condition<br>[Clearing conditions]<br>1. When 0 is written in STOP after reading STOP = 1<br>2. When the IRIC flag is cleared to 0 | (Initial value) |
| 1 | • In I²C bus format slave mode<br>Normal stop condition detected<br>[Setting condition]<br>When a stop condition is detected after completion of frame transfer<br>• In other modes<br>No meaning | |

**Bit 5—I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag (IRTR):** Indicates that the I²C bus interface has issued an interrupt request to the CPU, and the source is completion of reception/transmission of one frame in continuous transmission/reception for which DTC activation is possible. When the IRTR flag is set to 1, the IRIC flag is also set to 1 at the same time.

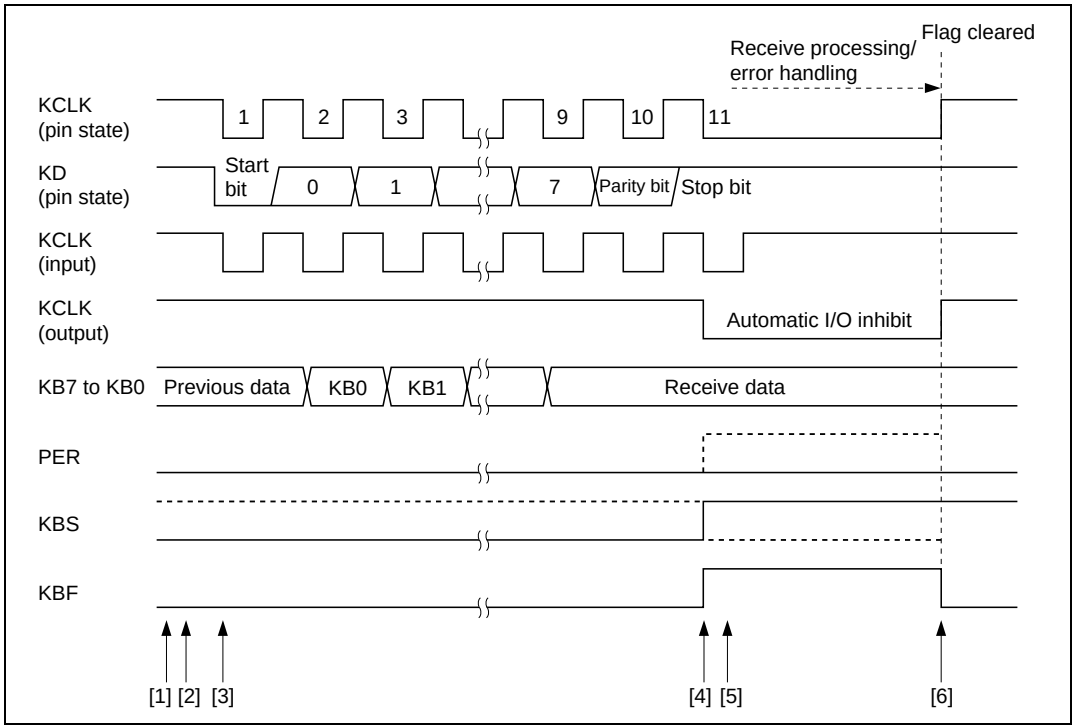



**Figure 17.4 Receive Timing**

### 17.3.2 Transmit Operation

In a transmit operation, KCLK (clock) is an output on the keyboard side, and KD (data) is an output on the H8S/2148 Group and H8S/2147N chip (system) side. KD outputs a start bit, 8 data bits (LSB-first), an odd parity bit, and a stop bit, in that order. The KD value is valid when KCLK is high. A sample transmit processing flowchart is shown in figure 17.5, and the transmit timing in figure 17.6.

## 26.2 Electrical Characteristics of H8S/2148 F-ZTAT

### 26.2.1 Absolute Maximum Ratings

Table 26.2 lists the absolute maximum ratings.

**Table 26.2 Absolute Maximum Ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage* | $V_{CC}$ | –0.3 to +7.0 | V |
| Input/output buffer power supply (power supply for the port A) | $V_{CC}B$ | –0.3 to +7.0 | V |
| Input voltage (except ports 6, 7, and A) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input not selected for port 6) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input not selected for port A) | $V_{in}$ | –0.3 to $V_{CC}B$ +0.3 | V |
| Input voltage (CIN input selected for port 6) | $V_{in}$ | –0.3 V to lower of voltages $V_{CC}$ +0.3 and $AV_{CC}$ +0.3 | V |
| Input voltage (CIN input selected for port A) | $V_{in}$ | –0.3 V to lower of voltages $V_{CC}B$ +0.3 and $AV_{CC}$ +0.3 | V |
| Input voltage (port 7) | $V_{in}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Reference supply voltage | $AV_{ref}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Analog power supply voltage | $AV_{CC}$ | –0.3 to +7.0 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Operating temperature | $T_{opr}$ | Regular specifications: –20 to +75 | °C |
| | | Wide-range specifications: –40 to +85 | °C |
| Operating temperature (flash memory programming/erasing) | $T_{opr}$ | Regular specifications: 0 to +75 | °C |
| | | Wide-range specifications: 0 to +85 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * Power supply voltage for VCC1 and VCC2 pins.

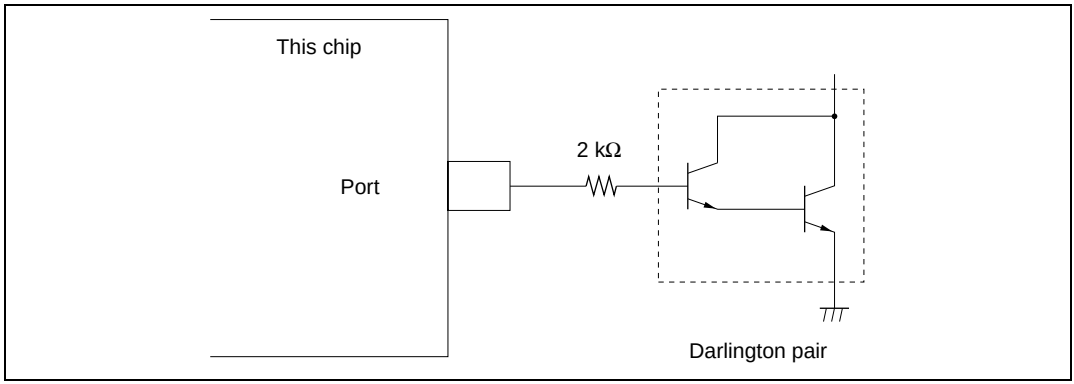



**Figure 26.1 Darlington Pair Drive Circuit (Example)**

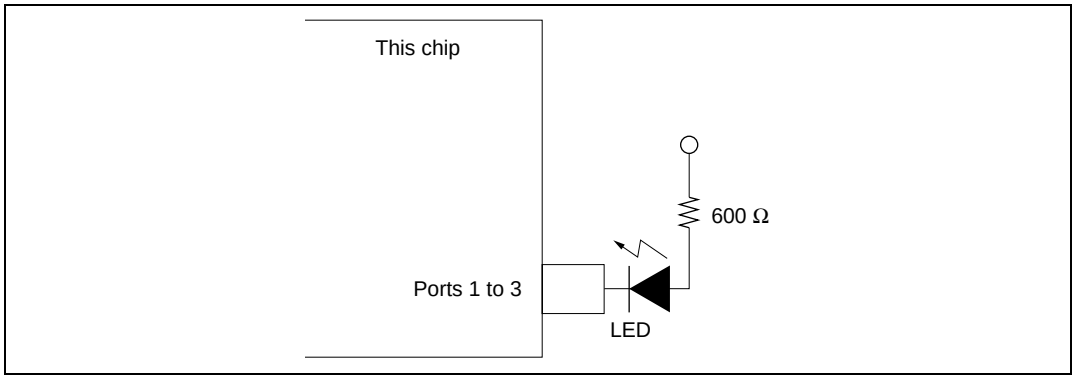



**Figure 26.2 LED Drive Circuit (Example)**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Operating temperature (flash memory programming/erasing) | $T_{opr}$ | Regular specifications: –20 to +75 | °C |
| | | Wide-range specifications: –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

Caution: 1. Permanent damage to the chip may result if absolute maximum ratings are exceeded.
2. Never apply more than 7.0 V to any of the pins of the 5- or 4-V version or 4.3 V to any of the pins (except port A) of the 3-V version

Notes: 1. Power supply voltage for VCC1 pin
Never exceed the maximum rating of $V_{CL}$ in the low-power version (3-V version) because both the VCC1 and VCL pins are connected to the $V_{CC}$ power supply.
2. It is an operating power supply voltage pin on the chip.
Never apply power supply voltage to the VCL pin in the 5- or 4-V version.
Always connect an external capacitor between the VCL pin and ground for internal voltage stabilization.

### 26.3.2 DC Characteristics

Table 26.17 lists the DC characteristics. Permitted output current values and bus drive characteristics are shown in tables 26.18 and 26.19, respectively.

**Table 26.17 DC Characteristics (1)**

Conditions: $V_{CC}$ = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, $AV_{CC}$*1 = 5.0 V ±10%, $AV_{ref}$*1 = 4.5 V to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$*1 = 0 V, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60(KWUL = 00)*2*6, $\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$*7*8, $\overline{\text{IRQ2}}$ to $\overline{\text{IRQ0}}$*3, $\overline{\text{IRQ5}}$ to $\overline{\text{IRQ3}}$ | (1) | $V_T^-$ | 1.0 | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$<br>$V_{CC}B \times 0.7$ | | |
| | | | $V_T^+ - V_T^-$ | 0.4 | — | — | | |
| Schmitt trigger input voltage (in level switching)*6 | P67 to P60 (KWUL = 01) | | $V_T^-$ | $V_{CC} \times 0.3$ | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$ | — | — | | |
| | P67 to P60 (KWUL = 10) | | $V_T^-$ | $V_{CC} \times 0.4$ | — | — | | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.8$ | | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.03$ | — | — | | |
| | P67 to P60 (KWUL = 11) | | $V_T^-$ | $V_{CC} \times 0.45$ | — | — | | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.9$ | | |
| | | | $V_T^+ - V_T^-$ | 0.05 | — | — | | |
| Input high voltage | $\overline{\text{RES}}$, $\overline{\text{STBY}}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC}$ –0.7 | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | | |
| | PA7 to PA0*7 | | | $V_{CC}B \times 0.7$ | — | $V_{CC}B$ +0.3 | | |
| | Port 7 | | | 2.0 | — | $AV_{CC}$ +0.3 | | |
| | Input pins except (1) and (2) above | | | 2.0 | — | $V_{CC}$ +0.3 | | |

**IER—IRQ Enable Register** **H'FFC2** **Interrupt Controller**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | IRQ7E | IRQ6E | IRQ5E | IRQ4E | IRQ3E | IRQ2E | IRQ1E | IRQ0E |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

IRQ7 to IRQ0 enable

| | |
|---|---|
| 0 | IRQn interrupt disabled |
| 1 | IRQn interrupt enabled |

(n = 7 to 0)

| | | |
|---|---|---|
| **TCORA0—Time Constant Register A0** | **H'FFCC** | **TMR0** |
| **TCORA1—Time Constant Register A1** | **H'FFCD** | **TMR1** |
| **TCORB0—Time Constant Register B0** | **H'FFCE** | **TMR0** |
| **TCORB1—Time Constant Register B1** | **H'FFCF** | **TMR1** |
| **TCORAY—Time Constant Register AY** | **H'FFF2** | **TMRY** |
| **TCORBY—Time Constant Register BY** | **H'FFF3** | **TMRY** |
| **TCORC—Time Constant Register C** | **H'FFF5** | **TMRX** |
| **TCORAX—Time Constant Register AX** | **H'FFF6** | **TMRX** |
| **TCORBX—Time Constant Register BX** | **H'FFF7** | **TMRX** |

TCORA0
TCORB0

TCORA1
TCORB1

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Initial value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Compare match flag (CMF) is set when TCOR and TCNT values match

TCORAX, TCORAY
TCORBX, TCORBY

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Initial value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Compare match flag (CMF) is set when TCOR and TCNT values match

TCORC

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Initial value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Compare match C signal is generated when sum of TCORC and TICR contents match TCNT value