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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b SAR; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2144vfa10v

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Pin No.	Pin Name			
	Expanded Modes		Single-Chip Modes	
FP-100B TFP-100B	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)	Flash Memory Writer Mode
72	A7	A7/P17	P17	FA7
73	A6	A6/P16	P16	FA6
74	A5	A5/P15	P15	FA5
75	A4	A4/P14	P14	FA4
76	A3	A3/P13	P13	FA3
77	A2	A2/P12	P12	FA2
78	A1	A1/P11	P11	FA1
79	A0	A0/P10	P10	FA0
80	PB3/D3	PB3/D3	PB3	NC
81	PB2/D2	PB2/D2	PB2	NC
82	D8	D8	P30	FO0
83	D9	D9	P31	FO1
84	D10	D10	P32	FO2
85	D11	D11	P33	FO3
86	D12	D12	P34	FO4
87	D13	D13	P35	FO5
88	D14	D14	P36	FO6
89	D15	D15	P37	FO7
90	PB1/D1	PB1/D1	PB1	NC
91	PB0/D0	PB0/D0	PB0	NC
92	VSS	VSS	VSS	VSS
93	P80	P80	P80	NC
94	P81	P81	P81	NC
95	P82	P82	P82	NC
96	P83	P83	P83	NC
97	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1	NC
98	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1	NC
99	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1	NC
100	$\overline{\text{RESO}}$	$\overline{\text{RESO}}$	$\overline{\text{RESO}}$	NC

2.6.2 Instructions and Addressing Modes

Table 2.2 indicates the combinations of instructions and addressing modes that the H8S/2000 CPU can use.

Table 2.2 Combinations of Instructions and Addressing Modes

Function	Instruction	Addressing Modes													
		#xx	Rn	@ERn	@(d:16,ERn)	@(d:32, ERn)	@–ERn/@ERn+	@aa:8	@aa:16	@aa:24	@aa:32	@(d:8, PC)	@(d:16, PC)	@@aa:8	|
Data transfer	MOV	BWL	BWL	BWL	BWL	BWL	BWL	B	BWL	—	BWL	—	—	—	—
	POP, PUSH	—	—	—	—	—	—	—	—	—	—	—	—	—	WL
	LDM*3, STM*3	—	—	—	—	—	—	—	—	—	—	—	—	—	L
	MOVFPE*1, MOVTPE*1	—	—	—	—	—	—	—	B	—	—	—	—	—	—
Arithmetic operations	ADD, CMP	BWL	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	SUB	WL	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	ADDX, SUBX	B	B	—	—	—	—	—	—	—	—	—	—	—	—
	ADDS, SUBS	—	L	—	—	—	—	—	—	—	—	—	—	—	—
	INC, DEC	—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	DAA, DAS	—	B	—	—	—	—	—	—	—	—	—	—	—	—
	MULXU, DIVXU	—	BW	—	—	—	—	—	—	—	—	—	—	—	—
	MULXS, DIVXS	—	BW	—	—	—	—	—	—	—	—	—	—	—	—
	NEG	—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	EXTU, EXTS	—	WL	—	—	—	—	—	—	—	—	—	—	—	—
	TAS*2	—	—	B	—	—	—	—	—	—	—	—	—	—	—
Logic operations	AND, OR, XOR	BWL	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	NOT	—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
Shift		—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
Bit-manipulation		—	B	B	—	—	—	B	B	—	B	—	—	—	—
Branch	Bcc, BSR	—	—	—	—	—	—	—	—	—	—	○	○	—	—
	JMP, JSR	—	—	—	—	—	—	—	—	○	—	—	—	○	—
	RTS	—	—	—	—	—	—	—	—	—	—	—	—	—	○

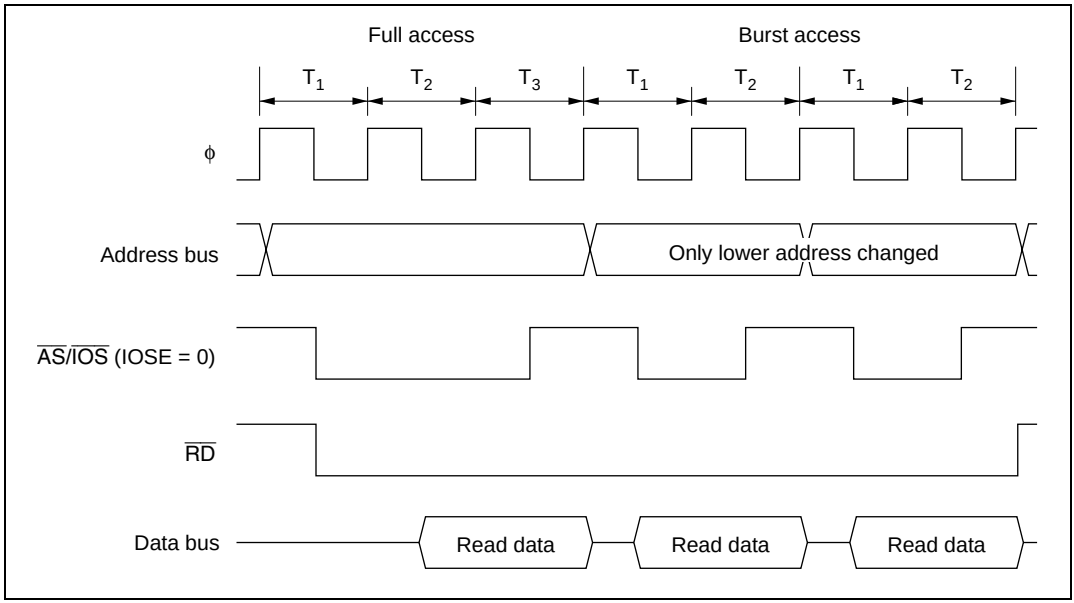


Figure 6.14 (a) Example of Burst ROM Access Timing (when AST = BRSTS1 = 1)

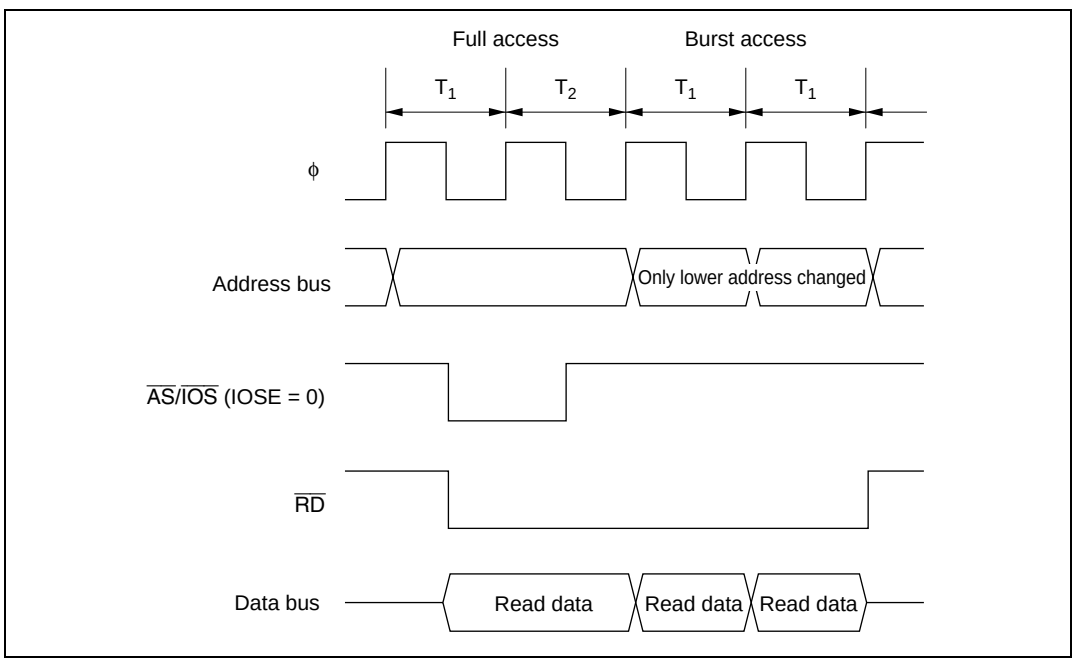


Figure 6.14 (b) Example of Burst ROM Access Timing (when AST = BRSTS1 = 0)

7.3.11 Procedures for Using the DTC

Activation by Interrupt

The procedure for using the DTC with interrupt activation is as follows:

1. Set the MRA, MRB, SAR, DAR, CRA, and CRB register information in the on-chip RAM.
2. Set the start address of the register information in the DTC vector address.
3. Set the corresponding bit in DTCER to 1.
4. Set the enable bits for the interrupt sources to be used as the activation sources to 1. The DTC is activated when an interrupt used as an activation source is generated.
5. After the end of one data transfer, or after the specified number of data transfers have ended, the DTCE bit is cleared to 0 and a CPU interrupt is requested. If the DTC is to continue transferring data, set the DTCE bit to 1.

Activation by Software

The procedure for using the DTC with software activation is as follows:

1. Set the MRA, MRB, SAR, DAR, CRA, and CRB register information in the on-chip RAM.
2. Set the start address of the register information in the DTC vector address.
3. Check that the SWDTE bit is 0.
4. Write 1 in the SWDTE bit and the vector number to DTVECR.
5. Check the vector number written to DTVECR.
6. After the end of one data transfer, if the DISEL bit is 0 and a CPU interrupt is not requested, the SWDTE bit is cleared to 0. If the DTC is to continue transferring data, set the SWDTE bit to 1. When the DISEL bit is 1, or after the specified number of data transfers have ended, the SWDTE bit is held at 1 and a CPU interrupt is requested.

16.1.4 Register Configuration

Table 16.2 summarizes the registers of the I²C bus interface.

Table 16.2 Register Configuration

Channel	Name	Abbreviation	R/W	Initial Value	Address*1
0	I²C bus control register	ICCR0	R/W	H'01	H'FFD8
	I²C bus status register	ICSR0	R/W	H'00	H'FFD9
	I²C bus data register	ICDR0	R/W	—	H'FFDE*2
	I²C bus mode register	ICMR0	R/W	H'00	H'FFDF*2
	Slave address register	SAR0	R/W	H'00	H'FFDF*2
	Second slave address register	SARX0	R/W	H'01	H'FFDE*2
1	I²C bus control register	ICCR1	R/W	H'01	H'FF88
	I²C bus status register	ICSR1	R/W	H'00	H'FF89
	I²C bus data register	ICDR1	R/W	—	H'FF8E*2
	I²C bus mode register	ICMR1	R/W	H'00	H'FF8F*2
	Slave address register	SAR1	R/W	H'00	H'FF8F*2
	Second slave address register	SARX1	R/W	H'01	H'FF8E*2
Common	Serial/timer control register	STCR	R/W	H'00	H'FFC3
	DDC switch register	DDCSWR	R/W	H'0F	H'FEE6
	Module stop control register	MSTPCRH	R/W	H'3F	H'FF86
		MSTPCRL	R/W	H'FF	H'FF87

Notes: 1. Lower 16 bits of the address.

2. The register that can be written or read depends on the ICE bit in the I²C bus control register. The slave address register can be accessed when ICE = 0, and the I²C bus mode register can be accessed when ICE = 1.

The I²C bus interface registers are assigned to the same addresses as other registers. Register selection is performed by means of the IICE bit in the serial/timer control register (STCR).

16.2.2 Slave Address Register (SAR)

Bit	7	6	5	4	3	2	1	0
	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SAR is an 8-bit readable/writable register that stores the slave address and selects the communication format. When the chip is in slave mode (and the addressing format is selected), if the upper 7 bits of SAR match the upper 7 bits of the first frame received after a start condition, the chip operates as the slave device specified by the master device. SAR is assigned to the same address as ICMR, and can be written and read only when the ICE bit is cleared to 0 in ICCR.

SAR is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 1—Slave Address (SVA6 to SVA0): Set a unique address in bits SVA6 to SVA0, differing from the addresses of other slave devices connected to the I²C bus.

Bit 0—Format Select (FS): Used together with the FSX bit in SARX and the SW bit in DDCSWR to select the communication format.

- I²C bus format: addressing format with acknowledge bit
- Synchronous serial format: non-addressing format without acknowledge bit, for master mode only
- Formatless mode (channel 0 only): non-addressing format with or without acknowledge bit, slave mode only, start/stop conditions not detected

The FS bit also specifies whether or not SAR slave address recognition is performed in slave mode.

Bit 7—Error Stop Condition Detection Flag (ESTP): Indicates that a stop condition has been detected during frame transfer in I²C bus format slave mode.

Bit 7

ESTP	Description	
0	No error stop condition [Clearing conditions] 1. When 0 is written in ESTP after reading ESTP = 1 2. When the IRIC flag is cleared to 0	(Initial value)
1	• In I²C bus format slave mode Error stop condition detected [Setting condition] When a stop condition is detected during frame transfer • In other modes No meaning	

Bit 6—Normal Stop Condition Detection Flag (STOP): Indicates that a stop condition has been detected after completion of frame transfer in I²C bus format slave mode.

Bit 6

STOP	Description	
0	No normal stop condition [Clearing conditions] 1. When 0 is written in STOP after reading STOP = 1 2. When the IRIC flag is cleared to 0	(Initial value)
1	• In I²C bus format slave mode Normal stop condition detected [Setting condition] When a stop condition is detected after completion of frame transfer • In other modes No meaning	

Bit 5—I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag (IRTR): Indicates that the I²C bus interface has issued an interrupt request to the CPU, and the source is completion of reception/transmission of one frame in continuous transmission/reception for which DTC activation is possible. When the IRTR flag is set to 1, the IRIC flag is also set to 1 at the same time.

Table 18.7 Fast A20 Gate Output Signal

HA0	Data/Command	Internal CPU Interrupt Flag	GA20 (P81)	Remarks
1	H'D1 command	0	Q	Turn-on sequence
0	1 data*1	0	1	
1	H'FF command	0	Q (1)	
1	H'D1 command	0	Q	Turn-off sequence
0	0 data*2	0	0	
1	H'FF command	0	Q (0)	
1	H'D1 command	0	Q	Turn-on sequence
0	1 data*1	0	1	(abbreviated form)
1/0	Command other than H'FF and H'D1	1	Q (1)	
1	H'D1 command	0	Q	Turn-off sequence
0	0 data*2	0	0	(abbreviated form)
1/0	Command other than H'FF and H'D1	1	Q (0)	
1	H'D1 command	0	Q	Cancelled sequence
1	Command other than H'D1	1	Q	
1	H'D1 command	0	Q	Retriggered sequence
1	H'D1 command	0	Q	
1	H'D1 command	0	Q	Consecutively executed
0	Any data	0	1/0	sequences
1	H'D1 command	0	Q(1/0)	

Notes: 1. Arbitrary data with bit 1 set to 1.
2. Arbitrary data with bit 1 cleared to 0.

18.3.4 Host Interface Pin Shutdown Function

Host interface output can be placed in the high-impedance state according to the state of the HIFSD pin. Setting the SDE bit to 1 in the SYSCR2 register enables the HIFSD pin is slave mode. The HIF constantly monitors the HIFSD pin, and when this pin goes low, places the host interface output pins (HIRQ1, HIRQ11, HIRQ12, HIRQ3, HIRQ4, and GA20) in the high-impedance state. At the same time, the host interface input pins ($\overline{CS1}$, $\overline{CS2}$ or $\overline{ECS2}$, $\overline{CS3}$, $\overline{CS4}$, $\overline{IOW}$, $\overline{IOR}$, and HA0) are disabled (fixed at the high input state internally) regardless of the pin states, and the signals of the multiplexed functions of these pins (input block) are similarly fixed internally. As a result, the host interface I/O pins (HDB7 to HDB0) also go to the high-impedance state.

This state is maintained while the HIFSD pin is low, and when the HIFSD pin returns to the high-level state, the pins are restored to their normal operation as host interface pins.

Bit 7—A/D End Flag (ADF): Status flag that indicates the end of A/D conversion.

Bit 7

ADF	Description	
0	[Clearing conditions]	(Initial value)
	• When 0 is written in the ADF flag after reading ADF = 1	
	• When the DTC is activated by an ADI interrupt and ADDR is read	
1	[Setting conditions]	
	• Single mode: When A/D conversion ends	
	• Scan mode: When A/D conversion ends on all specified channels	

Bit 6—A/D Interrupt Enable (ADIE): Selects enabling or disabling of interrupt (ADI) requests at the end of A/D conversion.

Bit 6

ADIE	Description	
0	A/D conversion end interrupt (ADI) request is disabled	(Initial value)
1	A/D conversion end interrupt (ADI) request is enabled	

Bit 5—A/D Start (ADST): Selects starting or stopping of A/D conversion. Holds a value of 1 during A/D conversion.

The ADST bit can be set to 1 by software, a timer conversion start trigger, or the A/D external trigger input pin ($\overline{\text{ADTRG}}$).

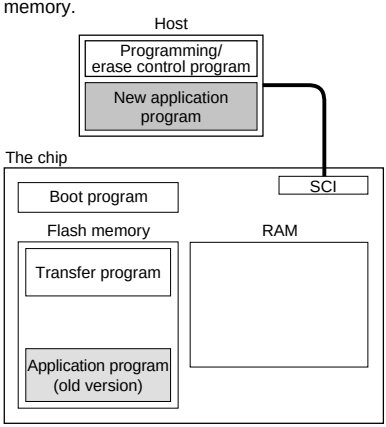
Bit 5

ADST	Description	
0	A/D conversion stopped	(Initial value)
1	Single mode: A/D conversion is started. Cleared to 0 automatically when conversion on the specified channel ends	
	Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode	

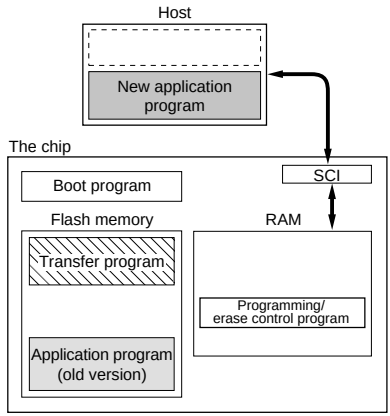
Bit 4—Scan Mode (SCAN): Selects single mode or scan mode as the A/D conversion operating mode. See section 20.4, Operation, for single mode and scan mode operation. Only set the SCAN bit while conversion is stopped.

- User program mode

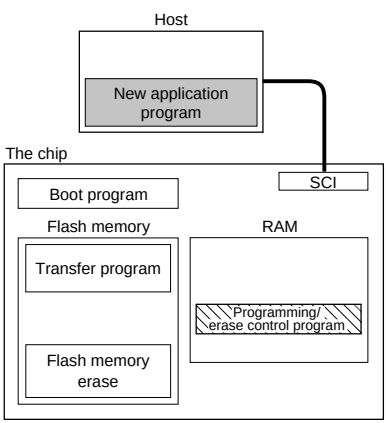
1. Initial state
   (1) The program that will transfer the programming/ erase control program to on-chip RAM should be written into the flash memory by the user beforehand.
   (2) The programming/erase control program should be prepared in the host or in the flash memory.



2. Programming/erase control program transfer
   Executes the transfer program in the flash memory, and transfers the programming/erase control program to RAM.



3. Flash memory initialization
   The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.



4. Writing new application program
   Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.

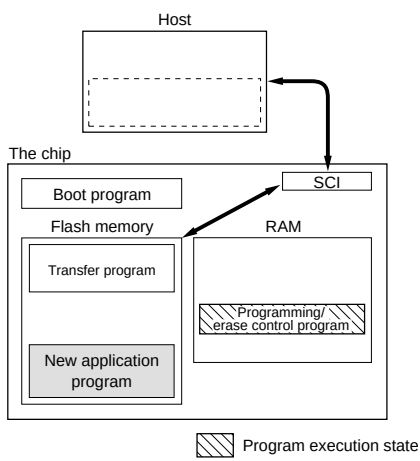


Figure 22.5 User Program Mode (Example)

Automatic SCI Bit Rate Adjustment

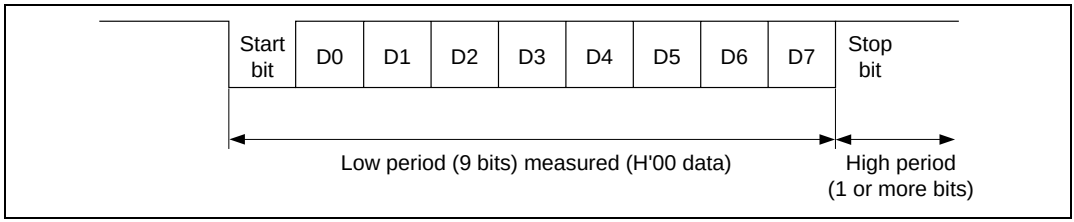


Figure 23.9 Automatic SCI Bit Rate Adjustment

When boot mode is initiated, the chip measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The chip calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the chips system clock frequency, there will be a discrepancy between the bit rates of the host and the chip. To ensure correct SCI operation, the host's transfer bit rate should be set to (4800, 9600, or 19200) bps.

Table 23.7 shows typical host transfer bit rates and system clock frequencies for which automatic adjustment of the chips bit rate is possible. The boot program should be executed within this system clock range.

Table 23.7 System Clock Frequencies for Which Automatic Adjustment of the Chips Bit Rate Is Possible

Host Bit Rate	System Clock Frequency for Which Automatic Adjustment of Bit Rate Is Possible
19200 bps	8 MHz to 20 MHz
9600 bps	4 MHz to 20 MHz
4800 bps	2 MHz to 18 MHz

On-Chip RAM Area Divisions in Boot Mode

In boot mode, the 1920-byte area from H'(FF)E880 to H'(FF) EFFF and the 128-byte area from H'(FF)FF00 to H'(FF)FF7F is reserved for use by the boot program, as shown in figure 23.10. The area to which the programming control program is transferred is H'(FF)E080 to H'(FF)E87F (2048 bytes). In the 64-kbyte version, this is a reserved area that is used only during the boot mode. However, the 8-byte area from H'(FF)E080 to H'(FF)E087 is reserved for ID codes as shown in

23.10.2 Socket Adapters and Memory Map

In programmer mode, a socket adapter is mounted on the writer programmer to match the package concerned. Socket adapters are available for each writer manufacturer supporting Renesas Technology microcomputer device types with 128-kbyte or 64-kbyte on-chip flash memory (V_{pp} = 3.3 V).

Figure 23.15 shows the memory map in programmer mode. For pin names in programmer mode, see section 1.3.2, Pin Functions in Each Operating Mode.

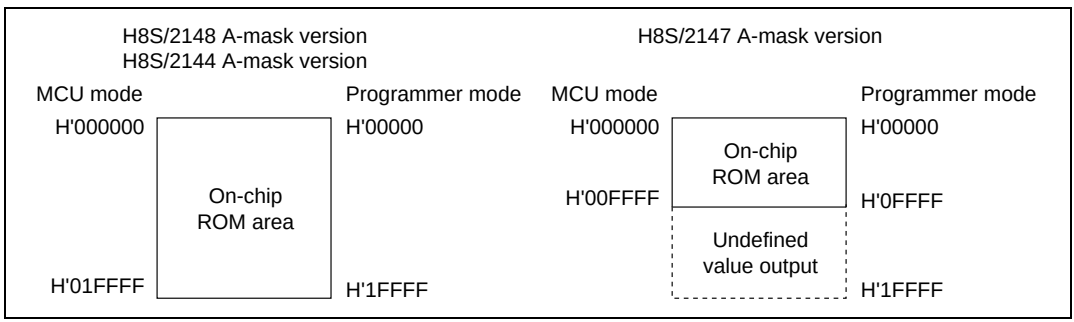


Figure 23.15 Memory Map in Programmer Mode

23.10.3 Programmer Mode Operation

Table 23.11 shows how the different operating modes are set when using programmer mode, and table 23.12 lists the commands used in programmer mode. Details of each mode are given below.

- Memory Read Mode

  Memory read mode supports byte reads.
- Auto-Program Mode

  Auto-program mode supports programming of 128 bytes at a time. Status polling is used to confirm the end of auto-programming.
- Auto-Erase Mode

  Auto-erase mode supports automatic erasing of the entire flash memory. Status polling is used to confirm the end of auto-erasing.
- Status Read Mode

  Status polling is used for auto-programming and auto-erasing, and normal termination can be confirmed by reading the FO6 signal. In status read mode, error information is output if an error occurs.

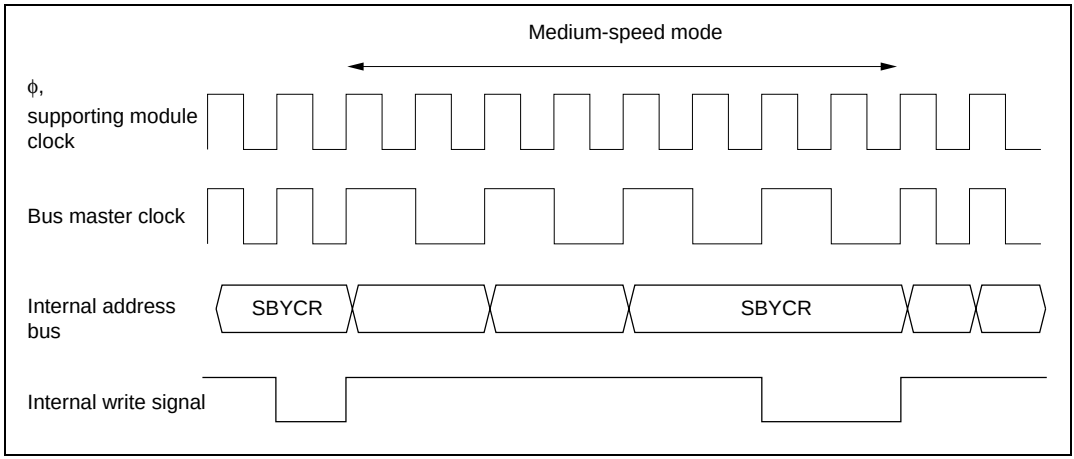


Figure 25.2 Medium-Speed Mode Transition and Clearance Timing

25.4 Sleep Mode

25.4.1 Sleep Mode

If a SLEEP instruction is executed when the SSBY bit in SBYCR and the LSON bit in LPWRCR are both cleared to 0, the CPU enters sleep mode. In sleep mode, CPU operation stops but the contents of the CPU's internal registers are retained. Other supporting modules do not stop.

25.4.2 Clearing Sleep Mode

Sleep mode is cleared by any interrupt, or with the $\overline{\text{RES}}$ pin or $\overline{\text{STBY}}$ pin.

Clearing with an Interrupt: When an interrupt request signal is input, sleep mode is cleared and interrupt exception handling is started. Sleep mode will not be cleared if interrupts are disabled, or if interrupts other than NMI have been masked by the CPU.

Clearing with the $\overline{\text{RES}}$ Pin: When the $\overline{\text{RES}}$ pin is driven low, the reset state is entered. When the $\overline{\text{RES}}$ pin is driven high after the prescribed reset input period, the CPU begins reset exception handling.

Clearing with the $\overline{\text{STBY}}$ Pin: When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode.

6. The upper limit of the port 6 applied voltage is V_{CC} +0.3 V when CIN input is not selected, and the lower of V_{CC} +0.3 V and AV_{CC} +0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
7. The upper limit of the port A applied voltage is $V_{CC}B$ +0.3 V when CIN input is not selected, and the lower of $V_{CC}B$ +0.3 V and AV_{CC} +0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
8. Port A characteristics depends on $V_{CC}B$ (or on V_{CC} when other pins are in output mode).
9. Current dissipation values are for V_{IH} min = V_{CC} –0.2 V, $V_{CC}B$ –0.2 V, and V_{IL} max = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.
10. The values are for $V_{RAM} \leq V_{CC} < 4.5V$, V_{IH} min = V_{CC} –0.2 V, $V_{CC}B$ –0.2 V, and V_{IL} max = 0.2 V.

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1 to 6, 8, 9, A, B	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	5	—	150	µA	V_{in} = 0 V, V_{CC} = 2.7 V to 3.6 V
	Ports 6, A, B		30	—	300	µA	
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50	pF	
	P52, P97, P42, P86, PA7 to PA2		—	—	20	pF	
	Input pins except (4) above		—	—	15	pF	
Current dissipation*6	Normal operation	I_{CC}	—	30	40	mA	f = 10 MHz
	Sleep mode		—	20	32	mA	
	Standby mode*7		—	1.0	5.0	µA	$T_a \leq 50°C$
			—	—	20.0	µA	$50°C < T_a$
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 3.6 V
Reference power supply current	During A/D conversion	AI_{ref}	—	0.5	1.0	mA	
	During A/D, D/A conversion		—	2.0	5.0	mA	
	Idle		—	0.01	5.0	µA	AV_{ref} = 2.0 V to AV_{CC}
Analog power supply voltage*1		AV_{CC}	2.7	—	3.6	V	Operating
			2.0	—	3.6	V	Idle/not used
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **Do not leave the AVCC, AV_{ref}, and AVSS pins open even if the A/D converter and D/A converter are not used.**

Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 3.6 V to AVCC and AV_{ref} pins by connection to the power supply (V_{CC}), or some other method. Ensure that $AV_{ref} \leq AV_{CC}$.

2. P67 to P60 include supporting module inputs multiplexed on those pins.
3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

Appendix A Instruction Set

A.1 Instruction

Operation Notation

Rd	General register (destination)*1
Rs	General register (source)*1
Rn	General register*1
ERn	General register (32-bit register)
MAC	Multiply-and-accumulate register (32-bit register)*2
(EAd)	Destination operand
(EAs)	Source operand
EXR	Extend register
CCR	Condition code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Exclusive logical OR
→	Transfer from left-hand operand to right-hand operand, or transition from left-hand state to right-hand state
¬	NOT (logical complement)
( ) < >	Operand contents
:8/:16/:24/:32	8-, 16-, 24-, or 32-bit length

Notes: 1. General registers include 8-bit registers (R0H to R7H, R0L to R7L), 16-bit registers (R0 to R7, E0 to E7), and 32-bit registers (ER0 to ER7).
2. MAC instructions cannot be used in this LSI.

MSTPCRH—Module Stop Control Register H **H'FF86** **System**
MSTPCRL—Module Stop Control Register L **H'FF87** **System**

	MSTPCRH								MSTPCRL							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Module stop

0	Module stop mode is cleared
1	Module stop mode is set

The correspondence between MSTPCR bits and on-chip supporting modules is shown below.

Register	Bit	Module
MSTPCRH	MSTP15	—
	MSTP14*	Data transfer controller (DTC)
	MSTP13	16-bit free-running timer (FRT)
	MSTP12	8-bit timers (TMR0, TMR1)
	MSTP11	8-bit PWM timer (PWM), 14-bit PWM timer (PWMX)
	MSTP10	D/A converter
	MSTP9	A/D converter
	MSTP8	8-bit timers (TMRX, TMRY), timer connection
MSTPCRL	MSTP7	Serial communication interface 0 (SCI0)
	MSTP6	Serial communication interface 1 (SCI1)
	MSTP5	Serial communication interface 2 (SCI2)
	MSTP4*	I^2C bus interface (IIC) channel 0 (option)
	MSTP3*	I^2C bus interface (IIC) channel 1 (option)
	MSTP2*	Host interface (HIF), keyboard buffer controller (PS2)
	MSTP1*	—
	MSTP0*	—

Notes: Do not set bit 15 to 1. Bits 1 and 0 can be read and written but do not affect operation.
* Must be set to 1 in the H8S/2144 Group.

ICMR1—I²C Bus Mode Register 1 **H'FF8F** **IIC1**
ICMR0—I²C Bus Mode Register 0 **H'FFDF** **IIC0**

Bit	7	6	5	4	3	2	1	0
	MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit counter

BC2	BC1	BC0	Synchronous serial format	I²C bus format
0	0	0	8	9
		1	1	2
	1	0	2	3
		1	3	4
1	0	0	4	5
		1	5	6
	1	0	6	7
		1	7	8

Serial clock select

IICX	CKS2	CKS1	CKS0	Clock
0	0	0	0	φ/28
			1	φ/40
		1	0	φ/48
			1	φ/64
	1	0	0	φ/80
			1	φ/100
		1	0	φ/112
			1	φ/128
1	0	0	0	φ/56
			1	φ/80
		1	0	φ/96
			1	φ/128
	1	0	0	φ/160
			1	φ/200
		1	0	φ/224
			1	φ/256

Wait insertion bit

0	Data and acknowledge bits transferred consecutively
1	Wait inserted between data and acknowledge bits

MSB-first/LSB-first select*

0	MSB-first
1	LSB-first

Note: * Do not set this bit to 1 when the I²C bus format is used.

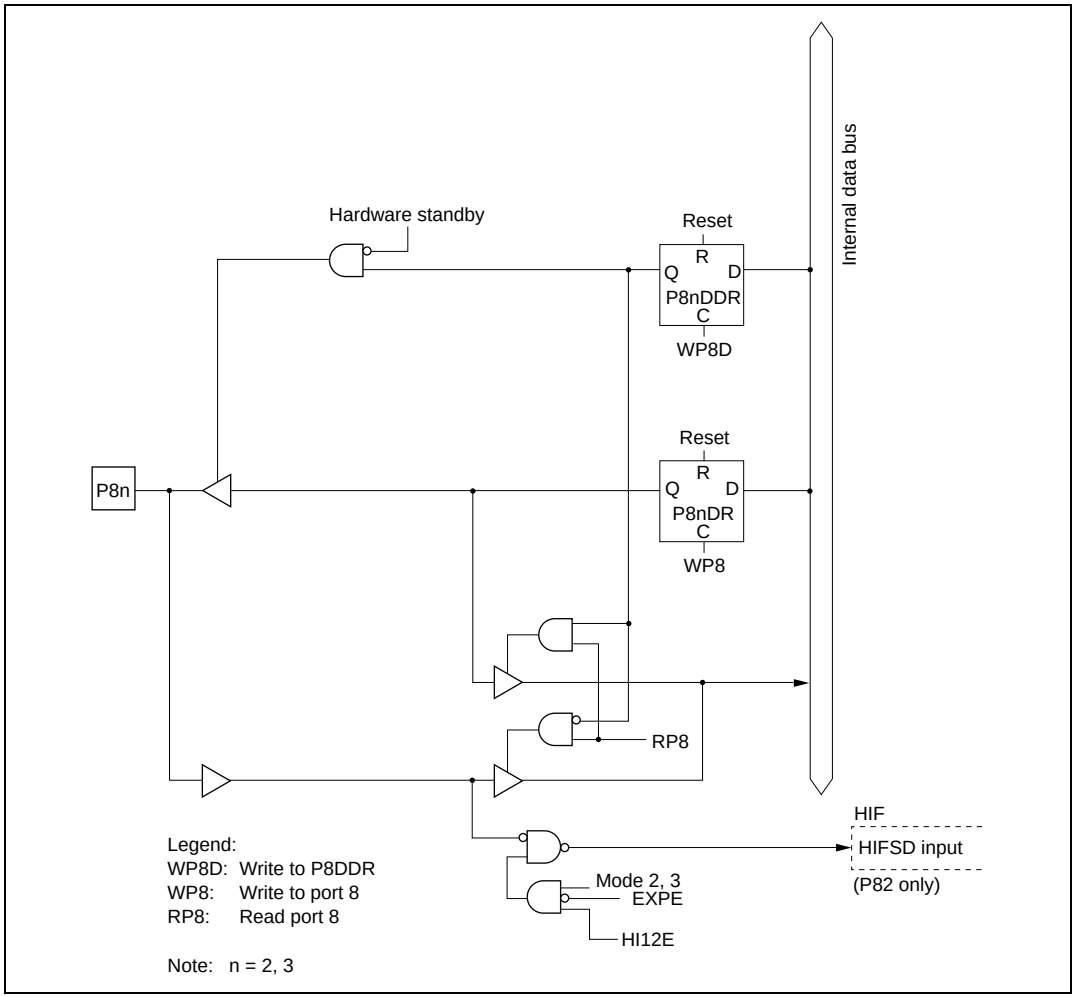


Figure C.25 Port 8 Block Diagram (Pins P82, P83)