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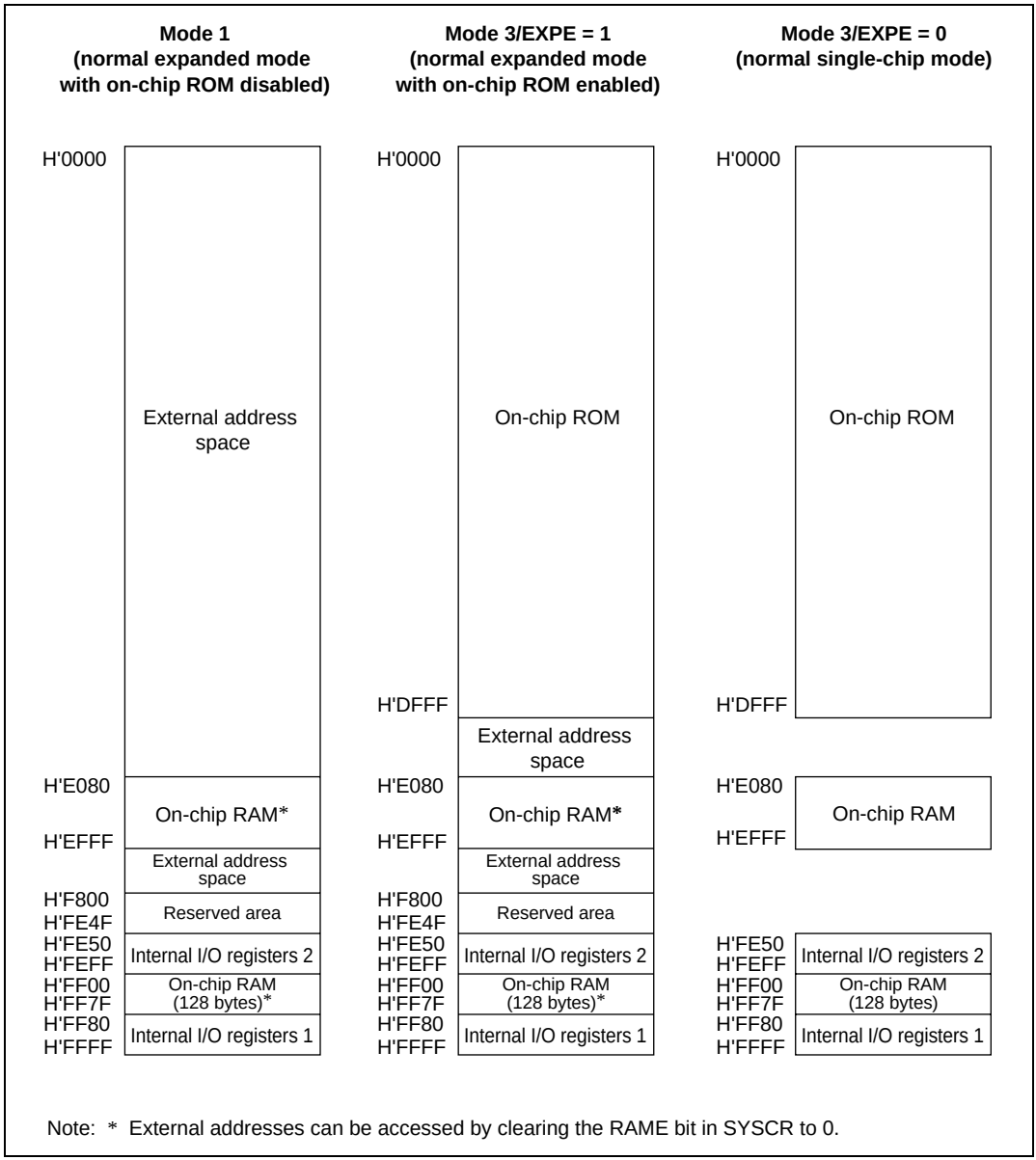
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2148afa20v

Item	Specifications
Bus controller	• 2-state or 3-state access space can be designated for external expansion areas • Number of program wait states can be set for external expansion areas
Data transfer controller (DTC) (H8S/2148 Group)	• Can be activated by internal interrupt or software • Multiple transfers or multiple types of transfer possible for one activation source • Transfer possible in repeat mode, block transfer mode, etc. • Request can be sent to CPU for interrupt that activated DTC
16-bit free-running timer module (FRT: 1 channel)	• One 16-bit free-running counter (also usable for external event counting) • Two output compare outputs • Four input capture inputs (with buffer operation capability)
8-bit timer module (2 channels: TMR0, TMR1)	Each channel has: • One 8-bit up-counter (also usable for external event counting) • Two timer constant registers • The two channels can be connected
Timer connection and 8-bit timer module (TMR) (2 channels: TMRX, TMRY) (Timer connection and TMRX provided in H8S/2148 Group)	Input/output and FRT, TMR1, TMRX, TMRY can be interconnected • Measurement of input signal or frequency-divided waveform pulse width and cycle (FRT, TMR1) • Output of waveform obtained by modification of input signal edge (FRT, TMR1) • Determination of input signal duty cycle (TMRX) • Output of waveform synchronized with input signal (FRT, TMRX, TMRY) • Automatic generation of cyclical waveform (FRT, TMRY)
Watchdog timer module (WDT: 2 channels)	• Watchdog timer or interval timer function selectable • Subclock operation capability (channel 1 only)
8-bit PWM timer (PWM) (H8S/2148 Group and H8S/2147N)	• Up to 16 outputs • Pulse duty cycle settable from 0 to 100% • Resolution: 1/256 • 1.25 MHz maximum carrier frequency (20-MHz operation)



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 3.2 H8S/2148 F-ZTAT A-Mask Version Memory Map in Each Operating Mode

12.1.2 Block Diagram

Figure 12.1 shows a block diagram of the 8-bit timer module (TMR0 and TMR1).

TMRX and TMRY have a similar configuration, but cannot be cascaded. TMRX also has an input capture function. For details, see section 13, Timer Connection.

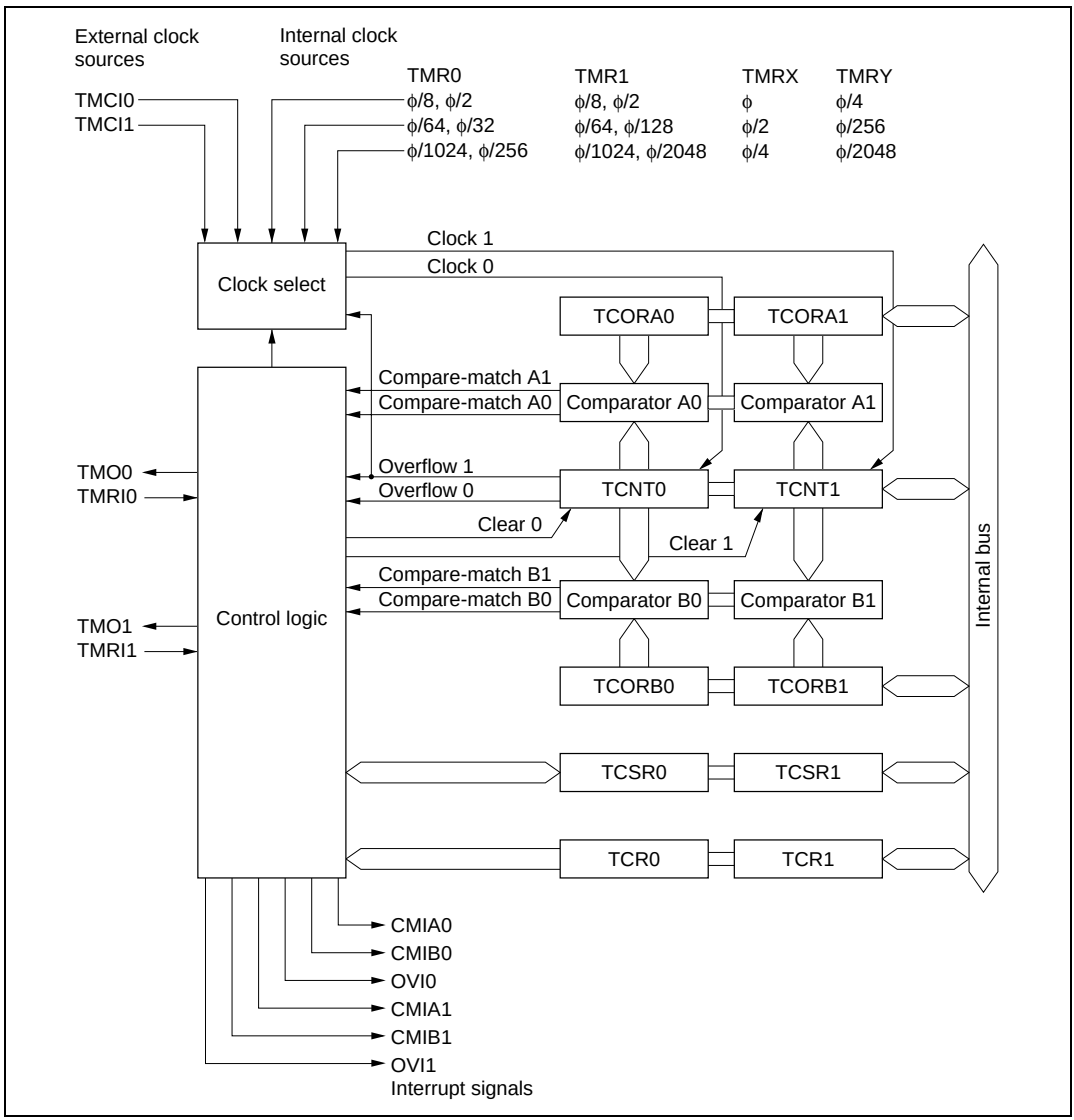


Figure 12.1 Block Diagram of 8-Bit Timer Module

DDCSWR Bit 6	SAR Bit 0	SARX Bit 0	
SW	**FS**	**FSX**	**Operating Mode**
0	0	0	I²C bus format • SAR and SARX slave addresses recognized
		1	I²C bus format (Initial value) • SAR slave address recognized • SARX slave address ignored
	1	0	I²C bus format • SAR slave address ignored • SARX slave address recognized
		1	Synchronous serial format • SAR and SARX slave addresses ignored
1	0	0	Formatless mode (start/stop conditions not detected)
	0	1	• Acknowledge bit used
	1	0	
	1	1	Formatless mode* (start/stop conditions not detected) • No acknowledge bit

Note: * Do not set this mode when automatic switching to the I²C bus format is performed by means of the DDCSWR setting.

16.2.3 Second Slave Address Register (SARX)

Bit	7	6	5	4	3	2	1	0
	SVAX6	SVAX5	SVAX4	SVAX3	SVAX2	SVAX1	SVAX0	FSX
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SARX is an 8-bit readable/writable register that stores the second slave address and selects the communication format. When the chip is in slave mode (and the addressing format is selected), if the upper 7 bits of SARX match the upper 7 bits of the first frame received after a start condition, the chip operates as the slave device specified by the master device. SARX is assigned to the same address as ICDR, and can be written and read only when the ICE bit is cleared to 0 in ICCR.

SARX is initialized to H'01 by a reset and in hardware standby mode.

(c) To confirm that the bus was not entered to the busy state while the MST bit is being set, check that the BBSY flag in the ICCR register is 0 immediately after the MST bit has been set.

- Notes on Interrupt Occurrence after ACKB Reception

— Conditions to cause this failure

The IRIC flag is set to 1 when both of the following conditions are satisfied.

- 1 is received as the acknowledge bit for transmit data and the ACKB bit in ICSR is set to 1
- Rising edge of the 9th transmit/receive clock is input to the SCL pin

When the above two conditions are satisfied in slave receive mode, an unnecessary interrupt occurs.

Figure 16.25 shows the note on interrupt occurrence in slave mode after receiving 1 as the acknowledge bit (ACKB = 1).

(1) For the last transmit data in master transmit mode or slave transmit mode, 1 is received as the acknowledge bit.

If the ACKE bit in ICCR is set to 1 at this time, the ACKB bit in ICSR is set to 1.

(2) After switching to slave receive mode, the start condition is input, and address reception is performed next.

(3) Even if the received address does not match the address set in SAR or SARX, the IRIC flag is set to 1 at the rise of the 9th transmit/receive clock, thus causing an interrupt to occur.

Note that if the slave address matches, an interrupt is to be generated at the rise of the 9th transmit/receive clock as normal operation, so this is not erroneous operation.

— Restriction

In a transmit operation of the I²C bus interface module, carry out the following countermeasures.

(1) After 1 is received as the acknowledge bit for transmit data, clear the ACKE bit in ICCR to 0 to clear the ACKB bit to 0.

(2) To enable acknowledge bit reception afterwards, set the ACKE bit to 1 again.

HICR2 Bit 2	HICR2 Bit 1	HICR Bit 2	HICR Bit 1	
IBFIE4	**IBFIE3**	**IBFIE2**	**IBFIE1**	**Description**
—	—	—	0	Input data register (IDR1) reception completed interrupt request disabled (Initial value)
—	—	—	1	Input data register (IDR1) reception completed interrupt request enabled
—	—	0	—	Input data register (IDR2) reception completed interrupt request disabled (Initial value)
—	—	1	—	Input data register (IDR2) reception completed interrupt request enabled
—	0	—	—	Input data register (IDR3) reception completed interrupt request disabled (Initial value)
—	1	—	—	Input data register (IDR3) reception completed interrupt request enabled
0	—	—	—	Input data register (IDR4) reception completed interrupt request disabled (Initial value)
1	—	—	—	Input data register (IDR4) reception completed interrupt request enabled

HICR Bit 0—Fast A20 Gate Function Enable (FGA20E): Enables or disables the fast A20 gate function. When the fast A20 gate is disabled, the normal A20 gate can be implemented byte firmware operation of the P81 output.

HICR Bit 0	
FGA20E	**Description**
0	Fast A20 gate function disabled (Initial value)
1	Fast A20 gate function enabled

HICR2 Bit 0—Reserved: Do not set this bit to 1.

20.1.2 Block Diagram

Figure 20.1 shows a block diagram of the A/D converter.

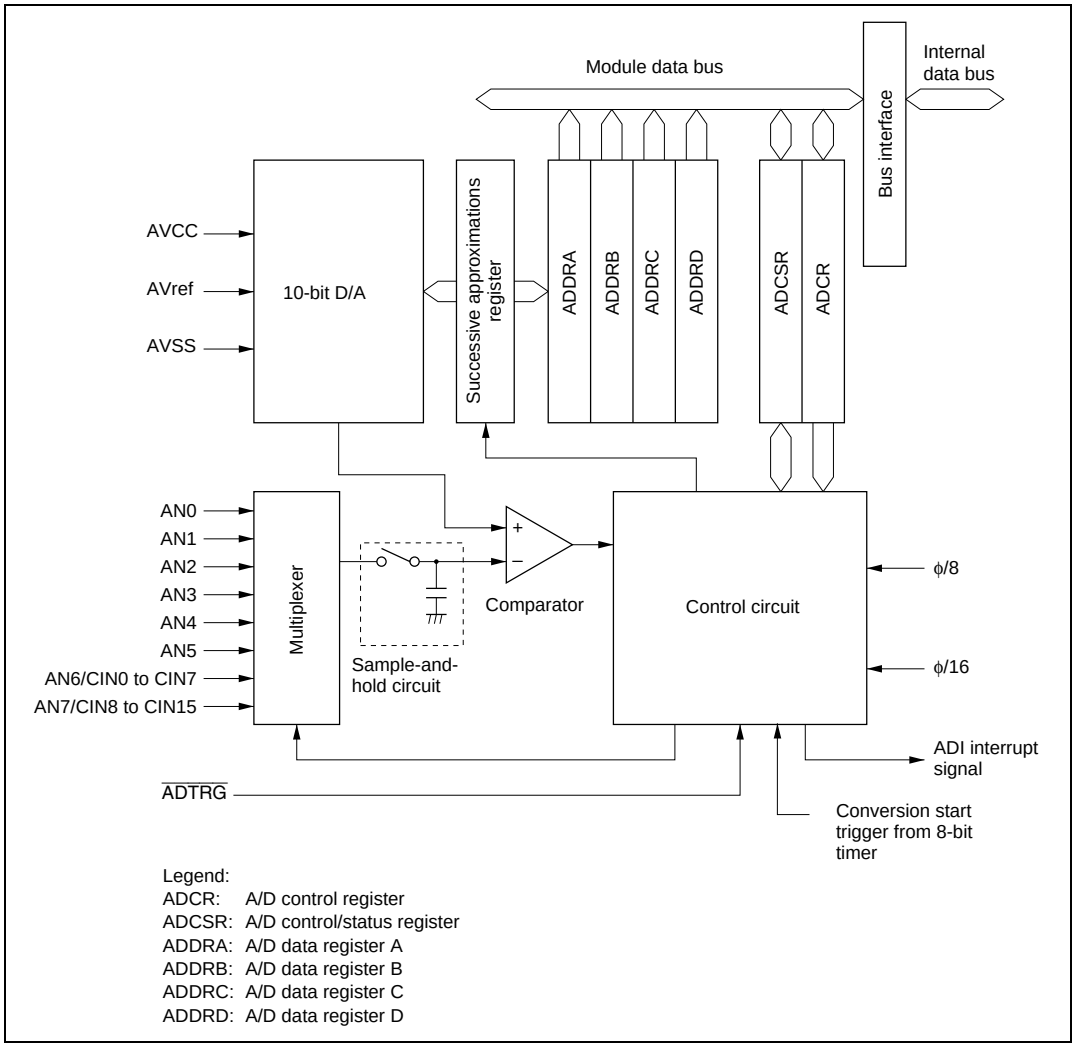


Figure 20.1 Block Diagram of A/D Converter

22.10.6 Auto-Erase Mode

AC Characteristics

Table 22.17 AC Characteristics in Auto-Erase Mode

Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, T_a = 25°C ±5°C

Item	Symbol	Min	Max	Unit
Command write cycle	t_{nxtc}	20	—	µs
$\overline{CE}$ hold time	t_{ceh}	0	—	ns
$\overline{CE}$ setup time	t_{ces}	0	—	ns
Data hold time	t_{dh}	50	—	ns
Data setup time	t_{ds}	50	—	ns
Write pulse width	t_{wep}	70	—	ns
Status polling start time	t_{ests}	1	—	ms
Status polling access time	t_{spa}	—	150	ns
Memory erase time	t_{erase}	100	40000	ms
$\overline{WE}$ rise time	t_r	—	30	ns
$\overline{WE}$ fall time	t_f	—	30	ns

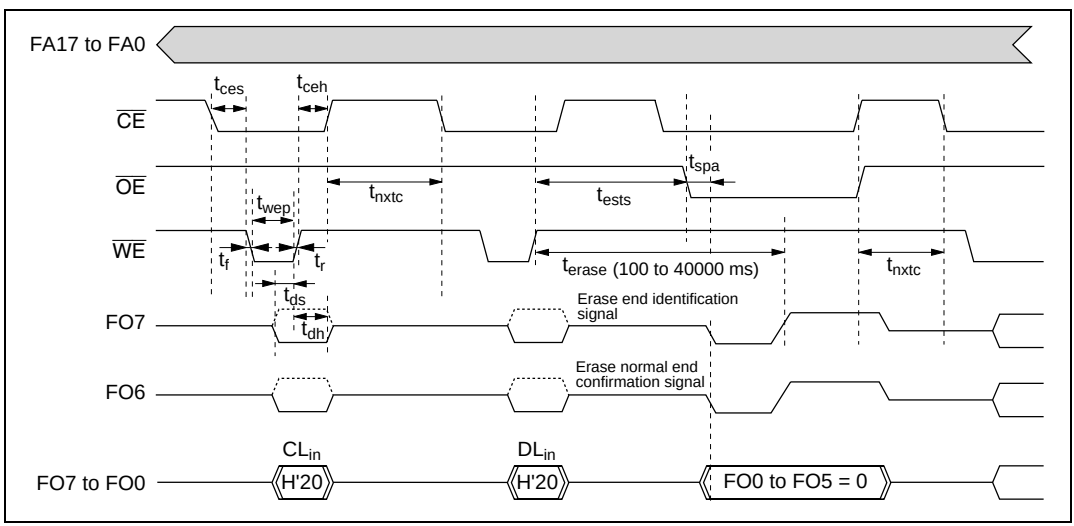


Figure 22.21 Auto-Erase Mode Timing Waveforms

Section 23 ROM (H8S/2148 F-ZTAT A-Mask Version, H8S/2147 F-ZTAT A-Mask Version, H8S/2144 F-ZTAT A-Mask Version)

23.1 Overview

H8S/2148 F-ZTAT A-mask version and H8S/2144 F-ZTAT A-mask version have 128 kbytes, and H8S/2147 F-ZTAT A-mask version has 64 kbytes of on-chip flash memory. The flash memory is connected to the bus master by a 16-bit data bus. The bus master accesses both byte and word data in one state, enabling faster instruction fetches and higher processing speed.

The mode pins (MD1 and MD0) and the EXPE bit in MDCR can be set to enable or disable the on-chip ROM.

The flash memory versions of this group can be erased and programmed on-board as well as with a general-purpose PROM programmer.

23.1.1 Block Diagram

Figure 23.1 shows a block diagram of the ROM.

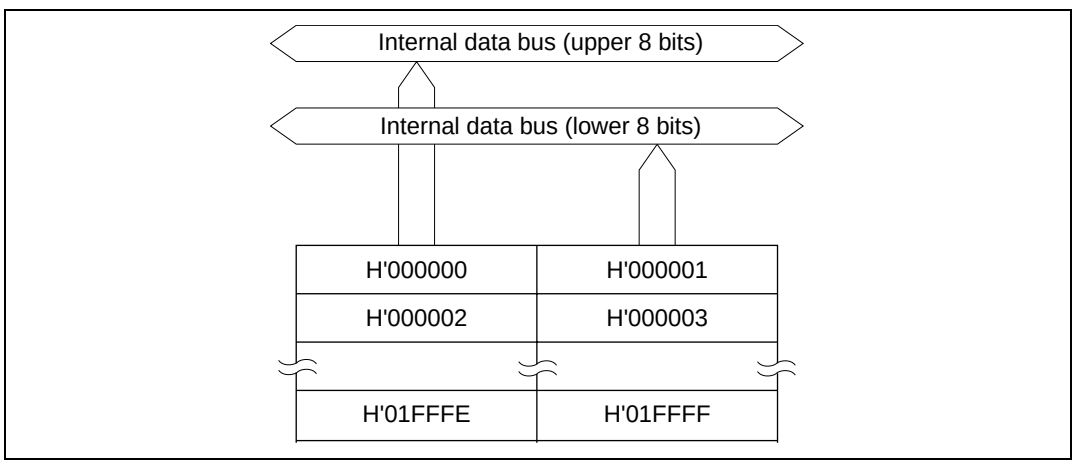


Figure 23.1 ROM Block Diagram
(A-mask versions of the H8S/2148 F-ZTAT and H8S/2144 F-ZTAT)

Table 23.9 Software Protection

Item	Description	Functions	
		Program	Erase
SWE bit protection	• Clearing the SWE bit to 0 in FLMCR1 sets the program/erase-protected state for all blocks. (Execute in on-chip RAM or external memory.)	Yes	Yes
Block specification protection	• Erase protection can be set for individual blocks by settings in erase block registers 1 and 2 (EBR1, EBR2). • Setting EBR1 and EBR2 to H'00 places all blocks in the erase-protected state.	—	Yes

23.8.3 Error Protection

In error protection, an error is detected when MCU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

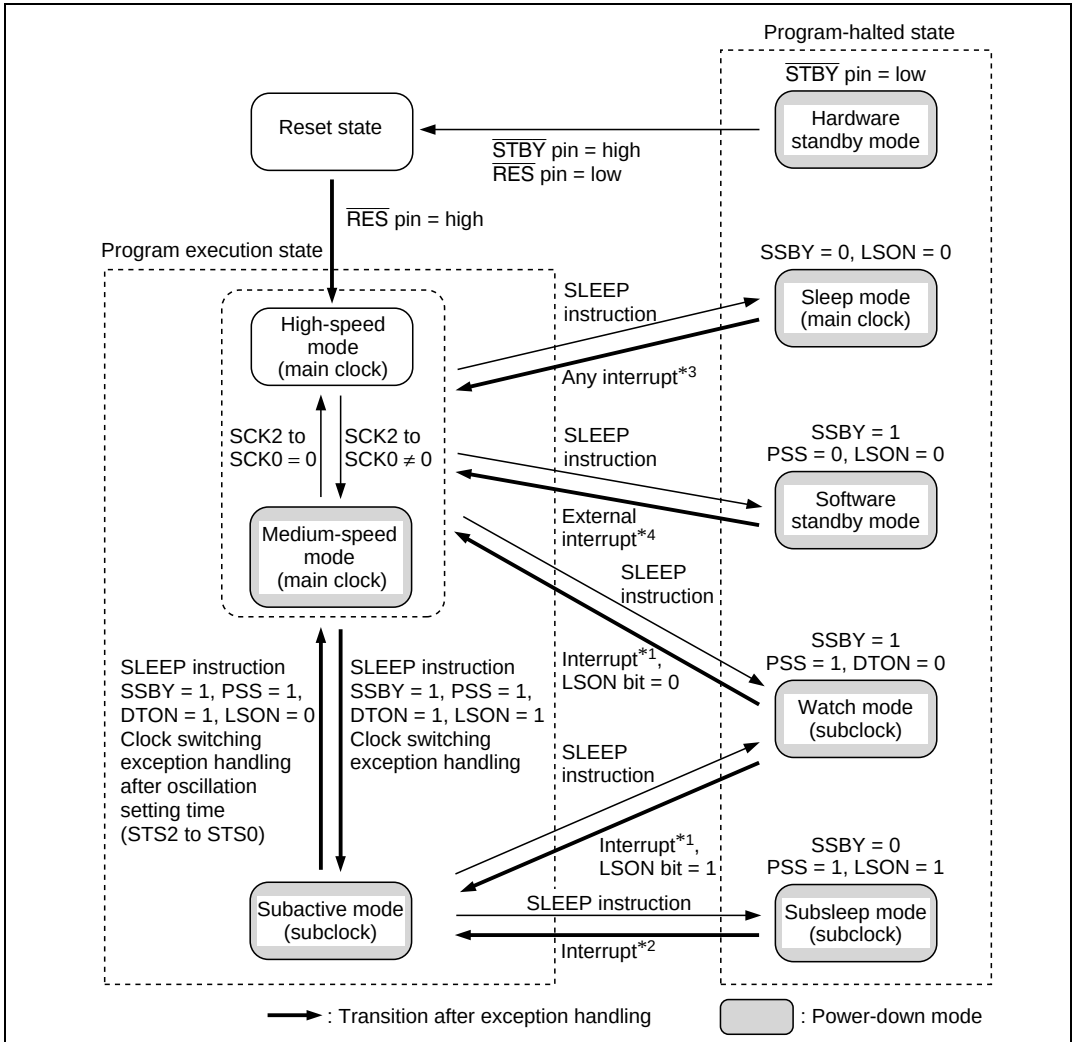
If the MCU malfunctions during flash memory programming/erasing, the FLER bit is set to 1 in FLMCR2 and the error protection state is entered. The FLMCR1, FLMCR2, EBR1, and EBR2 settings are retained, but program mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be re-entered by re-setting the P or E bit. However, PV and EV bit setting is enabled, and a transition can be made to verify mode.

FLER bit setting conditions are as follows:

- When flash memory is read during programming/erasing (including a vector read or instruction fetch)
- Immediately after exception handling (excluding a reset) during programming/erasing
- When a SLEEP instruction (including software standby, sleep, subactive, subsleep and watch mode) is executed during programming/erasing
- When the bus is released during programming/erasing

Error protection is released only by a reset and in hardware standby mode.

Figure 23.14 shows the flash memory state transition diagram.



Notes: When a transition is made between modes by means of an interrupt, transition cannot be made on interrupt source generation alone. Ensure that interrupt handling is performed after accepting the interrupt request.
From any state except hardware standby mode, a transition to the reset state occurs whenever RES goes low.
From any state, a transition to hardware standby mode occurs when STBY goes low.
When a transition is made to watch mode or subactive mode, high-speed mode must be set.

1. NMI, IRQ0 to IRQ2, IRQ6, IRQ7, and WDT1 interrupts
2. NMI, IRQ0 to IRQ7, and WDT0 interrupts, WDT1 interrupt, TMR0 interrupt, TMR1 interrupt
3. All interrupts
4. NMI, IRQ0 to IRQ2, IRQ6, IRQ7

Figure 25.1 Mode Transitions

25.1.1 Register Configuration

The power-down state is controlled by the SBYCR, LPWRCR, TCSR (WDT1), and MSTPCR registers. Table 25.3 summarizes these registers.

Table 25.3 Power-Down State Registers

Name	Abbreviation	R/W	Initial Value	Address*1
Standby control register	SBYCR	R/W	H'00	H'FF84*2
Low-power control register	LPWRCR	R/W	H'00	H'FF85*2
Timer control/status register (WDT1)	TCSR	R/W	H'00	H'FFEA
Module stop control register	MSTPCRH	R/W	H'3F	H'FF86*2
	MSTPCRL	R/W	H'FF	H'FF87*2

Notes: 1. Lower 16 bits of the address.
2. Some power down state registers are assigned to the same address as other registers. In this case, register selection is performed by the FLSHE bit in the serial timer control register (STCR).

25.2 Register Descriptions

25.2.1 Standby Control Register (SBYCR)

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	—	SCK2	SCK1	SCK0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W

SBYCR is an 8-bit readable/writable register that performs power-down mode control.

SBYCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

26.2.4 A/D Conversion Characteristics

Tables 26.12 and 26.13 list the A/D conversion characteristics.

Table 26.12 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, AV_{ref} = 3.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C

	Condition A			Condition B			Condition C			
	20 MHz			16 MHz			10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time*5	—	—	6.7	—	—	8.4	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*3 / 5*4	—	—	10*3 / 5*4	—	—	10*1 / 5*2	kΩ
Nonlinearity error	—	—	±3.0	—	—	±3.0	—	—	±7.0	LSB
Offset error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	—	—	±8.0	LSB

Notes: 1. When 4.0 V ≤ AV_{CC} ≤ 5.5 V
2. When 3.0 V ≤ AV_{CC} < 4.0 V
3. When conversion time ≥ 11. 17 µs (CKS = 1 and φ ≤ 12 MHz, or CKS = 0)
4. When conversion time < 11. 17 µs (CKS = 1 and φ > 12 MHz)
5. In single mode and φ = maximum operating frequency.

26.3 Electrical Characteristics of H8S/2148 F-ZTAT (A-mask version), H8S/2147 F-ZTAT (A-mask version), and Mask ROM Versions of H8S/2148 and H8S/2147

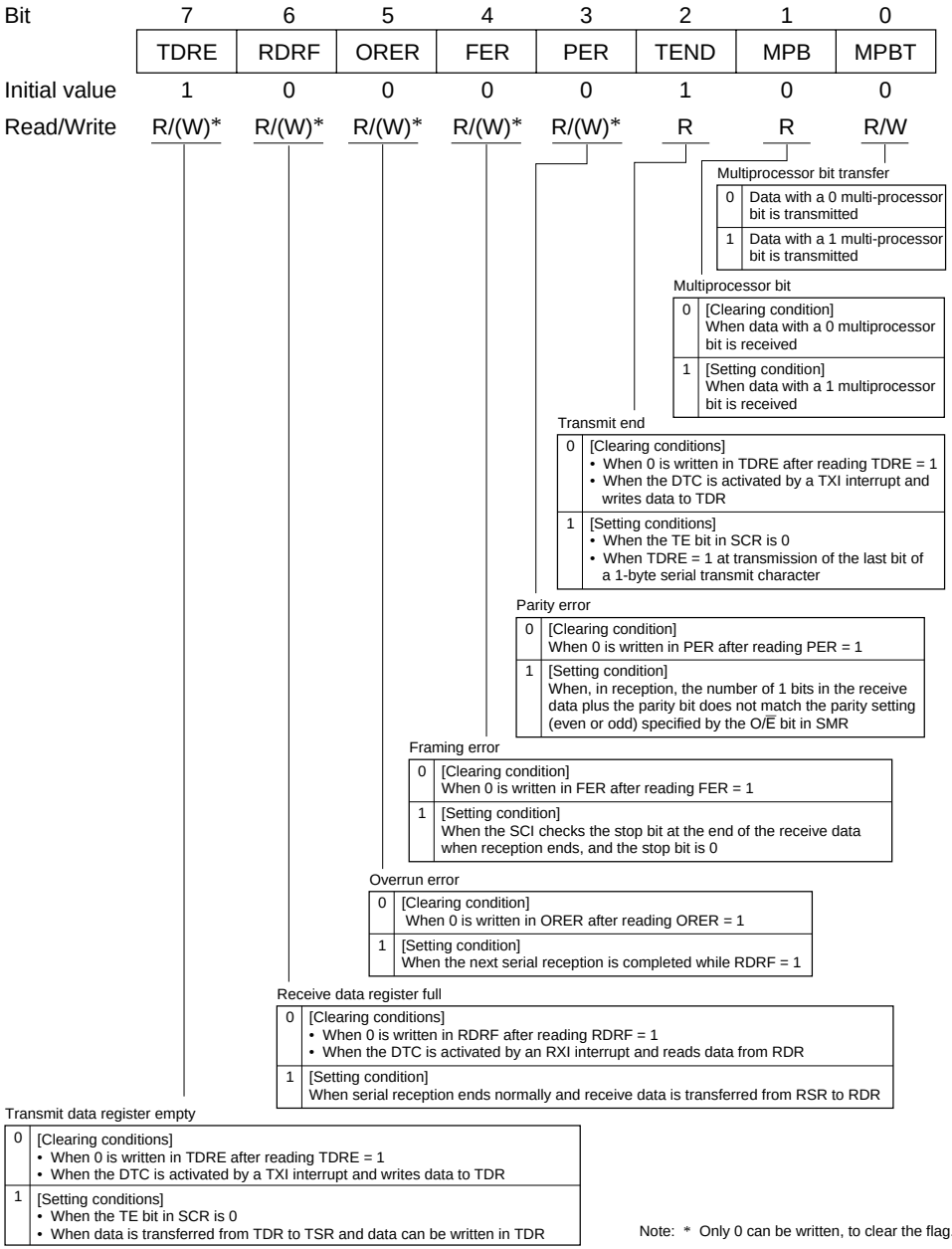
26.3.1 Absolute Maximum Ratings

Table 26.16 lists the absolute maximum ratings.

Table 26.16 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Input/output buffer power supply (power supply for the port A)	$V_{CC}B$	–0.3 to +7.0	V
Power supply voltage*1 (3 V version)	V_{CC}	–0.3 to +4.3	V
Power supply voltage*2 (VCL pin)	V_{CL}	–0.3 to +4.3	V
Input voltage (except ports 6, 7, and A)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port 6)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port A)	V_{in}	–0.3 to $V_{CC}B$ +0.3	V
Input voltage (CIN input selected for port 6)	V_{in}	–0.3 V to lower of voltages V_{CC} +0.3 and AV_{CC} +0.3	V
Input voltage (CIN input selected for port A)	V_{in}	–0.3 V to lower of voltages $V_{CC}B$ +0.3 and AV_{CC} +0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference supply voltage	AV_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog power supply voltage (3 V version)	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C

SSR1—Serial Status Register 1 **H'FF8C** **SCI1**
SSR2—Serial Status Register 2 **H'FFA4** **SCI2**
SSR0—Serial Status Register 0 **H'FFDC** **SCI0**



Note: * Only 0 can be written, to clear the flag.

C.5 Port 5 Block Diagrams

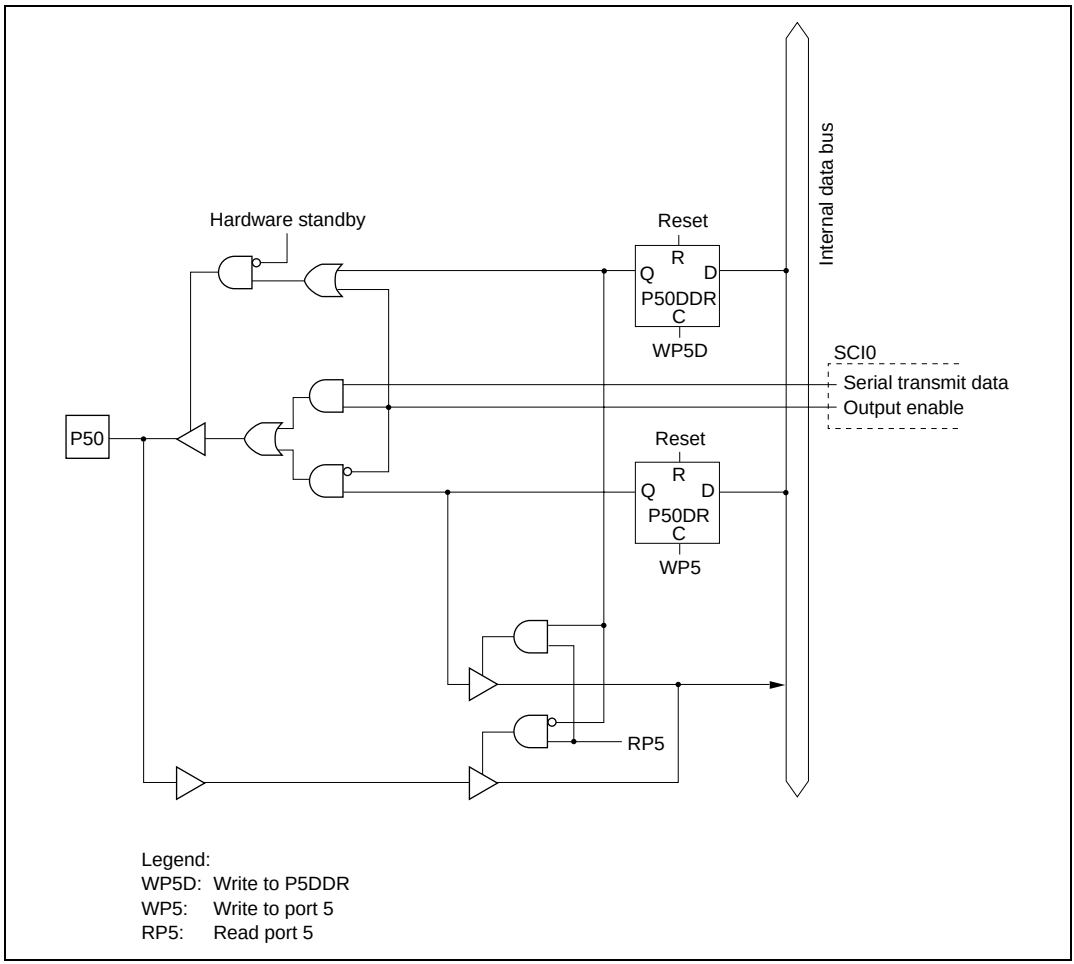


Figure C.13 Port 5 Block Diagram (Pin P50)

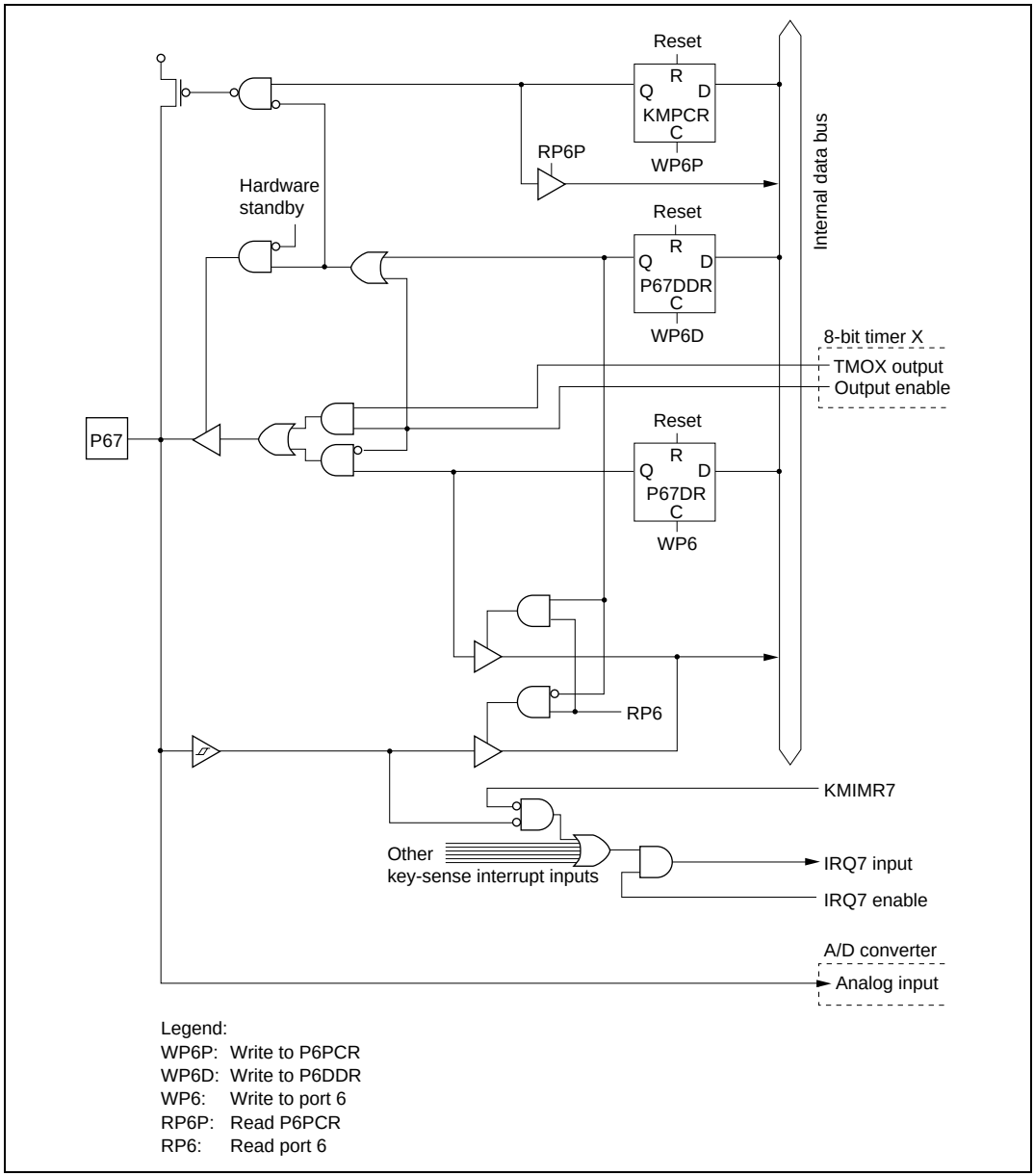


Figure C.20 Port 6 Block Diagram (Pin P67)

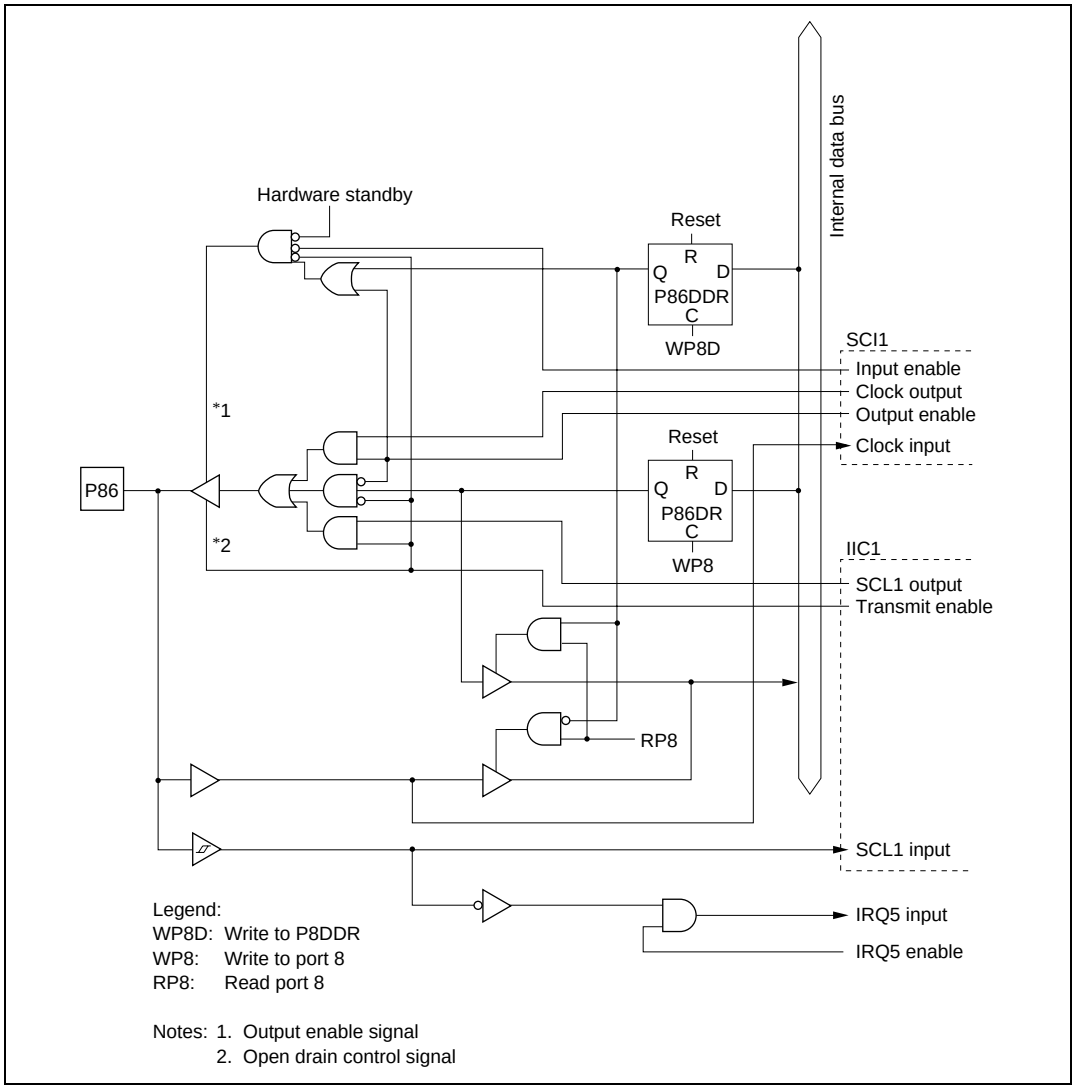


Figure C.28 Port 8 Block Diagram (Pin P86)

C.9 Port 9 Block Diagrams

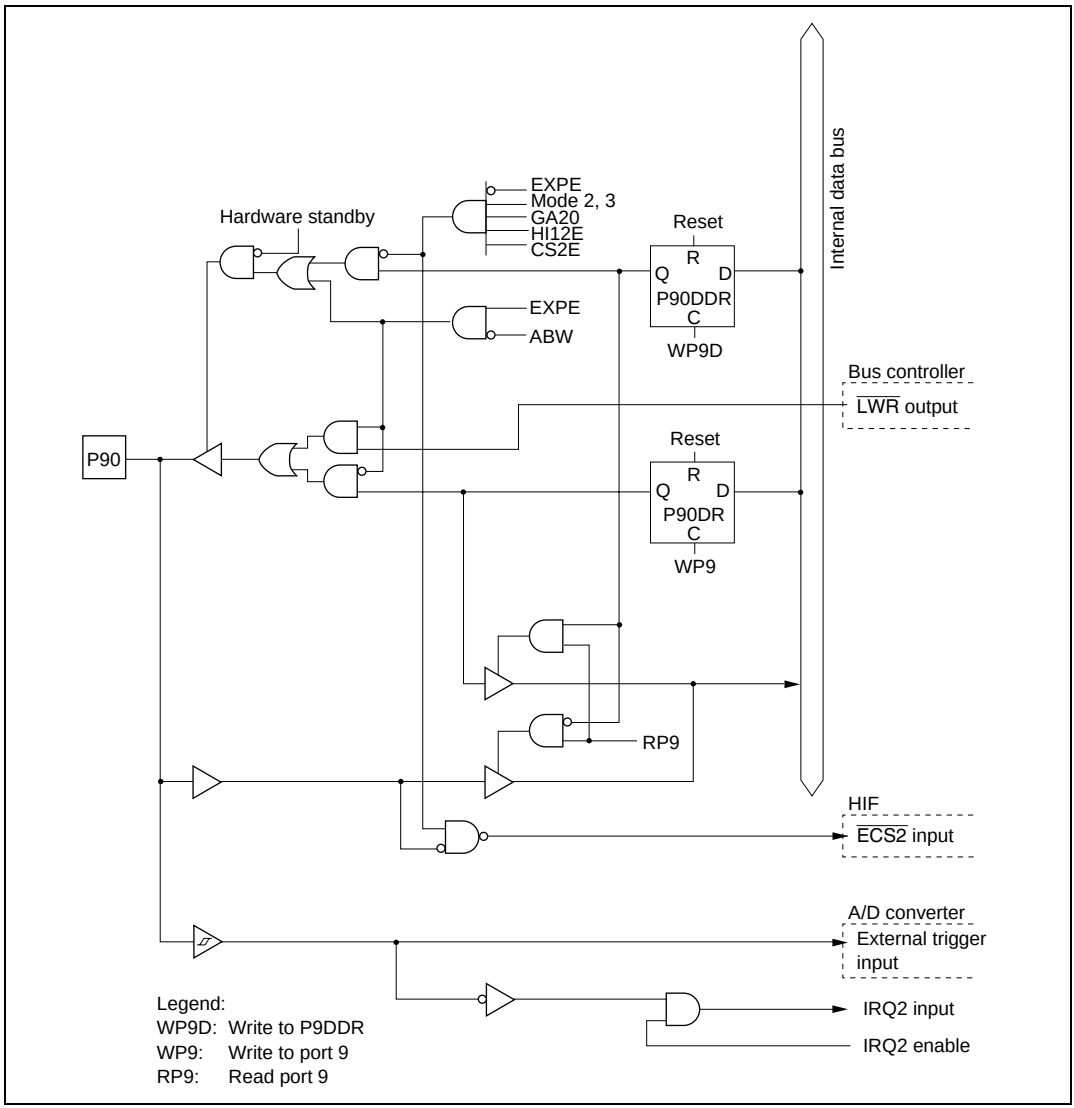


Figure C.29 Port 9 Block Diagram (Pin P90)