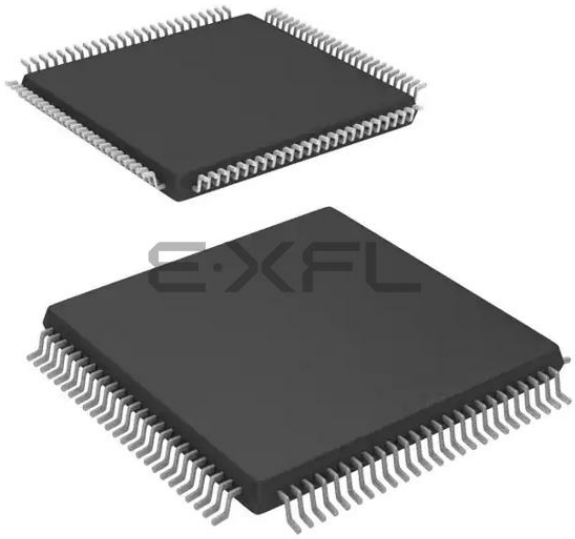

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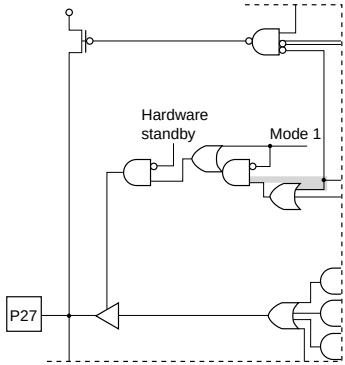
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2148ate20iv

Item	Page	Revision (See Manual for Details)
B.3 Functions	1077	TICRR—H'FFF2 TMRX TICRF—H'FFF3 TMRX Figure amended (Before) Stores TCNT value at fall of external trigger input → (After) Stores TCNT value at fall of external reset input
	1080	STR1—H'FFF6 HIF STR2—H'FFFE HIF Slave R/W description amended Bit 0 (Before) R → (After) R/(W)
C.2 Port 2 Block Diagrams Figure C.4 Port 2 Block Diagram (Pin P27)	1089	Figure C.4 amended 
Appendix F Product Code Lineup Table F.1 H8S/2148 Group and H8S/2144 Group Product Code Lineup	1128	Package code in table F.1 amended HD64F2144ATE20 (Before) FP-100B → (After) TFP-100B HD64F2144AVFA10 (Before) TFP-100B → (After) FP-100B
Appendix G Package Dimensions Figure G.1 Package Dimensions (FP-100B)	1129	Figure G.1 replaced
Figure G.2 Package Dimensions (TFP-100B)	1130	Figure G.2 replaced

Type	Instruction	Size*1	Function
Arithmetic operations	ADD SUB	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register. (Immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
	ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry on byte data in two general registers, or on immediate data and data in a general register.
	INC DEC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
	ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
	DAA DAS	B	Rd decimal adjust → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
	MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
	MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
	DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.

2.10 Usage Note

2.10.1 TAS Instruction

Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction. The TAS instruction is not generated by the Renesas H8S and H8/300 series C/C++ compilers. If the TAS instruction is used as a user-defined intrinsic function, ensure that only register ER0, ER1, ER4, or ER5 is used.

2.10.2 STM/LDM Instruction

ER7 is not used as the register that can be saved (STM)/restored (LDM) when using STM/LDM instruction, because ER7 is the stack pointer. Two, three, or four registers can be saved/restored by one STM/LDM instruction. The following ranges can be specified in the register list.

Two registers: ER0—ER1, ER2—ER3, or ER4—ER5
Three registers: ER0—ER2, or ER4—ER6
Four registers: ER0—ER3

The STM/LDM instruction including ER7 is not generated by the Renesas H8S and H8/300 series C/C++compilers.

5.2.3 IRQ Enable Register (IER)

Bit	7	6	5	4	3	2	1	0
	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IER is an 8-bit readable/writable register that controls enabling and disabling of interrupt requests IRQ7 to IRQ0.

IER is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 0—IRQ7 to IRQ0 Enable (IRQ7E to IRQ0E): These bits select whether IRQ7 to IRQ0 are enabled or disabled.

Bit n

IRQnE	Description	
0	IRQn interrupt disabled	(Initial value)
1	IRQn interrupt enabled	

Note: n = 7 to 0

5.2.4 IRQ Sense Control Registers H and L (ISCRH, ISCRL)

- ISCRH

Bit	15	14	13	12	11	10	9	8
	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

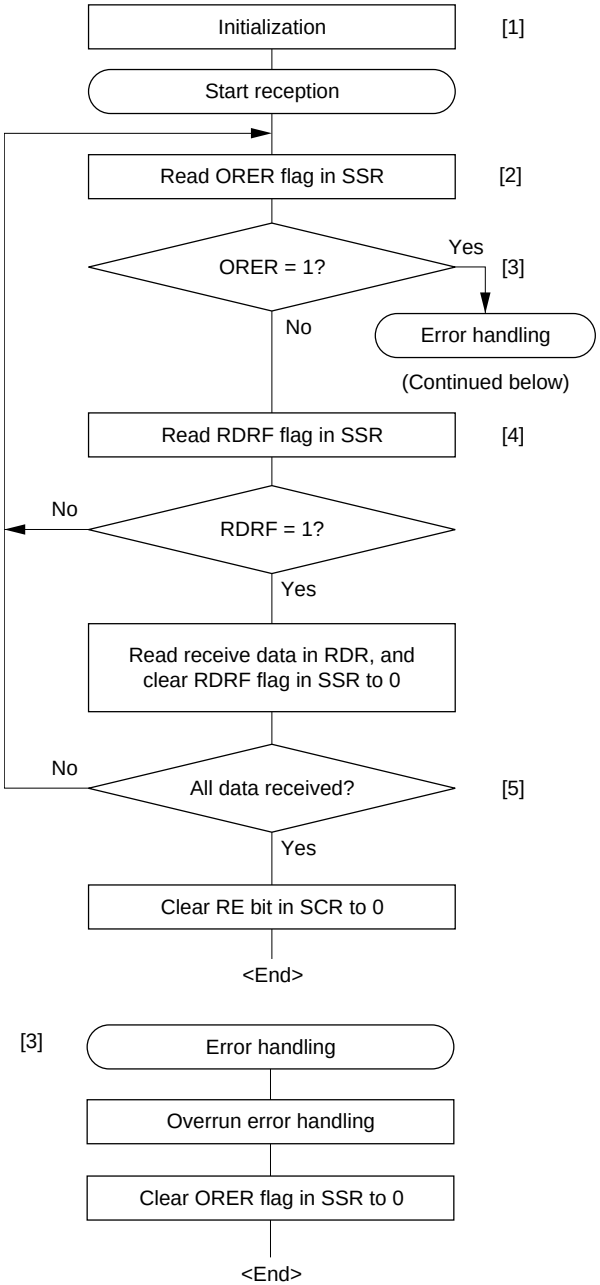
- ISCRL

Bit	7	6	5	4	3	2	1	0
	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port	Description	Pins	Expanded Modes		Single-Chip Mode
			Mode 1	Mode 2, Mode 3 (EXPE = 1)	Mode 2, Mode 3 (EXPE = 0)
Port 4	• 8-bit I/O port	P47/PWX1 P46/PWX0 P45/TMRI1/HIRQ12/CSYNCI P44/TMO1/HIRQ1/HSYNCO P43/TMCI1/HIRQ11/HSYNCI P42/TMRI0/SCK2/SDA1 P41/TMO0/RxD2/IrRxD P40/TMCI0/TxD2/IrTxD	I/O port also functioning as 14-bit PWM timer output (PWX1, PWX0), 8-bit timer 0 and 1 input/output (TMCI0, TMRI0, TMO0, TMCI1, TMRI1, TMO1), timer connection input/output (HSYNCO, CSYNCI, HSYNCI), SCI2 input/output (TxD2, RxD2, SCK2), IrDA interface input/output (IrTxD, IrRxD), and I^2C bus interface 1 (option) input/output (SDA1)		I/O port also functioning as 14-bit PWM timer output (PWX1, PWX0), 8-bit timer 0 and 1 input/output (TMCI0, TMRI0, TMO0, TMCI1, TMRI1, TMO1), timer connection input/output (HSYNCO, CSYNCI, HSYNCI), host interface host CPU interrupt request output (HIRQ12, HIRQ1, HIRQ11), SCI2 input/output (TxD2, RxD2, SCK2), IrDA interface input/output (IrTxD, IrRxD), and I^2C bus interface 1 (option) input/output (SDA1)
Port 5	• 3-bit I/O port	P52/SCK0/SCL0 P51/RxD0 P50/TxD0	I/O port also functioning as SCI0 input/output (TxD0, RxD0, SCK0) and I^2C bus interface 0 (option) input/output (SCL0)		
Port 6	• 8-bit I/O port	P67/$\overline{\text{IRQ7}}$/TMOX/$\overline{\text{KIN7}}$/CIN7 P66/$\overline{\text{IRQ6}}$/FTOB/$\overline{\text{KIN6}}$/CIN6 P65/FTID/$\overline{\text{KIN5}}$/CIN5 P64/FTIC/$\overline{\text{KIN4}}$/CIN4/CLAMPO P63/FTIB/$\overline{\text{KIN3}}$/CIN3/VFBACKI P62/FTIA/TMIY/$\overline{\text{KIN2}}$/CIN2/VSYNCI P61/FTOA/$\overline{\text{KIN1}}$/CIN1/VSYNCO P60/FTCI/TMIX/$\overline{\text{KIN0}}$/CIN0/HFBACKI	I/O port also functioning as external interrupt input ($\overline{\text{IRQ7}}$, $\overline{\text{IRQ6}}$), FRT input/output (FTCI, FTOA, FTIA, FTIB, FTIC, FTID, FTOB), 8-bit timer X and Y input/output (TMOX, TMIX, TMIY), timer connection input/output (CLAMPO, VFBACKI, VSYNCI, VSYNCO, HFBACKI), key-sense interrupt input ($\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$), and expansion A/D converter input (CIN7 to CIN0)		

	TCR			STCR		
	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0	
Channel	CKS2	CKS1	CKS0	ICKS1	ICKS0	Description
X	0	0	0	—	—	Clock input disabled (Initial value)
	0	0	1	—	—	Counted on ϕ internal clock source
	0	1	0	—	—	ϕ/2 internal clock source, counted on the falling edge
	0	1	1	—	—	ϕ/4 internal clock source, counted on the falling edge
	1	0	0	—	—	Clock input disabled
Y	0	0	0	—	—	Clock input disabled (Initial value)
	0	0	1	—	—	ϕ/4 internal clock source, counted on the falling edge
	0	1	0	—	—	ϕ/256 internal clock source, counted on the falling edge
	0	1	1	—	—	ϕ/2048 internal clock source, counted on the falling edge
	1	0	0	—	—	Clock input disabled
Common	1	0	1	—	—	External clock source, counted at rising edge
	1	1	0	—	—	External clock source, counted at falling edge
	1	1	1	—	—	External clock source, counted at both rising and falling edges

Note: * If the count input of channel 0 is the TCNT1 overflow signal and that of channel 1 is the TCNT0 compare-match signal, no incrementing clock will be generated. Do not use this setting.



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error handling:
If a receive error occurs, read the ORER flag in SSR , and after performing the appropriate error handling, clear the ORER flag to 0. Transfer cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0. The RDRF flag is cleared automatically when the DTC is activated by a receive-data-full interrupt (RXI) request and the RDR value is read.

Figure 15.18 Sample Serial Reception Flowchart

Table 18.7 Fast A20 Gate Output Signal

HA0	Data/Command	Internal CPU Interrupt Flag	GA20 (P81)	Remarks
1	H'D1 command	0	Q	Turn-on sequence
0	1 data*1	0	1	
1	H'FF command	0	Q (1)	
1	H'D1 command	0	Q	Turn-off sequence
0	0 data*2	0	0	
1	H'FF command	0	Q (0)	
1	H'D1 command	0	Q	Turn-on sequence
0	1 data*1	0	1	(abbreviated form)
1/0	Command other than H'FF and H'D1	1	Q (1)	
1	H'D1 command	0	Q	Turn-off sequence
0	0 data*2	0	0	(abbreviated form)
1/0	Command other than H'FF and H'D1	1	Q (0)	
1	H'D1 command	0	Q	Cancelled sequence
1	Command other than H'D1	1	Q	
1	H'D1 command	0	Q	Retriggered sequence
1	H'D1 command	0	Q	
1	H'D1 command	0	Q	Consecutively executed
0	Any data	0	1/0	sequences
1	H'D1 command	0	Q(1/0)	

Notes: 1. Arbitrary data with bit 1 set to 1.
2. Arbitrary data with bit 1 cleared to 0.

18.3.4 Host Interface Pin Shutdown Function

Host interface output can be placed in the high-impedance state according to the state of the HIFSD pin. Setting the SDE bit to 1 in the SYSCR2 register enables the HIFSD pin is slave mode. The HIF constantly monitors the HIFSD pin, and when this pin goes low, places the host interface output pins (HIRQ1, HIRQ11, HIRQ12, HIRQ3, HIRQ4, and GA20) in the high-impedance state. At the same time, the host interface input pins ($\overline{CS1}$, $\overline{CS2}$ or $\overline{ECS2}$, $\overline{CS3}$, $\overline{CS4}$, $\overline{IOW}$, $\overline{IOR}$, and HA0) are disabled (fixed at the high input state internally) regardless of the pin states, and the signals of the multiplexed functions of these pins (input block) are similarly fixed internally. As a result, the host interface I/O pins (HDB7 to HDB0) also go to the high-impedance state.

This state is maintained while the HIFSD pin is low, and when the HIFSD pin returns to the high-level state, the pins are restored to their normal operation as host interface pins.

22.4.4 Pin Configuration

The flash memory is controlled by means of the pins shown in table 22.3.

Table 22.3 Flash Memory Pins

Pin Name	Abbreviation	I/O	Function
Reset	$\overline{\text{RES}}$	Input	Reset
Mode 1	MD1	Input	Sets MCU operating mode
Mode 0	MD0	Input	Sets MCU operating mode
Port 92	P92	Input	Sets MCU operating mode when MD1 = MD0 = 0
Port 91	P91	Input	Sets MCU operating mode when MD1 = MD0 = 0
Port 90	P90	Input	Sets MCU operating mode when MD1 = MD0 = 0
Transmit data	TxD1	Output	Serial transmit data output
Receive data	RxD1	Input	Serial receive data input

22.4.5 Register Configuration

The registers used to control the on-chip flash memory when enabled are shown in table 22.4. In order for these registers to be accessed, the FLSHE bit must be set to 1 in STCR.

Table 22.4 Flash Memory Registers

Register Name	Abbreviation	R/W	Initial Value	Address*1
Flash memory control register 1	FLMCR1*5	R/W*3	H'80	H'FF80*2
Flash memory control register 2	FLMCR2*5	R/W*3	H'00*4	H'FF81*2
Erase block register 1	EBR1*5	R/W*3	H'00*4	H'FF82*2
Erase block register 2	EBR2*5	R/W*3	H'00*4	H'FF83*2
Serial/timer control register	STCR	R/W	H'00	H'FFC3

Notes: 1. Lower 16 bits of the address.
2. Flash memory registers share addresses with other registers. Register selection is performed by the FLSHE bit in the serial/timer control register (STCR).
3. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid.
4. The SWE bit in FLMCR1 is not set, these registers are initialized to H'00.
5. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers. Only byte accesses are valid for these registers, the access requiring 2 states. These registers are used only in the flash memory version. In the mask ROM version, a read at any of these addresses will return an undefined value, and writes are invalid.

On-Chip RAM Area Divisions in Boot Mode

In boot mode, the 128-byte area from H'(FF)FF00 to H'(FF)FF7F is reserved for use by the boot program, as shown in figure 22.10. The area to which the programming control program is transferred is H'(FF)E080 to H'(FF)EFFF (3968 bytes) in the 128-kbyte versions, or H'(FF)E880 to H'(FF)EFFF (1920 bytes) in the 64-kbyte versions. The boot program area can be used when the programming control program transferred into RAM enters the execution state. A stack area should be set up as required.

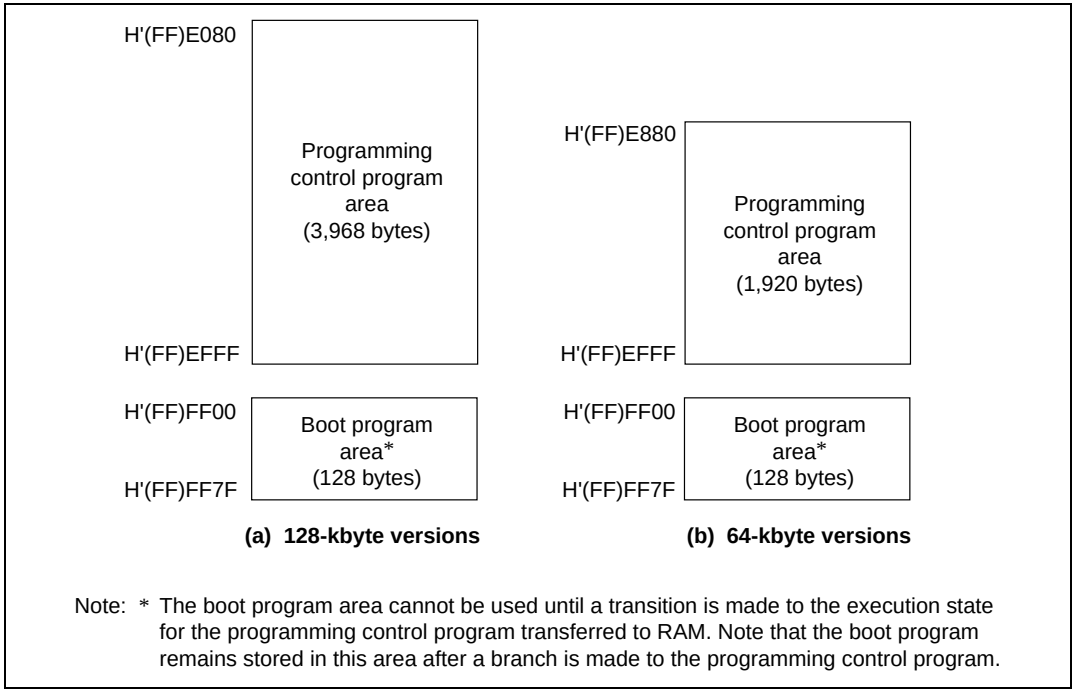


Figure 22.10 RAM Areas in Boot Mode

Notes on Use of User Mode

- When the chip comes out of reset in boot mode, it measures the low period of the input at the SCI's RxD1 pin. The reset should end with RxD1 high. After the reset ends, it takes about 100 states for the chip to get ready to measure the low period of the RxD1 input.
- In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.

Table 23.11 Settings for Each Operating Mode in Programmer Mode

	Pin Names				
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**FO0 to FO7**	**FA0 to FA17**
Read	L	L	H	Data output	Ain
Output disable	L	H	H	Hi-Z	X
Command write	L	H	L	Data input	Ain*2
Chip disable*1	H	X	X	Hi-Z	X

Notes: 1. Chip disable is not a standby state; internally, it is an operation state.
2. Ain indicates that there is also address input in auto-program mode.

Table 23.12 Programmer Mode Commands

	Number	1st Cycle			2nd Cycle		
Command Name	**of Cycles**	**Mode**	**Address**	**Data**	**Mode**	**Address**	**Data**
Memory read mode	1 + n	Write	X	H'00	Read	RA	Dout
Auto-program mode	129	Write	X	H'40	Write	WA	Din
Auto-erase mode	2	Write	X	H'20	Write	X	H'20
Status read mode	2	Write	X	H'71	Write	X	H'71

Notes: 1. In auto-program mode. 129 cycles are required for command writing by a simultaneous 128-byte write.
2. In memory read mode, the number of cycles depends on the number of address write cycles (n).

23.10.4 Memory Read Mode

- After the end of an auto-program, auto-erase, or status read operation, the command wait state is entered. To read memory contents, a transition must be made to memory read mode by means of a command write before the read is executed.
- Command writes can be performed in memory read mode, just as in the command wait state.
- Once memory read mode has been entered, consecutive reads can be performed.
- After power-on, memory read mode is entered.

Notes: 1. **Do not leave the AVCC, AV_{ref}, and AVSS pins open even if the A/D converter and D/A converter are not used.**

Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 5.5 V to AVCC and AV_{ref} pins by connection to the power supply (V_{CC}), or some other method. Ensure that $AV_{ref} \leq AV_{CC}$.

2. P67 to P60 include supporting module inputs multiplexed on those pins.
3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.
4. In the H8S/2148 Group, P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs.

   An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

   In the H8S/2148 Group, P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS.
5. When IICS = 0, ICE = 0, and KBIOE = 0. Low-level output when the bus drive function is selected is determined separately.
6. The upper limit of the port 6 applied voltage is V_{CC} +0.3 V when CIN input is not selected, and the lower of V_{CC} +0.3 V and AV_{CC} +0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
7. The upper limit of the port A applied voltage is $V_{CC}B$ +0.3 V when CIN input is not selected, and the lower of $V_{CC}B$ +0.3 V and AV_{CC} +0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
8. The port A characteristics depend on $V_{CC}B$, and the other pins characteristics depend on V_{CC}.
9. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V, $V_{CC}B$ –0.5 V, and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.
10. The values are for $V_{RAM} \leq V_{CC} < 4.0$ V, V_{IH} min = $V_{CC} \times 0.9$, $V_{CC}B \times 0.9$, and V_{IL} max = 0.3 V.
11. For flash memory program/erase operations, the applicable ranges are V_{CC} = 4.5 V to 5.5 V and T_a = 0 to +75°C (regular specifications) or T_a = 0 to +85°C (wide-range specifications).

(1) Clock Timing

Table 26.6 shows the clock timing. The clock timing specified here covers clock (φ) output and clock pulse generator (crystal) and external clock input (EXTAL pin) oscillation settling times. For details of external clock input (EXTAL pin and EXCL pin) timing, see section 24, Clock Pulse Generator.

Table 26.6 Clock Timing

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 3.0 V to 5.5 V, $V_{CC}B$ = 3.0 V to 5.5 V, V_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

		Condition A		Condition B		Condition C			
		20 MHz		16 MHz		10 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Clock cycle time	t_{cyc}	50	500	62.5	500	100	500	ns	Figure 26.5
Clock high pulse width	t_{CH}	17	—	20	—	30	—	ns	Figure 26.5
Clock low pulse width	t_{CL}	17	—	20	—	30	—	ns	
Clock rise time	t_{Cr}	—	8	—	10	—	20	ns	
Clock fall time	t_{Cf}	—	8	—	10	—	20	ns	
Oscillation settling time at reset (crystal)	t_{OSC1}	10	—	10	—	20	—	ms	Figure 26.6 Figure 26.7
Oscillation settling time in software standby (crystal)	t_{OSC2}	8	—	8	—	8	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	500	—	µs	

26.5.4 A/D Conversion Characteristics

Tables 26.52 and 26.53 list the A/D conversion characteristics.

Table 26.52 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C (mask ROM version): V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, AV_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

Condition C (F-ZTAT version): V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

	Condition A			Condition B			Condition C			
	20 MHz			16 MHz			10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time*5	—	—	6.7	—	—	8.4	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*3 / 5*4	—	—	10*3 / 5*4	—	—	10*1 / 5*2	kΩ
Nonlinearity error	—	—	±3.0	—	—	±3.0	—	—	±7.0	LSB
Offset error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	—	—	±8.0	LSB

Notes: 1. When 4.0 V ≤ AV_{CC} ≤ 5.5 V
2. When 2.7 V ≤ AV_{CC} < 4.0 V (mask ROM version) or when 3.0 V ≤ AV_{CC} < 4.0 V (F-ZTAT version)
3. When conversion time ≥ 11. 17 µs (CKS = 1 and ϕ ≤ 12 MHz, or CKS = 0)
4. When conversion time < 11. 17 µs (CKS = 1 and ϕ > 12 MHz)
5. In single mode and ϕ = maximum operating frequency.

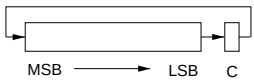
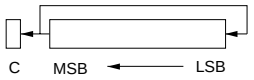
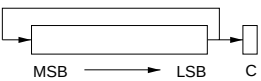
26.6.2 DC Characteristics

Table 26.57 lists the DC characteristics. Permitted output current values and bus drive characteristics are shown in tables 26.58 and 26.59, respectively.

Table 26.57 DC Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC}*1 = 5.0 V ±10%, AV_{ref}*1 = 4.5 V to AV_{CC},
V_{SS} = AV_{SS}*1 = 0 V, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60*2*5, $\overline{KIN15}$ to $\overline{KIN8}$*5, $\overline{IRQ2}$ to $\overline{IRQ0}$*3, $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	V_{CC} –0.7	—	V_{CC} +0.3	V	
	EXTAL, PA7 to PA0*5			$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 7			2.0	—	AV_{CC} +0.3	V	
	Input pins except (1) and (2) above			2.0	—	V_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0	(3)	V_{IL}	–0.3	—	0.5	V	
	PA7 to PA0			–0.3	—	1.0	V	
	NMI, EXTAL, input pins except (1) and (3) above			–0.3	—	0.8	V	
Output high voltage	All output pins*4		V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
				3.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)*4		V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3			—	—	1.0	V	I_{OL} = 10 mA
	$\overline{RESO}$			—	—	0.4	V	I_{OL} = 2.6 mA

Mnemonic		Size	Addressing Mode and Instruction Length (Bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d,ERn)	@-ERn/@ERn+	@aa	@(d,PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
ROTXR	ROTXR.B Rd	B		2									—	—	↕	↕	0	↕	1	
	ROTXR.B #2,Rd	B		2									—	—	↕	↕	0	↕	1	
	ROTXR.W Rd	W		2									—	—	↕	↕	0	↕	1	
	ROTXR.W #2,Rd	W		2									—	—	↕	↕	0	↕	1	
	ROTXR.L ERd	L		2									—	—	↕	↕	0	↕	1	
	ROTXR.L #2,ERd	L		2									—	—	↕	↕	0	↕	1	
ROTL	ROTL.B Rd	B		2									—	—	↕	↕	0	↕	1	
	ROTL.B #2,Rd	B		2									—	—	↕	↕	0	↕	1	
	ROTL.W Rd	W		2									—	—	↕	↕	0	↕	1	
	ROTL.W #2,Rd	W		2									—	—	↕	↕	0	↕	1	
	ROTL.L ERd	L		2									—	—	↕	↕	0	↕	1	
	ROTL.L #2,ERd	L		2									—	—	↕	↕	0	↕	1	
ROTR	ROTR.B Rd	B		2									—	—	↕	↕	0	↕	1	
	ROTR.B #2,Rd	B		2									—	—	↕	↕	0	↕	1	
	ROTR.W Rd	W		2									—	—	↕	↕	0	↕	1	
	ROTR.W #2,Rd	W		2									—	—	↕	↕	0	↕	1	
	ROTR.L ERd	L		2									—	—	↕	↕	0	↕	1	
	ROTR.L #2,ERd	L		2									—	—	↕	↕	0	↕	1	

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FFA2	SCR2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	SCI2	8
H'FFA3	TDR2										
H'FFA4	SSR2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT		
H'FFA5	RDR2										
H'FFA6	SCMR2	—	—	—	—	SDIR	SINV	—	SMIF		
	DADRBH	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	PWMX	8
	DACNTH										
H'FFA7	DADRBL	DA5	DA4	DA3	DA2	DA1	DA0	CFS	REGS		
	DACNTL							—	REGS		
H'FFA8	TCSR0	OVF	WT/$\overline{IT}$	TME	RSTS	RST/$\overline{NMI}$	CKS2	CKS1	CKS0	WDT0	16
	TCNT0 (write)										
H'FFA9	TCNT0 (read)										
H'FFAA	PAODR	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR	Ports	8
H'FFAB	PAPIN (read)	PA7PIN	PA6PIN	PA5PIN	PA4PIN	PA3PIN	PA2PIN	PA1PIN	PA0PIN		
	PADDR (write)	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR		
H'FFAC	P1PCR	P17PCR	P16PCR	P15PCR	P14PCR	P13PCR	P12PCR	P11PCR	P10PCR		
H'FFAD	P2PCR	P27PCR	P26PCR	P25PCR	P24PCR	P23PCR	P22PCR	P21PCR	P20PCR		
H'FFAE	P3PCR	P37PCR	P36PCR	P35PCR	P34PCR	P33PCR	P32PCR	P31PCR	P30PCR		
H'FFB0	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR		
H'FFB1	P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR		
H'FFB2	P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR		
H'FFB3	P2DR	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR		
H'FFB4	P3DDR	P37DDR	P36DDR	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FFB5	P4DDR	P47DDR	P46DDR	P45DDR	P44DDR	P43DDR	P42DDR	P41DDR	P40DDR		
H'FFB6	P3DR	P37DR	P36DR	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR		
H'FFB7	P4DR	P47DR	P46DR	P45DR	P44DR	P43DR	P42DR	P41DR	P40DR		
H'FFB8	P5DDR	—	—	—	—	—	P52DDR	P51DDR	P50DDR		
H'FFB9	P6DDR	P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR		
H'FFBA	P5DR	—	—	—	—	—	P52DR	P51DR	P50DR		
H'FFBB	P6DR	P67DR	P66DR	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR		
H'FFBC	PBODR	PB7ODR	PB6ODR	PB5ODR	PB4ODR	PB3ODR	PB2ODR	PB1ODR	PB0ODR		
H'FFBD	PBPIN (read)	PB7PIN	PB6PIN	PB5PIN	PB4PIN	PB3PIN	PB2PIN	PB1PIN	PB0PIN		
	P8DDR (write)	—	P86DDR	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR		

STR3—Status Register 3 **H'FE86** **HIF**
STR4—Status Register 4 **H'FE8E** **HIF**

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	C/$\overline{D}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Slave R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/(W)
Host R/W	R	R	R	R	R	R	R	R

User-defined bits

Output buffer full

0	[Clearing condition] When the host processor reads ODR or the slave writes 0 in the OBF bit
1	[Setting condition] When the slave processor writes to ODR

Input buffer full

0	[Clearing condition] When the slave processor reads IDR
1	[Setting condition] When the host processor writes to IDR

Command/data

0	Contents of input data register (IDR) are data
1	Contents of input data register (IDR) are a command

STCR—Serial Timer Control Register **H'FFC3** **System**

Bit	7	6	5	4	3	2	1	0
	IICS	IICX1	IICX0	IICE	FLSHE	—	ICKS1	ICKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Internal Clock Source Select*1

Reserved bit

Flash memory control register enable

0	Flash memory control register not selected
1	Flash memory control register selected

I2C master enable

0	CPU access to SCI0, SCI1, and SCI2 control registers is enabled
1	CPU access to I2C bus interface data, PWMX and control registers is enabled

I2C transfer select 1 and 0*2

I2C extra buffer select

0	PA7 to PA4 are normal I/O pins
1	PA7 to PA4 are I/O pins with bus driving capability

Notes: 1. Used for 8-bit timer input clock selection. For details, see section 12.2.4, Timer Control Register (TCR).
2. Used for I2C bus interface transfer clock selection. For details, see section 16.2.4, I2C Bus Mode Register (ICMR).

TCORA0—Time Constant Register A0	**H'FFCC**	**TMR0**
TCORA1—Time Constant Register A1	**H'FFCD**	**TMR1**
TCORB0—Time Constant Register B0	**H'FFCE**	**TMR0**
TCORB1—Time Constant Register B1	**H'FFCF**	**TMR1**
TCORAY—Time Constant Register AY	**H'FFF2**	**TMRY**
TCORBY—Time Constant Register BY	**H'FFF3**	**TMRY**
TCORC—Time Constant Register C	**H'FFF5**	**TMRX**
TCORAX—Time Constant Register AX	**H'FFF6**	**TMRX**
TCORBX—Time Constant Register BX	**H'FFF7**	**TMRX**

TCORA0
TCORB0

TCORA1
TCORB1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Compare match flag (CMF) is set when TCOR and TCNT values match

TCORAX, TCORAY
TCORBX, TCORBY

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Compare match flag (CMF) is set when TCOR and TCNT values match

TCORC

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Compare match C signal is generated when sum of TCORC and TICR contents match TCNT value