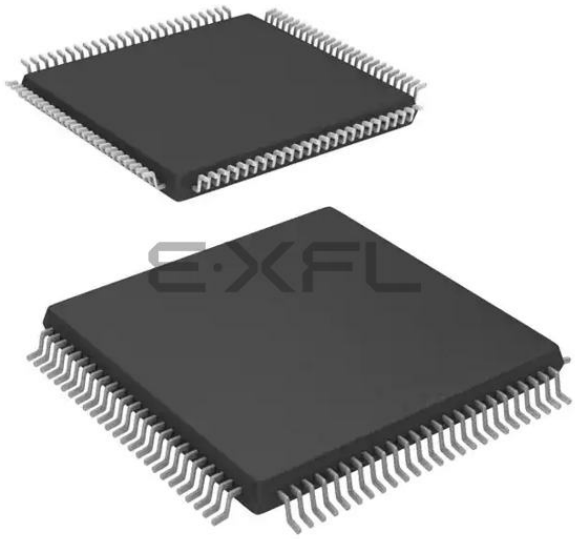

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2148ate20v

Item	Specifications				
Product lineup (preliminary)	Product Code[*2]				
	Group	Mask ROM Versions	F-ZTAT Versions	ROM/RAM (Bytes)	Packages
	H8S/2148	HD6432148S	HD64F2148 HD64F2148V[*2]	128 k/4 k	FP-100B, TFP-100B
		HD6432148SW[*1]	HD64F2148A HD64F2148AV[*2]		
		HD6432147S	HD64F2147A	64 k/2 k	
		HD6432147SW[*1]	HD64F2147AV[*2]		
	H8S/2147N	—	HD64F2147N HD64F2147NV[*2]	64 k/2 k	
	H8S/2144	HD6432144S	HD64F2144 HD64F2144V[*2]	128 k/4 k	
			HD64F2144A HD64F2144AV[*2]		
		HD6432143S	—	96 k/4 k	
		HD6432142	HD64F2142R HD64F2142RV[*2]	64 k/2 k	
	Notes: 1. W indicates the I^2C bus option. 2. V indicates the 3-V version. Please refer to appendix F, Product Code Lineup.				

1.2 Internal Block Diagram

An internal block diagram of the H8S/2148 Group is shown in figure 1.1 (a), an internal block diagram of the H8S/2147N is shown in figure 1.1 (b), and an internal block diagram of the H8S/2144 Group in figure 1.1 (c).

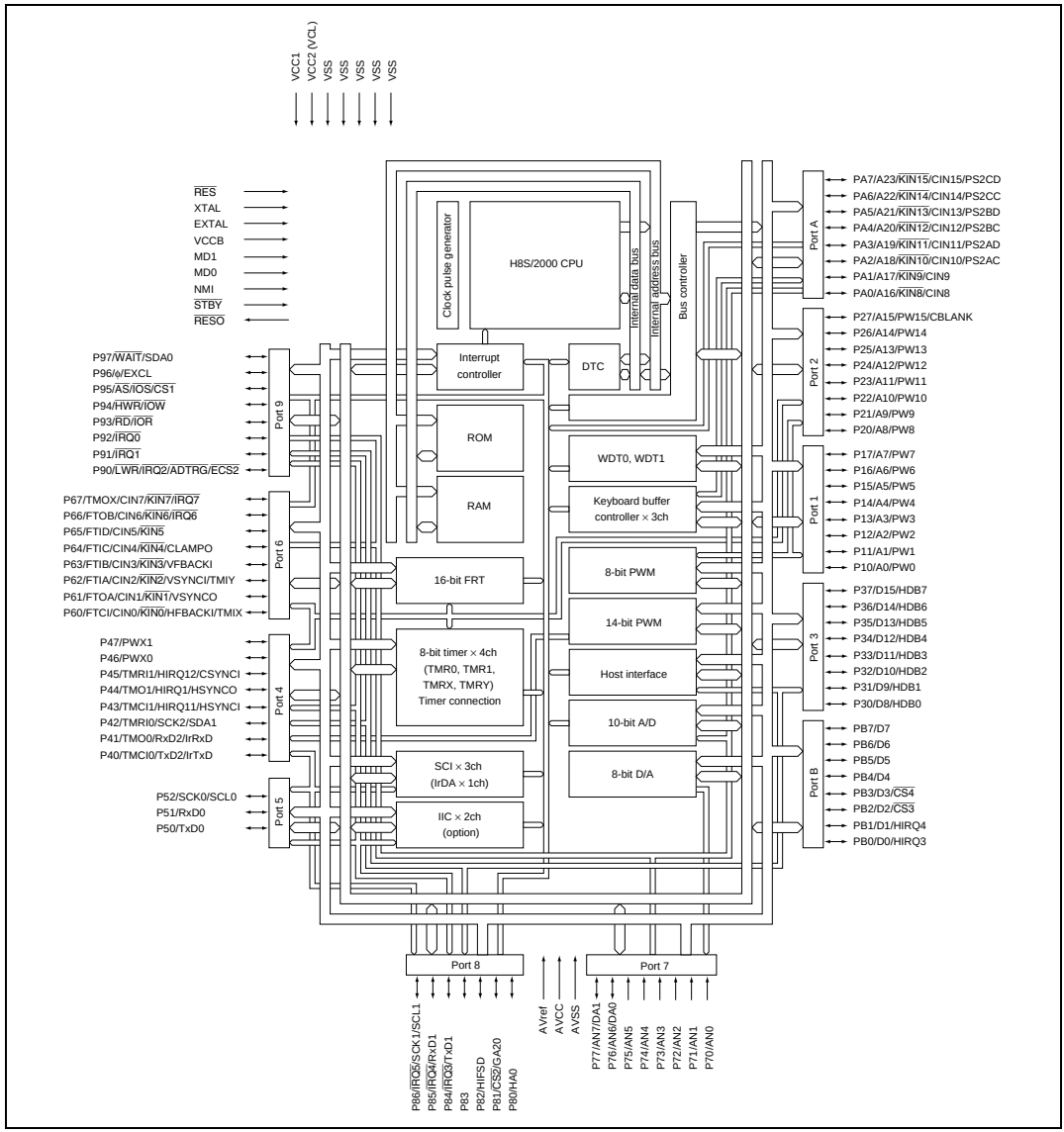


Figure 1.1 (a) Internal Block Diagram of H8S/2148 Group

Pin No.	Pin Name			
	Expanded Modes		Single-Chip Modes	
FP-100B TFP-100B	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)	Flash Memory Writer Mode
25	$\overline{\text{LWR}}$/P90/$\overline{\text{IRQ2}}$/ $\overline{\text{ADTRG}}$	$\overline{\text{LWR}}$/P90/$\overline{\text{IRQ2}}$/ $\overline{\text{ADTRG}}$	P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$/ $\overline{\text{ECS2}}$	VCC
26	P60/FTCI/CIN0/ $\overline{\text{KIN0}}$	P60/FTCI/CIN0/ $\overline{\text{KIN0}}$	P60/FTCI/CIN0/ $\overline{\text{KIN0}}$	NC
27	P61/FTOA/CIN1/ $\overline{\text{KIN1}}$	P61/FTOA/CIN1/ $\overline{\text{KIN1}}$	P61/FTOA/CIN1/ $\overline{\text{KIN1}}$	NC
28	P62/FTIA/CIN2/ $\overline{\text{KIN2}}$/TMIY	P62/FTIA/CIN2/ $\overline{\text{KIN2}}$/TMIY	P62/FTIA/CIN2/ $\overline{\text{KIN2}}$/TMIY	NC
29	P63/FTIB/CIN3/ $\overline{\text{KIN3}}$	P63/FTIB/CIN3/ $\overline{\text{KIN3}}$	P63/FTIB/CIN3/ $\overline{\text{KIN3}}$	NC
30	PA3/CIN11/ $\overline{\text{KIN11}}$/PS2AD	A19/PA3/CIN11/ $\overline{\text{KIN11}}$/PS2AD	PA3/CIN11/ $\overline{\text{KIN11}}$/PS2AD	NC
31	PA2/CIN10/ $\overline{\text{KIN10}}$/PS2AC	A18/PA2/CIN10/ $\overline{\text{KIN10}}$/PS2AC	PA2/CIN10/ $\overline{\text{KIN10}}$/PS2AC	NC
32	P64/FTIC/CIN4/ $\overline{\text{KIN4}}$	P64/FTIC/CIN4/ $\overline{\text{KIN4}}$	P64/FTIC/CIN4/ $\overline{\text{KIN4}}$	NC
33	P65/FTID/CIN5/ $\overline{\text{KIN5}}$	P65/FTID/CIN5/ $\overline{\text{KIN5}}$	P65/FTID/CIN5/ $\overline{\text{KIN5}}$	NC
34	P66/FTOB/CIN6/ $\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$	P66/FTOB/CIN6/ $\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$	P66/FTOB/CIN6/ $\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$	NC
35	P67/CIN7/$\overline{\text{KIN7}}$/ $\overline{\text{IRQ7}}$	P67/CIN7/$\overline{\text{KIN7}}$/ $\overline{\text{IRQ7}}$	P67/CIN7/$\overline{\text{KIN7}}$/ $\overline{\text{IRQ7}}$	VSS
36	AVref	AVref	AVref	VCC
37	AVCC	AVCC	AVCC	VCC
38	P70/AN0	P70/AN0	P70/AN0	NC
39	P71/AN1	P71/AN1	P71/AN1	NC
40	P72/AN2	P72/AN2	P72/AN2	NC
41	P73/AN3	P73/AN3	P73/AN3	NC
42	P74/AN4	P74/AN4	P74/AN4	NC
43	P75/AN5	P75/AN5	P75/AN5	NC
44	P76/AN6/DA0	P76/AN6/DA0	P76/AN6/DA0	NC
45	P77/AN7/DA1	P77/AN7/DA1	P77/AN7/DA1	NC

2.6.2 Instructions and Addressing Modes

Table 2.2 indicates the combinations of instructions and addressing modes that the H8S/2000 CPU can use.

Table 2.2 Combinations of Instructions and Addressing Modes

Function	Instruction	Addressing Modes													
		#xx	Rn	@ERn	@(d:16,ERn)	@(d:32, ERn)	@–ERn/@ERn+	@aa:8	@aa:16	@aa:24	@aa:32	@(d:8, PC)	@(d:16, PC)	@@aa:8	|
Data transfer	MOV	BWL	BWL	BWL	BWL	BWL	BWL	B	BWL	—	BWL	—	—	—	—
	POP, PUSH	—	—	—	—	—	—	—	—	—	—	—	—	—	WL
	LDM*3, STM*3	—	—	—	—	—	—	—	—	—	—	—	—	—	L
	MOVFPE*1, MOVTPE*1	—	—	—	—	—	—	—	B	—	—	—	—	—	—
Arithmetic operations	ADD, CMP	BWL	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	SUB	WL	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	ADDX, SUBX	B	B	—	—	—	—	—	—	—	—	—	—	—	—
	ADDS, SUBS	—	L	—	—	—	—	—	—	—	—	—	—	—	—
	INC, DEC	—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	DAA, DAS	—	B	—	—	—	—	—	—	—	—	—	—	—	—
	MULXU, DIVXU	—	BW	—	—	—	—	—	—	—	—	—	—	—	—
	MULXS, DIVXS	—	BW	—	—	—	—	—	—	—	—	—	—	—	—
	NEG	—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	EXTU, EXTS	—	WL	—	—	—	—	—	—	—	—	—	—	—	—
	TAS*2	—	—	B	—	—	—	—	—	—	—	—	—	—	—
Logic operations	AND, OR, XOR	BWL	BWL	—	—	—	—	—	—	—	—	—	—	—	—
	NOT	—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
Shift		—	BWL	—	—	—	—	—	—	—	—	—	—	—	—
Bit-manipulation		—	B	B	—	—	—	B	B	—	B	—	—	—	—
Branch	Bcc, BSR	—	—	—	—	—	—	—	—	—	—	○	○	—	—
	JMP, JSR	—	—	—	—	—	—	—	—	○	—	—	—	○	—
	RTS	—	—	—	—	—	—	—	—	—	—	—	—	—	○

Section 3 MCU Operating Modes

3.1 Overview

3.1.1 Operating Mode Selection

This LSI has three operating modes (modes 1 to 3). These modes enable selection of the CPU operating mode and enabling/disabling of on-chip ROM, by setting the mode pins (MD1 and MD0).

Table 3.1 lists the MCU operating modes.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM
0	0	0	—	—	—
1		1	Normal	Expanded mode with on-chip ROM disabled	Disabled
2	1	0	Advanced	Expanded mode with on-chip ROM enabled	Enabled
				Single-chip mode	
3		1	Normal	Expanded mode with on-chip ROM enabled	
				Single-chip mode	

The CPU's architecture allows for 4 Gbytes of address space, but this LSI actually access a maximum of 16 Mbytes.

Mode 1 is an externally expanded mode that allows access to external memory and peripheral devices. With modes 2 and 3, operation begins in single-chip mode after reset release, but a transition can be made to external expansion mode by setting the EXPE bit in MDCR.

This LSI can only be used in modes 1 to 3. These means that the mode pins must select one of these modes. Do not changes the inputs at the mode pins during operation.

5.5.4 Interrupt Exception Handling Sequence

Figure 5.11 shows the interrupt exception handling sequence. The example shown is for the case where interrupt control mode 0 is set in advanced mode, and the program area and stack area are in on-chip memory.

6.2 Register Descriptions

6.2.1 Bus Control Register (BCR)

Bit	7	6	5	4	3	2	1	0
	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	IOS1	IOS0
Initial value	1	1	0	1	0	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCR is an 8-bit readable/writable register that specifies the external memory space access mode, and the extent of the I/O area when the I/O strobe function has been selected for the $\overline{AS}$ pin.

BCR is initialized to H'D7 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Idle Cycle Insert 1 (ICIS1): Reserved. Do not write 0 to this bit.

Bit 6—Idle Cycle Insert 0 (ICIS0): Selects whether or not a one-state idle cycle is to be inserted between bus cycles when successive external read and external write cycles are performed.

Bit 6

ICIS0	Description
0	Idle cycle not inserted in case of successive external read and external write cycles
1	Idle cycle inserted in case of successive external read and external write cycles (Initial value)

Bit 5—Burst ROM Enable (BRSTRM): Selects whether external space is designated as a burst ROM interface space. The selection applies to the entire external space.

Bit 5

BRSTRM	Description
0	Basic bus interface (Initial value)
1	Burst ROM interface

8.4.3 Pin Functions in Each Mode

Modes 1, 2, and 3 (EXPE = 1)

In modes 1, 2, and 3 (when EXPE = 1), port 3 pins automatically function as data I/O pins. The port 3 pin functions are shown in figure 8.10.

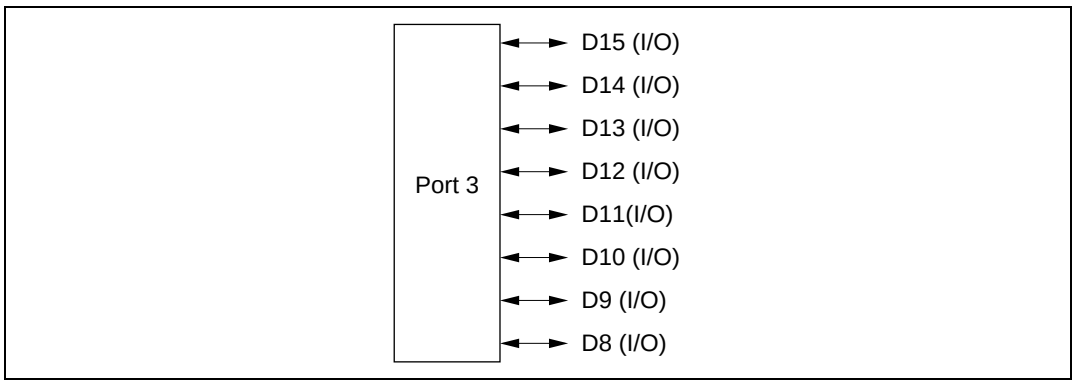


Figure 8.10 Port 3 Pin Functions (Modes 1, 2, and 3 (EXPE = 1))

Modes 2 and 3 (EXPE = 0)

In modes 2 and 3 (when EXPE = 0), port 3 functions as host interface data bus I/O pins (HDB7 to HDB0) or as I/O ports. When the HI12E bit is set to 1 in SYSCR2 and a transition is made to slave mode, port 3 functions as the host interface data bus. In slave mode, P3DR and P3DDR should be cleared to H'00. When the HI12E bit is cleared to 0, port 3 functions as an I/O port, and input or output can be specified on a bit-by-bit basis. When a bit in P3DDR is set to 1, the corresponding pin functions as an output port, and when cleared to 0, as an input port.

The port 3 pin functions are shown in figure 8.11.

Table 9.3 Resolution, PWM Conversion Period, and Carrier Frequency when ϕ = 20 MHz

Internal Clock Frequency	Resolution	PWM Conversion Period	Carrier Frequency
ϕ	50 ns	12.8 µs	1250 kHz
ϕ/2	100 ns	25.6 µs	625 kHz
ϕ/4	200 ns	51.2 µs	312.5 kHz
ϕ/8	400 ns	102.4 µs	156.3 kHz
ϕ/16	800 ns	204.8 µs	78.1 kHz

Bit 5—Reserved: This bit is always read as 1 and cannot be modified.

Bit 4—Reserved: This bit is always read as 0 and cannot be modified.

Bits 3 to 0—Register Select (RS3 to RS0): These bits select the PWM data register.

Bit 3	Bit 2	Bit 1	Bit 0	
RS3	RS2	RS1	RS0	Register Selection
0	0	0	0	PWDR0 selected
			1	PWDR1 selected
		1	0	PWDR2 selected
			1	PWDR3 selected
	1	0	0	PWDR4 selected
			1	PWDR5 selected
		1	0	PWDR6 selected
			1	PWDR7 selected
1	0	0	0	PWDR8 selected
			1	PWDR9 selected
		1	0	PWDR10 selected
			1	PWDR11 selected
	1	0	0	PWDR12 selected
			1	PWDR13 selected
		1	0	PWDR14 selected
			1	PWDR15 selected

Bit 7

ICRDMS	Description	
0	The normal operating mode is specified for ICRD	(Initial value)
1	The operating mode using OCRDM is specified for ICRD	

Bit 6—Output Compare A Mode Select (OCRAMS): Specifies whether OCRA is used in the normal operating mode or in the operating mode using OCRAR and OCRAF.

Bit 6

OCRAMS	Description	
0	The normal operating mode is specified for OCRA	(Initial value)
1	The operating mode using OCRAR and OCRAF is specified for OCRA	

Bit 5—Input Capture Register Select (ICRS): The same addresses are shared by ICRA and OCRAR, by ICRB and OCRAF, and by ICRC and OCRDM. The ICRS bit determines which registers are selected when the shared addresses are read or written to. The operation of ICRA, ICRB, and ICRC is not affected.

Bit 5

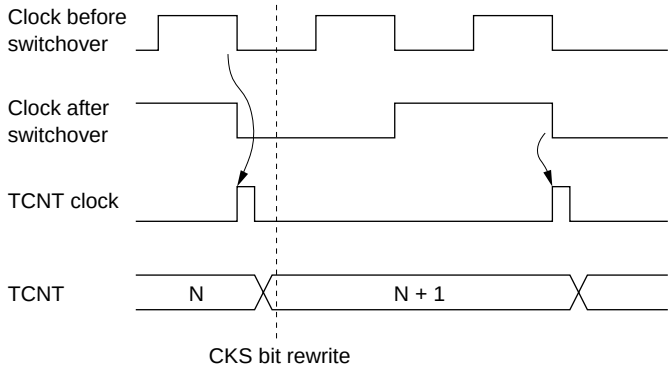
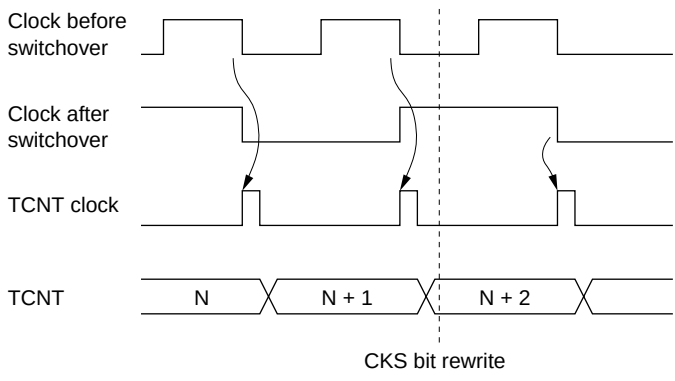
ICRS	Description	
0	The ICRA, ICRB, and ICRC registers are selected	(Initial value)
1	The OCRAR, OCRAF, and OCRDM registers are selected	

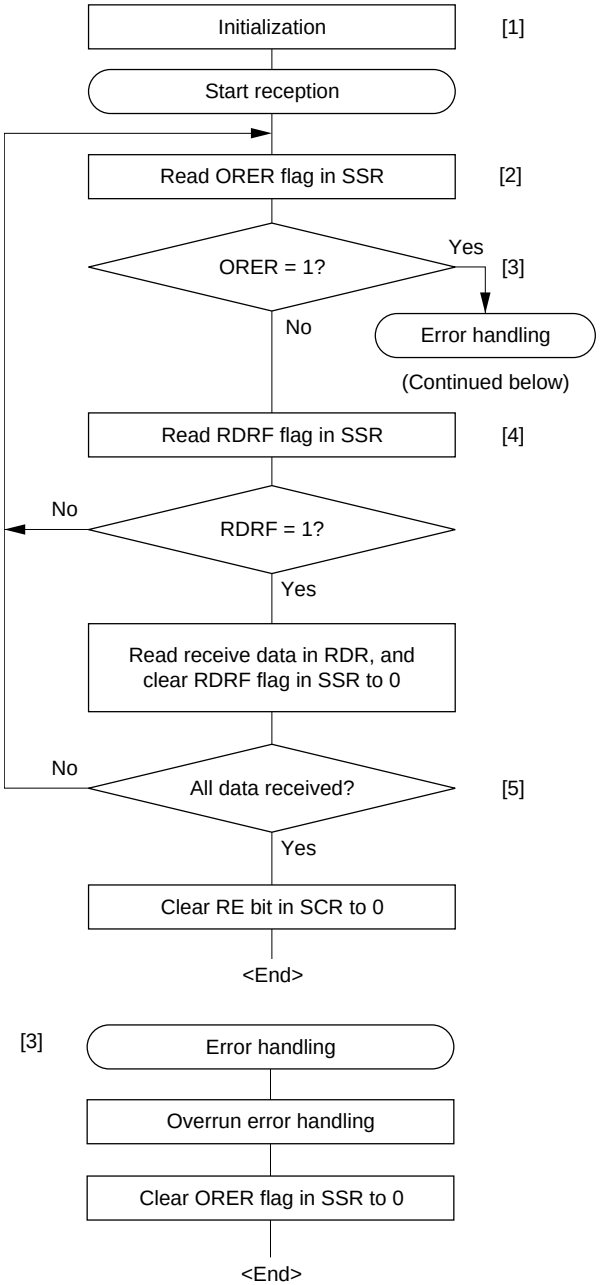
Bit 4—Output Compare Register Select (OCRS): OCRA and OCRB share the same address. When this address is accessed, the OCRS bit selects which register is accessed. This bit does not affect the operation of OCRA or OCRB.

Bit 4

OCRS	Description	
0	The OCRA register is selected	(Initial value)
1	The OCRB register is selected	

Table 12.8 Switching of Internal Clock and TCNT Operation

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
1	Switching from low to low*1	
2	Switching from low to high*2	



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error handling:
If a receive error occurs, read the ORER flag in SSR , and after performing the appropriate error handling, clear the ORER flag to 0. Transfer cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0. The RDRF flag is cleared automatically when the DTC is activated by a receive-data-full interrupt (RXI) request and the RDR value is read.

Figure 15.18 Sample Serial Reception Flowchart

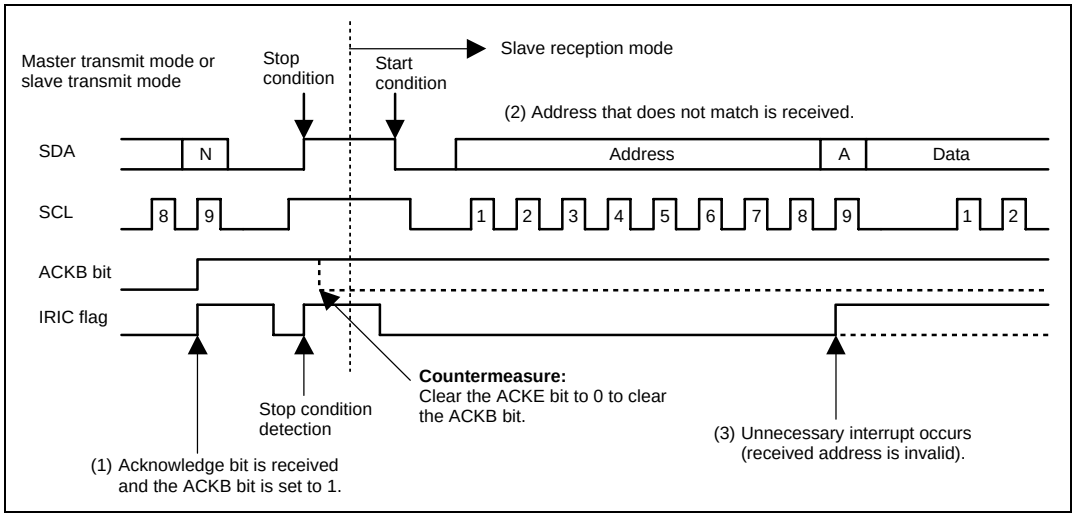


Figure 16.25 Note on Interrupt Occurrence in Slave Mode after ACKB = 1 Reception

Bit 0—Output Buffer Full (OBF): Set to 1 when the slave processor writes to ODR1. Cleared to 0 when the host processor reads ODR.

Bit 0

OBF	Description
0	[Clearing condition]
	When the host processor reads ODR or the slave writes 0 in the OBF bit (Initial value)
1	[Setting condition]
	When the slave processor writes to ODR

Table 18.3 shows the conditions for setting and clearing the STR flags.

Table 18.3 Set/Clear Timing for STR Flags

Flag	Setting Condition	Clearing Condition
C/$\overline{D}$	Rising edge of host's write signal ($\overline{IOW}$) when HA0 is high	Rising edge of host's write signal ($\overline{IOW}$) when HA0 is low
IBF*	Rising edge of host's write signal ($\overline{IOW}$) when writing to IDR1	Falling edge of slave's internal read signal ($\overline{RD}$) when reading IDR1
OBF	Falling edge of slave's internal write signal ($\overline{WR}$) when writing to ODR1	Rising edge of host's read signal ($\overline{IOR}$) when reading ODR1

Note: * The IBF flag setting and clearing conditions are different when the fast A20 gate is used. For details see table 18.7.

19.3 Operation

The D/A converter module has two built-in D/A converter circuits that can operate independently.

D/A conversion is performed continuously whenever enabled by the D/A control register (DACR). When a new value is written in DADR0 or DADR1, conversion of the new value begins immediately. The converted result is output by setting the DAOE0 or DAOE1 bit to 1.

An example of conversion on channel 0 is given next. Figure 19.2 shows the timing.

- Software writes the data to be converted in DADR0.
- D/A conversion begins when the DAOE0 bit in DACR is set to 1. After the elapse of the conversion time, analog output appears at the DA0 pin. The output value is AVref × (DADR value)/256.

  This output continues until a new value is written in DADR0 or the DAOE0 bit is cleared to 0.
- If a new value is written in DADR0, conversion begins immediately. Output of the converted result begins after the conversion time.
- When the DAOE0 bit is cleared to 0, DA0 becomes an input pin.

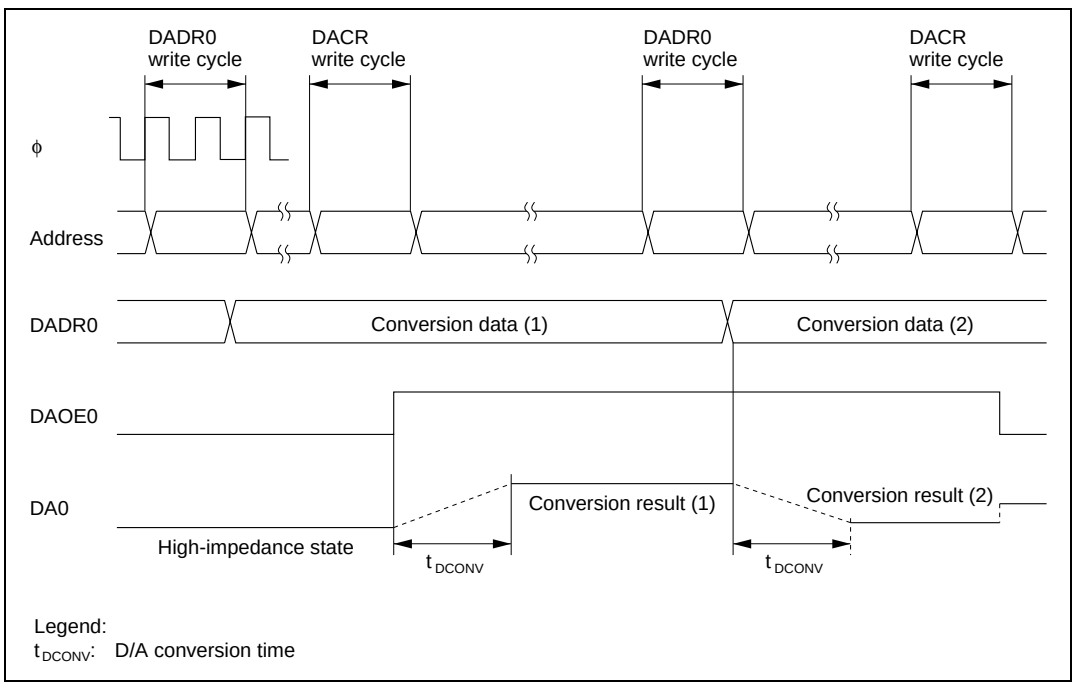


Figure 19.2 D/A Conversion (Example)

Table 26.36 Bus Timing (2) (Advanced mode)

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

Condition B: V_{CC} = 3.0 V to 5.5 V, $V_{CC}B$ = 3.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

		Condition A		Condition B			
		20 MHz		10 MHz			
Item	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Address delay time	t_{AD}	—	30	—	60	ns	Figure 26.10 to figure 26.14
Address setup time	t_{AS}	0.5 × t_{cyc} –25	—	0.5 × t_{cyc} –50	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} –10	—	0.5 × t_{cyc} –20	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	30	—	60	ns	
$\overline{AS}$ delay time	t_{ASD}	—	30	—	60	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	30	—	60	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	30	—	60	ns	
Read data setup time	t_{RDS}	15	—	35	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} –40	—	1.0 × t_{cyc} –80	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} –25	—	1.5 × t_{cyc} –50	ns	

Instruction	Mnemonic		Instruction Fetch I	Branch Address Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
BXOR	BXOR #xx:3,Rd		1					
	BXOR #xx:3,@ERd		2			1		
	BXOR #xx:3,@aa:8		2			1		
	BXOR #xx:3,@aa:16		3			1		
	BXOR #xx:3,@aa:32		4			1		
CLRMAC	CLRMAC		Cannot be used with this LSI.					
CMP	CMP.B #xx:8,Rd		1					
	CMP.B Rs,Rd		1					
	CMP.W #xx:16,Rd		2					
	CMP.W Rs,Rd		1					
	CMP.L #xx:32,ERd		3					
	CMP.L ERs,ERd		1					
DAA	DAA Rd		1					
DAS	DAS Rd		1					
DEC	DEC.B Rd		1					
	DEC.W #1/2,Rd		1					
	DEC.L #1/2,ERd		1					
DIVXS	DIVXS.B Rs,Rd		2					11
	DIVXS.W Rs,ERd		2					19
DIVXU	DIVXU.B Rs,Rd		1					11
	DIVXU.W Rs,ERd		1					19
EEPMOV	EEPMOV.B		2			2n+2*2		
	EEPMOV.W		2			2n+2*2		
EXTS	EXTS.W Rd		1					
	EXTS.L ERd		1					
EXTU	EXTU.W Rd		1					
	EXTU.L ERd		1					
INC	INC.B Rd		1					
	INC.W #1/2,Rd		1					
	INC.L #1/2,ERd		1					
JMP	JMP @ERn		2					
	JMP @aa:24		2					1
	JMP @@aa:8	Normal	2	1				1
		Advanced	2	2				1

MRA—DTC Mode Register A **H'EC00–H'EFFF** **DTC**

Bit	7	6	5	4	3	2	1	0
	SM1	SM0	DM1	DM0	MD1	MD2	DTS	Sz
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

DTC data transfer size

0	Byte-size transfer
1	Word-size transfer

DTC transfer mode select

0	Destination side is repeat area or block area
1	Source side is repeat area or block area

DTC mode

0	0	Normal mode
	1	Repeat mode
1	0	Block transfer mode
	1	—

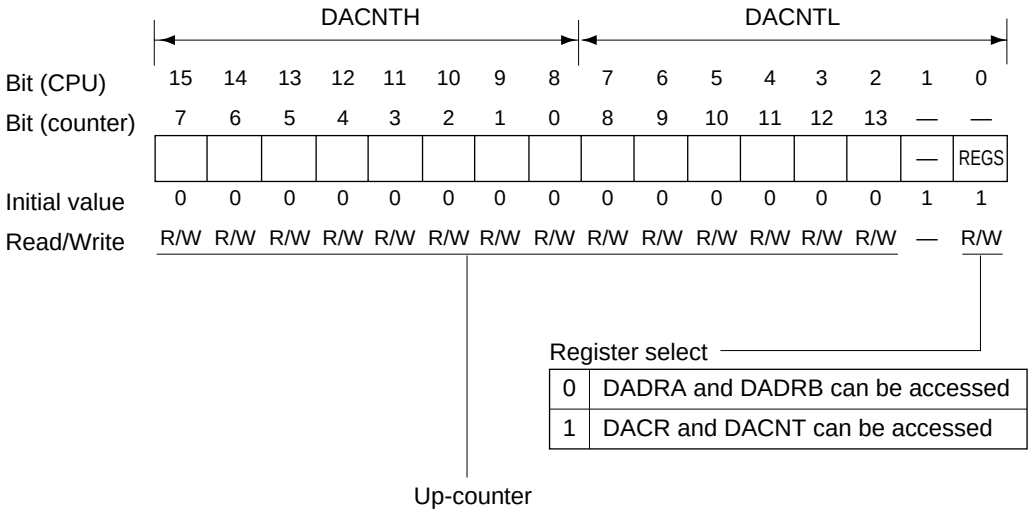
Destination address mode

0	—	DAR is fixed
1	0	DAR is incremented after a transfer (by 1 when Sz = 0; by 2 when Sz = 1)
	1	DAR is decremented after a transfer (by 1 when Sz = 0; by 2 when Sz = 1)

Source address mode

0	—	SAR is fixed
1	0	SAR is incremented after a transfer (by 1 when Sz = 0; by 2 when Sz = 1)
	1	SAR is decremented after a transfer (by 1 when Sz = 0; by 2 when Sz = 1)

DACNTH—PWM (D/A) Counter H **H'FFA6** **PWMX**
DACNTL—PWM (D/A) Counter L **H'FFA7** **PWMX**



C.11 Port B Block Diagram

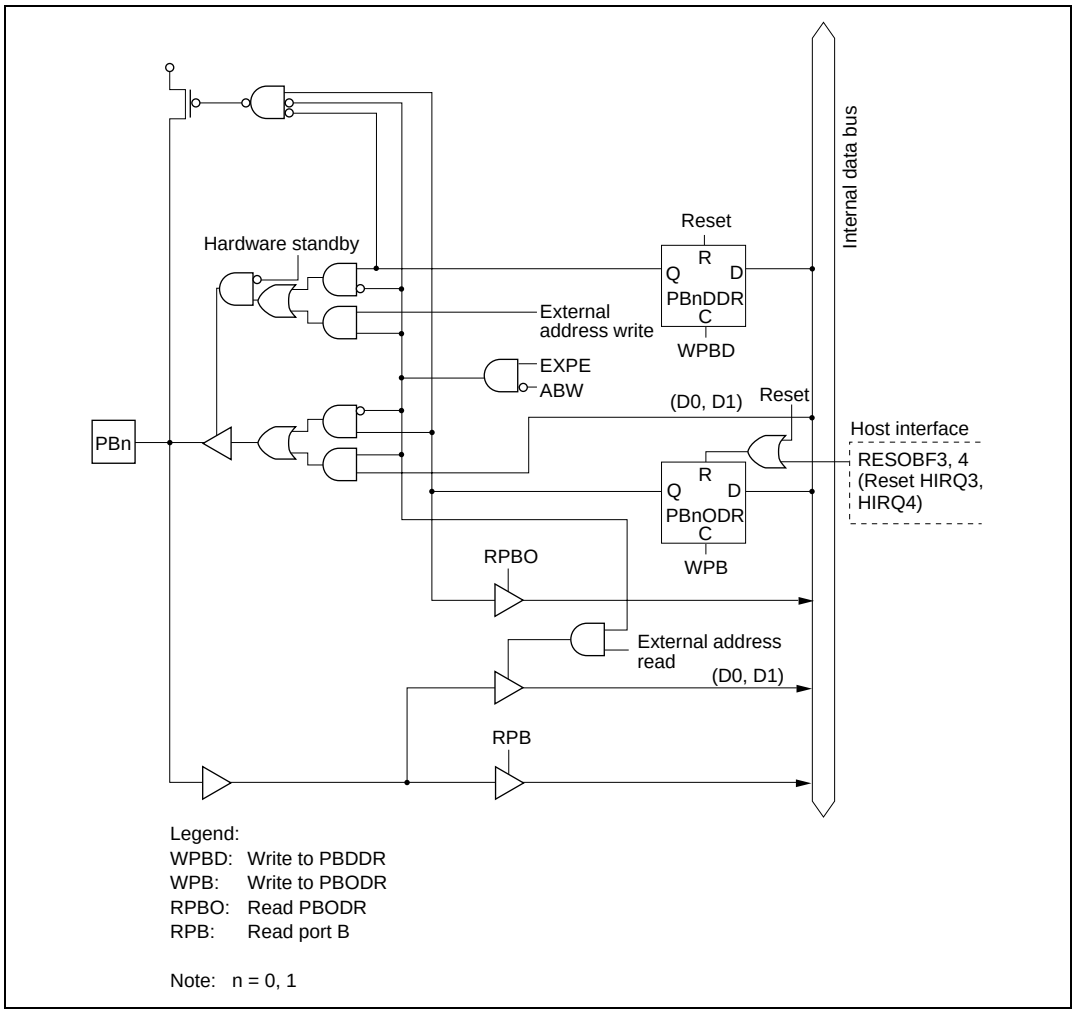


Figure C.37 Port B Block Diagram (Pins PB0 and PB1)