Renesas Electronics America Inc - DF2148AVFA10V Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2148avfa10v

Pin No.	Pin Name			
	Expanded Modes		Single-Chip Modes	
FP-100B TFP-100B	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)	Flash Memory Writer Mode
72	A7	A7/P17	P17	FA7
73	A6	A6/P16	P16	FA6
74	A5	A5/P15	P15	FA5
75	A4	A4/P14	P14	FA4
76	A3	A3/P13	P13	FA3
77	A2	A2/P12	P12	FA2
78	A1	A1/P11	P11	FA1
79	A0	A0/P10	P10	FA0
80	PB3/D3	PB3/D3	PB3	NC
81	PB2/D2	PB2/D2	PB2	NC
82	D8	D8	P30	FO0
83	D9	D9	P31	FO1
84	D10	D10	P32	FO2
85	D11	D11	P33	FO3
86	D12	D12	P34	FO4
87	D13	D13	P35	FO5
88	D14	D14	P36	FO6
89	D15	D15	P37	FO7
90	PB1/D1	PB1/D1	PB1	NC
91	PB0/D0	PB0/D0	PB0	NC
92	VSS	VSS	VSS	VSS
93	P80	P80	P80	NC
94	P81	P81	P81	NC
95	P82	P82	P82	NC
96	P83	P83	P83	NC
97	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1	NC
98	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1	NC
99	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1	NC
100	$\overline{\text{RESO}}$	$\overline{\text{RESO}}$	$\overline{\text{RESO}}$	NC

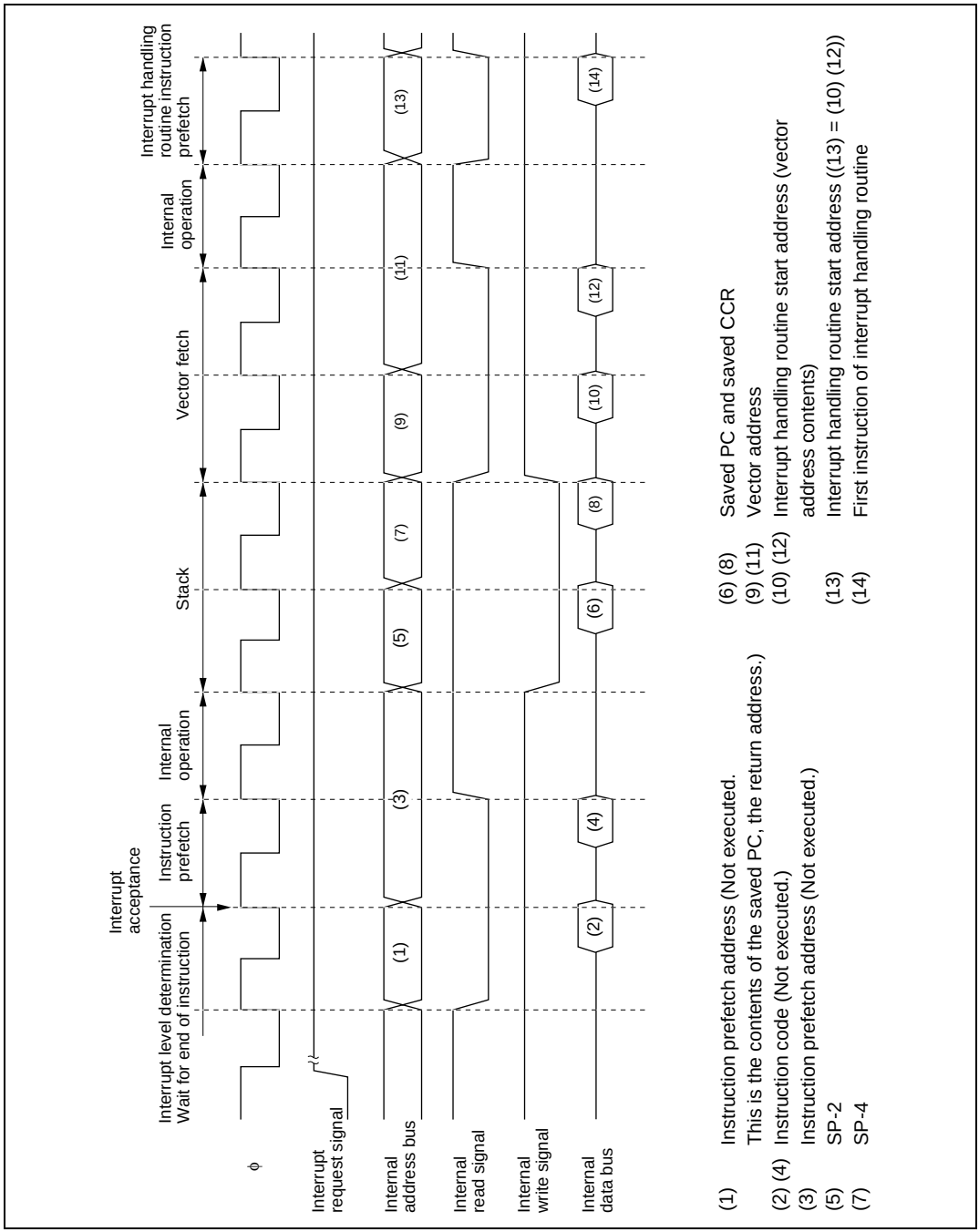

Figure 5.11 Interrupt Exception Handling

6.5.3 Wait Control

As with the basic bus interface, either program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) of the burst ROM interface. See section 6.4.5, Wait Control.

Wait states cannot be inserted in a burst cycle.

6.6 Idle Cycle

6.6.1 Operation

When this LSI chip accesses external space, it can insert a 1-state idle cycle (T_i) between bus cycles when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, with a long output floating time, and high-speed memory, I/O interfaces, and so on.

If an external write occurs after an external read while the ICIS0 bit in BCR is set to 1, an idle cycle is inserted at the start of the write cycle. This is enabled in advanced mode and normal mode.

Figure 6.15 shows an example of the operation in this case. In this example, bus cycle A is a read cycle from ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

MSTPCRH Bit 4—Module Stop (MSTP12): Specifies 8-bit timer channel 0 and 1 module stop mode.

MSTPCRH Bit 4		
MSTP12	**Description**	
0	8-bit timer channel 0 and 1 module stop mode is cleared	
1	8-bit timer channel 0 and 1 module stop mode is set	(Initial value)

MSTPCRH Bit 0—Module Stop (MSTP8): Specifies 8-bit timer channel X and Y and timer connection module stop mode.

MSTPCRH Bit 0		
MSTP8	**Description**	
0	8-bit timer channel X and Y and timer connection module stop mode is cleared	
1	8-bit timer channel X and Y and timer connection module stop mode is set	(Initial value)

13.3 Operation

13.3.1 PWM Decoding (PDC Signal Generation)

The timer connection facility and TMRX can be used to decode a PWM signal in which 0 and 1 are represented by the pulse width. To do this, a signal in which a rising edge is generated at regular intervals must be selected as the IHI signal.

The timer counter (TCNT) in TMRX is set to count the internal clock pulses and to be cleared on the rising edge of the external reset signal (IHI signal). The value to be used as the threshold for deciding the pulse width is written in TCORB. The PWM decoder contains a delay latch which uses the IHI signal as data and compare-match signal B (CMB) as a clock, and the state of the IHI signal (the result of the pulse width decision) at the compare-match signal B timing after TCNT is reset by the rise of the IHI signal is output as the PDC signal. The pulse width setting using TICRR and TICRF of TMRX can be used to determine the pulse width decision threshold. Examples of TCR and TCORB settings are shown in tables 13.3 and 13.4, and the timing chart is shown in figure 13.2.

15.3.3 Multiprocessor Communication Function

The multiprocessor communication function performs serial communication using a multiprocessor format, in which a multiprocessor bit is added to the transfer data, in asynchronous mode. Use of this function enables data transfer to be performed among a number of processors sharing transmission lines.

When multiprocessor communication is carried out, each receiving station is addressed by a unique ID code.

The serial communication cycle consists of two component cycles: an ID transmission cycle which specifies the receiving station, and a data transmission cycle. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle.

The transmitting station first sends the ID of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added.

The receiving station skips the data until data with a 1 multiprocessor bit is sent.

When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose ID does not match continue to skip the data until data with a 1 multiprocessor bit is again received. In this way, data communication is carried out among a number of processors.

Figure 15.9 shows an example of inter-processor communication using a multiprocessor format.

Data Transfer Format

There are four data transfer formats.

When a multiprocessor format is specified, the parity bit specification is invalid.

For details, see table 15.10.

Clock

See the section on asynchronous mode.

Bit 7—I²C Extra Buffer Select (IICS): Designates bits 7 to 4 of port A as the same kind of output buffer as SCL and SDA. This bit is used when implementing the I²C interface by software only.

Bit 7

IICS	Description	
0	PA7 to PA4 are normal I/O pins	(Initial value)
1	PA7 to PA4 are I/O pins with bus driving capability	

Bits 6 and 5—I²C Transfer Select 1 and 0 (IICX1 and 0): This bit, together with bits CKS2 to CKS0 in ICMR, selects the transfer rate in master mode. For details, see section 16.2.4, I²C Bus Mode Register (ICMR).

Bit 4—I²C Master Enable (IICE): Controls CPU access to the I²C bus interface data and control registers (ICCR, ICSR, ICDR/SARX, ICMR/SAR).

Bit 4

IICE	Description	
0	CPU access to I²C bus interface data and control registers is disabled	(Initial value)
1	CPU access to I²C bus interface data and control registers is enabled	

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers, the power-down mode control registers, and the supporting module control registers. See section 3.2.4, Serial Timer Control Register (STCR), for details.

Bit 2—Reserved: Do not write 1 to this bit.

Bits 1 and 0—Internal Clock Source Select 1 and 0 (ICKS1, ICSK0): These bits, together with bits CKS2 to CKS0 in TCR, select the clock input to the timer counters (TCNT). For details, see section 12.2.4, Timer Control Register (TCR).

16.3.8 Operation Using the DTC

The I²C bus format provides for selection of the slave device and transfer direction by means of the slave address and the R/$\overline{W}$ bit, confirmation of reception with the acknowledge bit, indication of the last frame, and so on. Therefore, continuous data transfer using the DTC must be carried out in conjunction with CPU processing by means of interrupts.

Table 16.5 shows some examples of processing using the DTC. These examples assume that the number of transfer data bytes is known in slave mode.

Table 16.5 Examples of Operation Using the DTC

Item	Master Transmit Mode	Master Receive Mode	Slave Transmit Mode	Slave Receive Mode
Slave address + R/$\overline{W}$ bit transmission/ reception	Transmission by DTC (ICDR write)	Transmission by CPU (ICDR write)	Reception by CPU (ICDR read)	Reception by CPU (ICDR read)
Dummy data read	—	Processing by CPU (ICDR read)	—	—
Actual data transmission/ reception	Transmission by DTC (ICDR write)	Reception by DTC (ICDR read)	Transmission by DTC (ICDR write)	Reception by DTC (ICDR read)
Dummy data (H'FF) write	—	—	Processing by DTC (ICDR write)	—
Last frame processing	Not necessary	Reception by CPU (ICDR read)	Not necessary	Reception by CPU (ICDR read)
Transfer request processing after last frame processing	1st time: Clearing by CPU 2nd time: End condition issuance by CPU	Not necessary	Automatic clearing on detection of end condition during transmission of dummy data (H'FF)	Not necessary
Setting of number of DTC transfer data frames	Transmission: Actual data count + 1 (+1 equivalent to slave address + R/$\overline{W}$ bits)	Reception: Actual data count	Transmission: Actual data count + 1 (+1 equivalent to dummy data (H'FF))	Reception: Actual data count

18.2.3 Host Interface Control Register (HICR)

- HICR

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	IBFIE2	IBFIE1	FGA20E
Initial value	1	1	1	1	1	0	0	0
Slave Read/Write	—	—	—	—	—	R/W	R/W	R/W
Host Read/Write	—	—	—	—	—	—	—	—

- HICR2

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	IBFIE4	IBFIE3	—
Initial value	1	1	1	1	1	0	0	0
Slave Read/Write	—	—	—	—	—	R/W	R/W	—
Host Read/Write	—	—	—	—	—	—	—	—

HICR is an 8-bit readable/writable register which controls host interface channel 1 and 2 interrupts and the fast A20 gate function. HICR2 is an 8-bit readable/writable register which controls host interface channel 3 and 4 interrupts. HICR and HICR2 are initialized to H'F8 by a reset and in hardware standby mode.

Bits 7 to 3—Reserved: These bits cannot be modified and are always read as 1.

HICR Bits 2 and 1—Input Data Register Full Interrupt Enable 2 and 1 (IBFIE2, IBFIE1)
HICR2 Bits 2 and 1—Input Data Register Full Interrupt Enable 4 and 3 (IBFIE4, IBFIE3)
These bits enable or disable the IBF1, IBF2, IBF3, and IBF4 interrupts to the internal CPU.

20.2.4 Keyboard Comparator Control Register (KBCOMP)

Bit	7	6	5	4	3	2	1	0
	IrE	IrCKS2	IrCKS1	IrCKS0	KBADE	KBCH2	KBCH1	KBCH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

KBCOMP is an 8-bit readable/writable register that controls the SCI2 IrDA function and selects the CIN input channels for A/D conversion.

KBCOMP is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 4—IrDA Control: See the description in section 15.2.11, Keyboard Comparator Control Register (KBCOMP).

Bit 3—Keyboard A/D Enable (KBADE): Selects either analog input pins (AN6, AN7) or digital input pins (CIN0 to CIN7, CIN8 to CIN15) for A/D converter channel 6 and channel 7 input.

Bits 2 to 0—Keyboard A/D Channel Select 2 to 0 (KBCH2 to KBCH0): These bits select the channels for A/D conversion from among the digital input pins. Only set the input channel while A/D conversion is stopped.

Bit 3	Bit 2	Bit 1	Bit 0	A/D Converter	A/D Converter
KBADE	KBCH2	KBCH1	KBCH0	Channel 6 Input	Channel 7 Input
0	—	—	—	AN6	AN7
1	0	0	0	CIN0	CIN8
			1	CIN1	CIN9
		1	0	CIN2	CIN10
			1	CIN3	CIN11
	1	0	0	CIN4	CIN12
			1	CIN5	CIN13
		1	0	CIN6	CIN14
			1	CIN7	CIN15

23.4 Overview of Flash Memory

23.4.1 Features

The features of the flash memory are summarized below.

- Four flash memory operating modes
  - Program mode
  - Erase mode
  - Program-verify mode
  - Erase-verify mode
- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erasing is performed by block erase (in single-block units). When erasing multiple blocks, the individual blocks must be erased sequentially. Block erasing can be performed as required on 1-kbyte, 28-kbyte, 16-kbyte, 8-kbyte, and 32-kbyte blocks.
- Programming/erase times

  The flash memory programming time is 10 ms (typ.) for simultaneous 128-byte programming, equivalent to approximately 80 µs (typ.) per byte, and the erase time is 100 ms (typ.) per block.
- Reprogramming capability

  The flash memory can be reprogrammed up to 100 times.
- On-board programming modes

  There are two modes in which flash memory can be programmed/erased/verified on-board:
  - Boot mode
  - User program mode
- Automatic bit rate adjustment

  With data transfer in boot mode, the bit rate of the chip can be automatically adjusted to match the transfer bit rate of the host.
- Protect modes

  There are three protect modes, hardware, software, and error protect, which allow protected status to be designated for flash memory program/erase/verify operations.
- Programmer mode

  Flash memory can be programmed/erased in programmer mode, using a PROM programmer, as well as in on-board programming mode.

External Clock

The external clock signal should have the same frequency as the system clock (ϕ).

Table 24.4 and figure 24.6 show the input conditions for the external clock.

Table 24.4 External Clock Input Conditions

		V_{cc} = 2.7 to 5.5 V		V_{cc} = 5.0 V ±10%				
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
External clock input low pulse width	t_{EXL}	40	—	20	—	ns	Figure 24.6	
External clock input high pulse width	t_{EXH}	40	—	20	—	ns		
External clock rise time	t_{EXr}	—	10	—	5	ns		
External clock fall time	t_{EXf}	—	10	—	5	ns		
Clock low pulse width	t_{CL}	0.4	0.6	0.4	0.6	t_{cyc}	ϕ ≥ 5 MHz	Figure 26.5
		80	—	80	—	ns	ϕ < 5 MHz	
Clock high pulse width	t_{CH}	0.4	0.6	0.4	0.6	t_{cyc}	ϕ ≥ 5 MHz	
		80	—	80	—	ns	ϕ < 5 MHz	

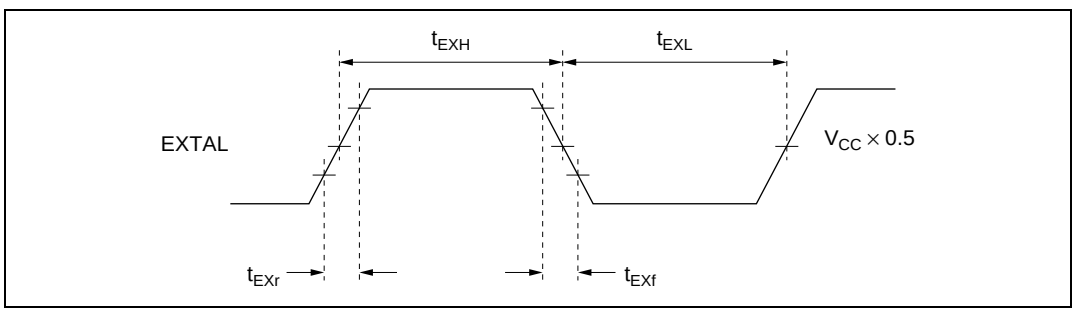

Figure 24.6 External Clock Input Timing

Table 24.5 shows the external clock output settling delay time, and figure 24.7 shows the external clock output settling delay timing. The oscillator and duty adjustment circuit have a function for adjusting the waveform of the external clock input at the EXTAL pin. When the prescribed clock signal is input at the EXTAL pin, internal clock signal output is fixed after the elapse of the

24.9 Clock Selection Circuit

This circuit selects the system clock used in the MCU.

The clock signal generated in the EXTAL/XTAL pin oscillator is selected as the system clock when MCU is returned from high-speed mode, medium-speed mode, sleep mode, reset state, or standby mode.

In sub-active mode, sub-sleep mode, and watch mode, the sub-clock signal input from EXCL pin is selected as the system clock. In these modes, modules such as CPU, TMR0, TMR1, WDT0, WDT1, and I/O ports operate on the ϕ SUB clock. The count clock for each timer is a clock obtained by driving the ϕ SUB clock.

For details, see the description of Clock Select 2 to 0 in section 14.2.2, Timer Control/Status Register (TCSR).

Bit 4

PSS	Description
0	TCNT counts ϕ-based prescaler (PSM) divided clock pulses When a SLEEP instruction is executed in high-speed mode or medium-speed mode, a transition is made to sleep mode or software standby mode (Initial value)
1	TCNT counts ϕSUB-based prescaler (PSM) divided clock pulses When a SLEEP instruction is executed in high-speed mode or medium-speed mode, a transition is made to sleep mode, watch mode*, or subactive mode* When a SLEEP instruction is executed in subactive mode, a transition is made to subsleep mode, watch mode, or high-speed mode

Note: * When a transition is made to watch mode or subactive mode, high-speed mode must be set.

25.2.4 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR comprises two 8-bit readable/writable registers that perform module stop mode control.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

MSTRCRH and MSTPCRL Bits 7 to 0—Module Stop (MSTP 15 to MSTP 0): These bits specify module stop mode. See table 25.4 for the method of selecting on-chip supporting modules.

MSTPCRH, MSTPCRL Bits 7 to 0

MSTP15 to MSTP0	Description	
0	Module stop mode is cleared	(Initial value of MSTP15, MSTP14)
1	Module stop mode is set	(Initial value of MSTP13 to MSTP0)

Using a Crystal Oscillator

Set bits STS2 to STS0 so that the standby time is at least 8 ms (the oscillation settling time).

Table 25.5 shows the standby times for different operating frequencies and settings of bits STS2 to STS0.

Table 25.5 Oscillation Settling Time Settings

STS2	STS1	STS0	Standby Time	20 MHz	16 MHz	12 MHz	10 MHz	8 MHz	6 MHz	4 MHz	2 MHz	Unit
0	0	0	8192 states	0.41	0.51	0.65	0.8	1.0	1.3	2.0	4.1	ms
		1	16384 states	0.82	1.0	1.3	1.6	2.0	2.7	4.1	[8.2]	
	1	0	32768 states	1.6	2.0	2.7	3.3	4.1	5.5	[8.2]	16.4	
		1	65536 states	3.3	4.1	5.5	6.6	[8.2]	[10.9]	16.4	32.8	
1	0	0	131072 states	6.6	[8.2]	[10.9]	[13.1]	16.4	21.8	32.8	65.5	
		1	262144 states	[13.1]	16.4	21.8	26.2	32.8	43.6	65.6	131.2	
	1	0	Reserved	—	—	—	—	—	—	—	—	µs
		1	16 states*	0.8	1.0	1.3	1.6	2.0	2.7	4.0	8.0	

[ ]: Recommended time setting
Note: * This setting must not be used in the flash memory version.

Using an External Clock

Any value can be set. Normally, use of the minimum time is recommended.

25.6.4 Software Standby Mode Application Example

Figure 25.3 shows an example in which a transition is made to software standby mode at the falling edge on the NMI pin, and software standby mode is cleared at the rising edge on the NMI pin.

In this example, an NMI interrupt is accepted with the NMIEG bit in SYSCR cleared to 0 (falling edge specification), then the NMIEG bit is set to 1 (rising edge specification), the SSBY bit is set to 1, and a SLEEP instruction is executed, causing a transition to software standby mode.

Software standby mode is then cleared at the rising edge on the NMI pin.

26.5 Electrical Characteristics of H8S/2144 F-ZTAT, H8S/2142 F-ZTAT, and Mask ROM Version of H8S/2142

26.5.1 Absolute Maximum Ratings

Table 26.44 lists the absolute maximum ratings.

Table 26.44 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage*	V_{CC}	–0.3 to +7.0	V
Input voltage (except ports 6, 7, and A)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port 6 and A)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input selected for port 6 and A)	V_{in}	–0.3 V to lower of voltages V_{CC} +0.3 and AV_{CC} +0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference supply voltage	AV_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Operating temperature (flash memory programming/erasing)	T_{opr}	Regular specifications: 0 to +75	°C
		Wide-range specifications: 0 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * Power supply voltage for VCC1 and VCC2 pins.

Item	Symbol	Condition A 20 MHz Min	Condition A 20 MHz Max	Condition B 16 MHz Min	Condition B 16 MHz Max	Condition C 10 MHz Min	Condition C 10 MHz Max	Unit	Test Conditions
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 40$	—	$1.0 \times t_{cyc} - 60$	ns	Figure 26.10 to figure 26.14
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 25$	—	$1.5 \times t_{cyc} - 35$	—	$1.5 \times t_{cyc} - 50$	ns	
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 30$	—	$2.0 \times t_{cyc} - 40$	—	$2.0 \times t_{cyc} - 60$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 25$	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 50$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 30$	—	$3.0 \times t_{cyc} - 40$	—	$3.0 \times t_{cyc} - 60$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	30	—	45	—	60	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	30	—	45	—	60	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 40$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 30$	—	$1.5 \times t_{cyc} - 40$	—	ns	
Write data delay time	t_{WDD}	—	30	—	45	—	60	ns	
Write data setup time	t_{WDS}	0	—	0	—	0	—	ns	
Write data hold time	t_{WDH}	10	—	15	—	20	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	45	—	60	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	10	—	ns	

Instruction	Mnemonic	Size	Instruction Format									
			1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte	9th Byte	10th Byte
ROTR	ROTR.B Rd	B	1 3	8 rd								
	ROTR.B #2, Rd	B	1 3	C rd								
	ROTR.W Rd	W	1 3	9 rd								
	ROTR.W #2, Rd	W	1 3	D rd								
	ROTR.L ERd	L	1 3	B 0 erd								
	ROTR.L #2, ERd	L	1 3	F 0 erd								
ROTXL	ROTXL.B Rd	B	1 2	0 rd								
	ROTXL.B #2, Rd	B	1 2	4 rd								
	ROTXL.W Rd	W	1 2	1 rd								
	ROTXL.W #2, Rd	W	1 2	5 rd								
	ROTXL.L ERd	L	1 2	3 0 erd								
	ROTXL.L #2, ERd	L	1 2	7 0 erd								
ROTXR	ROTXR.B Rd	B	1 3	0 rd								
	ROTXR.B #2, Rd	B	1 3	4 rd								
	ROTXR.W Rd	W	1 3	1 rd								
	ROTXR.W #2, Rd	W	1 3	5 rd								
	ROTXR.L ERd	L	1 3	3 0 erd								
	ROTXR.L #2, ERd	L	1 3	7 0 erd								
RTE	RTE	—	5 6	7 0								
RTS	RTS	—	5 4	7 0								
SHAL	SHAL.B Rd	B	1 0	8 rd								
	SHAL.B #2, Rd	B	1 0	C rd								
	SHAL.W Rd	W	1 0	9 rd								
	SHAL.W #2, Rd	W	1 0	D rd								
	SHAL.L ERd	L	1 0	B 0 erd								
	SHAL.L #2, ERd	L	1 0	F 0 erd								

C.6 Port 6 Block Diagrams

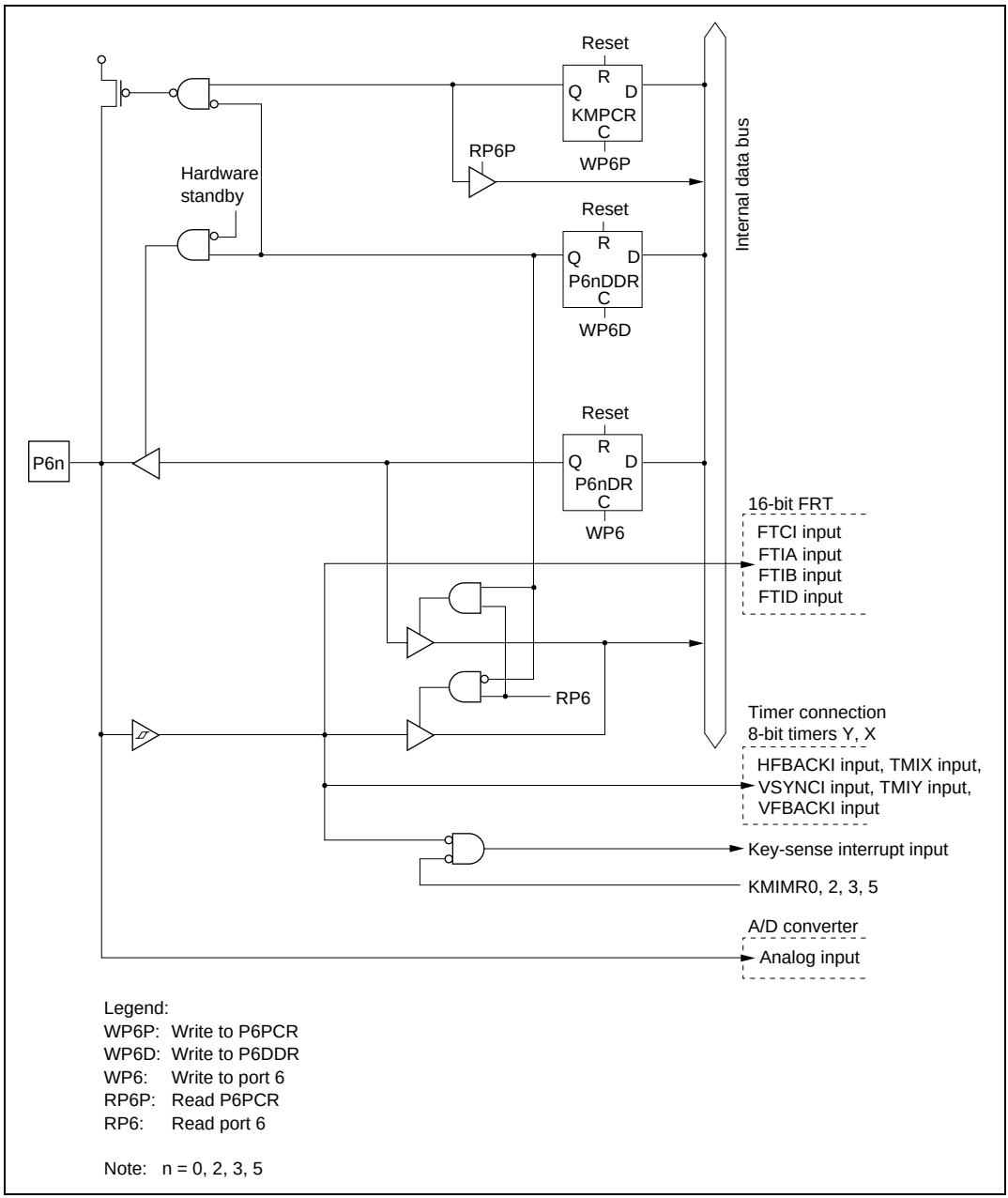

Figure C.16 Port 6 Block Diagram (Pins P60, P62, P63, P65)

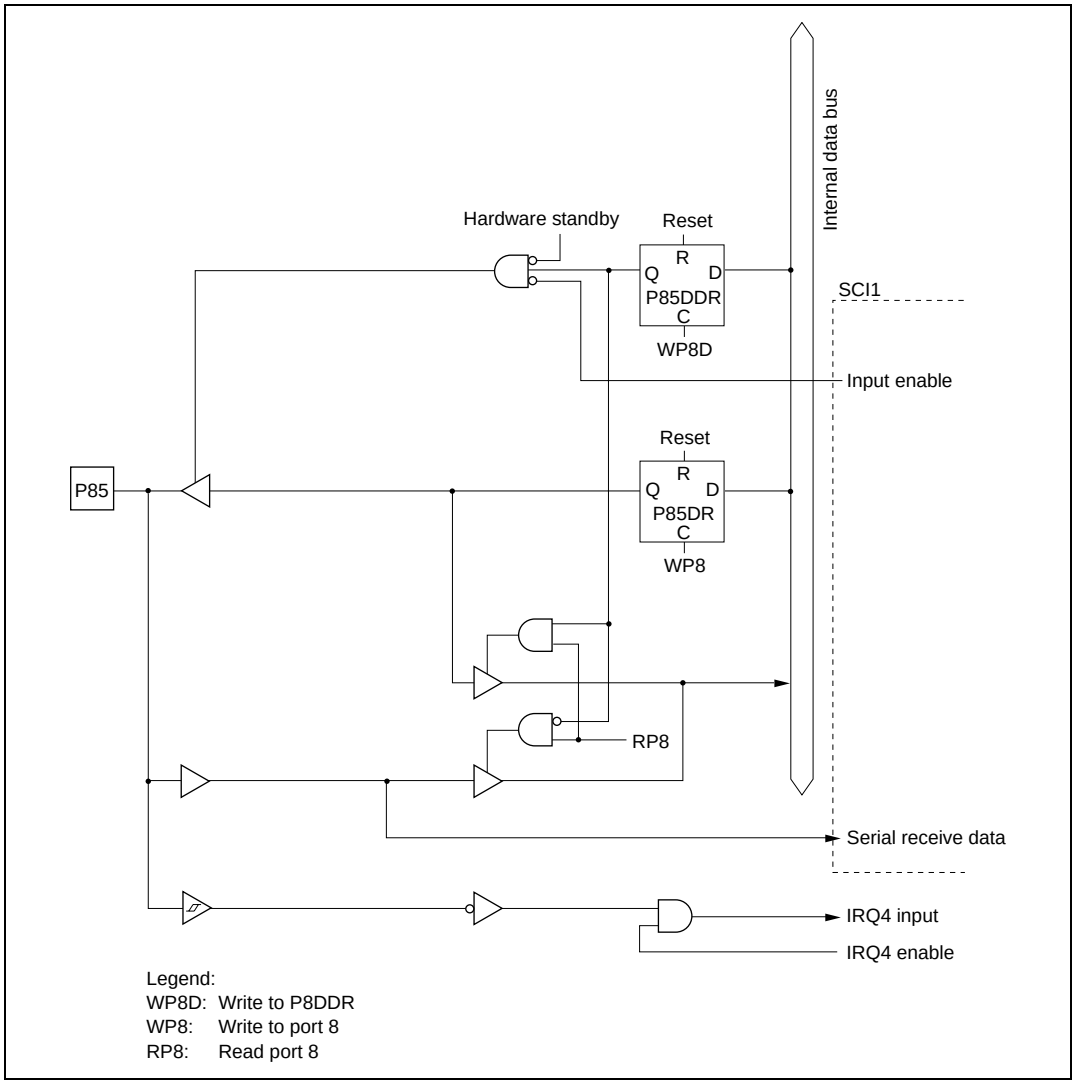

Figure C.27 Port 8 Block Diagram (Pin P85)