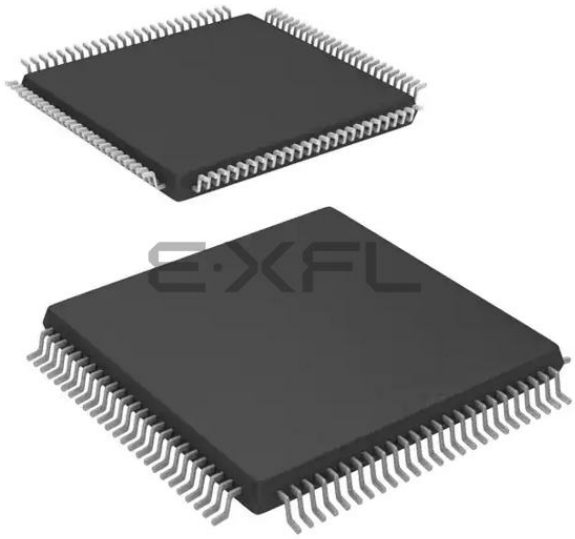

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface (LPC), I²C, IrDA, SCI, X-Bus
Peripherals	PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2148bvte10v

Item	Specifications
Bus controller	• 2-state or 3-state access space can be designated for external expansion areas • Number of program wait states can be set for external expansion areas
Data transfer controller (DTC) (H8S/2148 Group)	• Can be activated by internal interrupt or software • Multiple transfers or multiple types of transfer possible for one activation source • Transfer possible in repeat mode, block transfer mode, etc. • Request can be sent to CPU for interrupt that activated DTC
16-bit free-running timer module (FRT: 1 channel)	• One 16-bit free-running counter (also usable for external event counting) • Two output compare outputs • Four input capture inputs (with buffer operation capability)
8-bit timer module (2 channels: TMR0, TMR1)	Each channel has: • One 8-bit up-counter (also usable for external event counting) • Two timer constant registers • The two channels can be connected
Timer connection and 8-bit timer module (TMR) (2 channels: TMRX, TMRY) (Timer connection and TMRX provided in H8S/2148 Group)	Input/output and FRT, TMR1, TMRX, TMRY can be interconnected • Measurement of input signal or frequency-divided waveform pulse width and cycle (FRT, TMR1) • Output of waveform obtained by modification of input signal edge (FRT, TMR1) • Determination of input signal duty cycle (TMRX) • Output of waveform synchronized with input signal (FRT, TMRX, TMRY) • Automatic generation of cyclical waveform (FRT, TMRY)
Watchdog timer module (WDT: 2 channels)	• Watchdog timer or interval timer function selectable • Subclock operation capability (channel 1 only)
8-bit PWM timer (PWM) (H8S/2148 Group and H8S/2147N)	• Up to 16 outputs • Pulse duty cycle settable from 0 to 100% • Resolution: 1/256 • 1.25 MHz maximum carrier frequency (20-MHz operation)

Function	Instruction	Addressing Modes													
		#xx	Rn	@ERn	@(d:16,ERn)	@(d:32, ERn)	@–ERn/@ERn+	@aa:8	@aa:16	@aa:24	@aa:32	@(d:8, PC)	@(d:16, PC)	@@aa:8	|
System control	TRAPA	—	—	—	—	—	—	—	—	—	—	—	—	—	○
	RTE	—	—	—	—	—	—	—	—	—	—	—	—	—	○
	SLEEP	—	—	—	—	—	—	—	—	—	—	—	—	—	○
	LDC	B	B	W	W	W	W	—	W	—	W	—	—	—	—
	STC	—	B	W	W	W	W	—	W	—	W	—	—	—	—
	ANDC, ORC, XORC	B	—	—	—	—	—	—	—	—	—	—	—	—	—
	NOP	—	—	—	—	—	—	—	—	—	—	—	—	—	○
Block data transfer		—	—	—	—	—	—	—	—	—	—	—	—	—	BW

Legend:

B: Byte

W: Word

L: Longword

Notes: 1. Cannot be used in this LSI.

2. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.

3. Only registers ER0 to ER6 should be used when using the STM/LDM instruction.

5.2.6 Keyboard Matrix Interrupt Mask Register (KMIMR)

Bit	7	6	5	4	3	2	1	0
	KMIMR7	KMIMR6	KMIMR5	KMIMR4	KMIMR3	KMIMR2	KMIMR1	KMIMR0
Initial value	1	0	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

KMIMR is an 8-bit readable/writable register that performs mask control for the keyboard matrix interrupt inputs (pins $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$). To enable key-sense input interrupts from multiple pin inputs in keyboard matrix scanning/sensing, clear the corresponding mask bits to 0.

KMIMR is initialized to H'BF by a reset and in hardware standby mode and only $\overline{\text{IRQ6}}$ ($\overline{\text{KIN6}}$) input is enabled.

Bits 7 to 0—Keyboard Matrix Interrupt Mask (KMIMR7 to KMIMR0): These bits control key-sense input interrupt requests (KIN7 to KIN0).

Bits 7 to 0 KMIMR7 to KMIMR0	Description
0	Key-sense input interrupt requests enabled
1	Key-sense input interrupt requests disabled (Initial value)*

Note: * However, the initial value of KMIMR6 is 0 because the KMIMR6 bit controls both $\overline{\text{IRQ6}}$ interrupt request masking and key-sense input enabling.

5.2.7 Keyboard Matrix Interrupt Mask Register (KMIMRA)

Bit	7	6	5	4	3	2	1	0
	KMIMR15	KMIMR14	KMIMR13	KMIMR12	KMIMR11	KMIMR10	KMIMR9	KMIMR8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

KMIMRA is an 8-bit readable/writable register that performs mask control for the keyboard matrix interrupt inputs (pins $\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$). To enable key-sense input interrupts from multiple pin inputs in keyboard matrix scanning/sensing, clear the corresponding mask bits to 0.

KMIMRA is initialized to H'FF by a reset and in hardware standby mode.

5.5.4 Interrupt Exception Handling Sequence

Figure 5.11 shows the interrupt exception handling sequence. The example shown is for the case where interrupt control mode 0 is set in advanced mode, and the program area and stack area are in on-chip memory.

8.4.2 Register Configuration

Table 8.8 shows the port 3 register configuration.

Table 8.8 Port 3 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 3 data direction register	P3DDR	W	H'00	H'FFB4
Port 3 data register	P3DR	R/W	H'00	H'FFB6
Port 3 MOS pull-up control register	P3PCR	R/W	H'00	H'FFAE

Note: * Lower 16 bits of the address.

Port 3 Data Direction Register (P3DDR)

Bit	7	6	5	4	3	2	1	0
	P37DDR	P36DDR	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P3DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 3. P3DDR cannot be read; if it is, an undefined value will be returned.

P3DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 1, 2, and 3 (EXPE = 1)

  The input/output direction specified by P3DDR is ignored, and pins automatically function as data I/O pins.

  After a reset, and in hardware standby mode or software standby mode, the data I/O pins go to the high-impedance state.

- Modes 2 and 3 (EXPE = 0)

  The corresponding port 3 pins are output ports when P3DDR bits are set to 1, and input ports when cleared to 0.

8.11.2 Register Configuration

Table 8.22 summarizes the port A registers.

Table 8.22 Port A Registers

Name	Abbreviation	R/W	Initial Value	Address*1
Port A data direction register	PADDR	W	H'00	H'FFAB*2
Port A output data register	PAODR	R/W	H'00	H'FFAA
Port A input data register	PAPIN	R	Undefined	H'FFAB*2

Notes: 1. Lower 16 bits of the address.
2. PADDR and PAPIN have the same address.

Port A Data Direction Register (PADDR)

Bit	7	6	5	4	3	2	1	0
	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PADDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port A.

Setting a PADDR bit to 1 makes the corresponding port A pin an output pin, while clearing the bit to 0 makes the pin an input pin.

PADDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port A Output Data Register (PAODR)

Bit	7	6	5	4	3	2	1	0
	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PAODR is an 8-bit readable/writable register that stores output data for the port A pins (PA7 to PA0). PAODR can always be read or written to, regardless of the contents of PADDR.

9.1.3 Pin Configuration

Table 9.1 shows the PWM output pin.

Table 9.1 Pin Configuration

Name	Abbreviation	I/O	Function
PWM output pin 0 to 15	PW0 to PW15	Output	PWM timer pulse output 0 to 15

9.1.4 Register Configuration

Table 9.2 lists the registers of the PWM timer module.

Table 9.2 PWM Timer Module Registers

Name	Abbreviation	R/W	Initial Value	Address*1
PWM register select	PWSL	R/W	H'20	H'FFD6
PWM data registers 0 to 15	PWDR0 to PWDR15	R/W	H'00	H'FFD7
PWM data polarity register A	PWDPRA	R/W	H'00	H'FFD5
PWM data polarity register B	PWDPRB	R/W	H'00	H'FFD4
PWM output enable register A	PWOERA	R/W	H'00	H'FFD3
PWM output enable register B	PWOERB	R/W	H'00	H'FFD2
Port 1 data direction register	P1DDR	W	H'00	H'FFB0
Port 2 data direction register	P2DDR	W	H'00	H'FFB1
Port 1 data register	P1DR	R/W	H'00	H'FFB2
Port 2 data register	P2DR	R/W	H'00	H'FFB3
Peripheral clock select register	PCSR	R/W	H'00	H'FF82*2
Module stop control register	MSTPCRH	R/W	H'3F	H'FF86
	MSTPCRL	R/W	H'FF	H'FF87

Note: 1. Lower 16 bits of the address.
2. Some registers in the 8-bit timer are assigned in the addresses as other registers. In this case, register selection is performed by the FLSHE bit in the serial timer control register (STCR).

14.5.3 Switching between Watchdog Timer Mode and Interval Timer Mode

If the mode is switched from watchdog timer to interval timer, or vice versa, while the WDT is operating, errors could occur in the incrementation. Software must stop the watchdog timer (by clearing the TME bit to 0) before switching the mode.

14.5.4 System Reset by $\overline{\text{RESO}}$ Signal

If the $\overline{\text{RESO}}$ output signal is input to the chip's $\overline{\text{RES}}$ pin, the chip will not be initialized correctly. Ensure that the $\overline{\text{RESO}}$ signal is not logically input to the chip's $\overline{\text{RES}}$ pin. When resetting the entire system with the $\overline{\text{RESO}}$ signal, use a circuit such as that shown in figure 14.8.

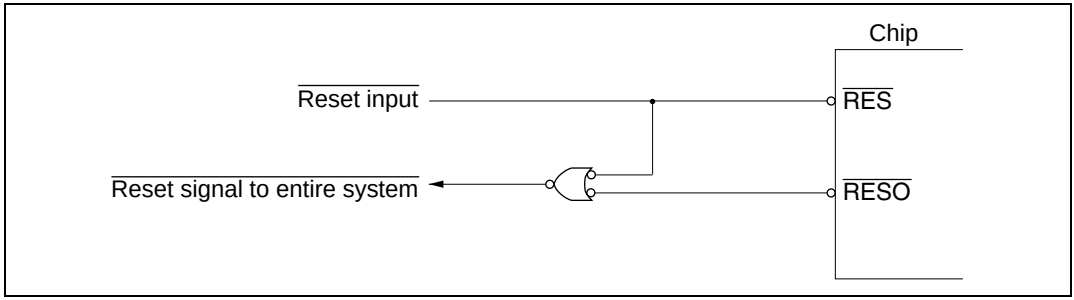

Figure 14.8 Sample Circuit for System Reset by $\overline{\text{RESO}}$ Signal

14.5.5 Counter Value in Transitions between High-Speed Mode, Subactive Mode, and Watch Mode

If the mode is switched between high-speed mode and subactive mode or between high-speed mode and watch mode when WDT1 is used as a realtime clock counter, an error will occur in the counter value when the internal clock is switched.

When the mode is switched from high-speed mode to subactive mode or watch mode, the increment timing is delayed by approximately 2 or 3 clock cycles when the WDT1 control clock is switched from the main clock to the subclock.

Also, since the main clock oscillator is halted during subclock operation, when the mode is switched from watch mode or subactive mode to high-speed mode, the clock is not supplied until internal oscillation stabilizes. As a result, after oscillation is started, counter incrementing is halted during the oscillation stabilization time set by bits STS2 to STS0 in SBYCR, and there is a corresponding discrepancy in the counter value.

Break Detection and Processing

When a framing error (FER) is detected, a break can be detected by reading the RxD pin value directly. In a break, the input from the RxD pin becomes all 0s, and so the FER flag is set, and the parity error flag (PER) may also be set.

Note that, since the SCI continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

Sending a Break

The TxD pin has a dual function as an I/O port whose direction (input or output) is determined by DR and DDR. This feature can be used to send a break.

Between serial transmission initialization and setting of the TE bit to 1, the mark state is replaced by the value of DR (the pin does not function as the TxD pin until the TE bit is set to 1). Consequently, DDR and DR for the port corresponding to the TxD pin should first be set to 1.

To send a break during serial transmission, first clear DR to 0, then clear the TE bit to 0.

When the TE bit is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TxD pin becomes an I/O port, and 0 is output from the TxD pin.

Receive Error Flags and Transmit Operations (Synchronous Mode Only)

Transmission cannot be started when a receive error flag (ORER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission.

Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times the transfer rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the base clock. This is illustrated in figure 15.23.

Section 16 I²C Bus Interface [Option]

A two-channel I²C bus interface is available as an option in the H8S/2148 Group and H8S/2147N. The I²C bus interface is not available for the H8S/2144 Group. Observe the following notes when using this option.

1. For mask-ROM versions, a W is added to the part number in products in which this optional function is used.

   Examples: HD6432147SWFA

2. The product number is identical for F-ZTAT versions. However, be sure to inform your Renesas sales representative if you will be using this option.

16.1 Overview

A two-channel I²C bus interface is available for the H8S/2148 Group and H8S/2147N as an option. The I²C bus interface conforms to and provides a subset of the Philips I²C bus (inter-IC bus) interface functions. The register configuration that controls the I²C bus differs partly from the Philips configuration, however.

Each I²C bus interface channel uses only one data line (SDA) and one clock line (SCL) to transfer data, saving board and connector space.

16.1.1 Features

- Selection of addressing format or non-addressing format
  - — I²C bus format: addressing format with acknowledge bit, for master/slave operation
  - — Serial format: non-addressing format without acknowledge bit, for master operation only
- Conforms to Philips I²C bus interface (I²C bus format)
- Two ways of setting slave address (I²C bus format)
- Start and stop conditions generated automatically in master mode (I²C bus format)
- Selection of acknowledge output levels when receiving (I²C bus format)
- Automatic loading of acknowledge bit when transmitting (I²C bus format)
- Wait function in master mode (I²C bus format)

  A wait can be inserted by driving the SCL pin low after data transfer, excluding acknowledgement. The wait can be cleared by clearing the interrupt flag.

- Wait function in slave mode (I²C bus format)

  A wait request can be generated by driving the SCL pin low after data transfer, excluding acknowledgement. The wait request is cleared when the next transfer becomes possible.
- Three interrupt sources
  - Data transfer end (including transmission mode transition with I²C bus format and address reception after loss of master arbitration)
  - Address match: when any slave address matches or the general call address is received in slave receive mode (I²C bus format)
  - Stop condition detection
- Selection of 16 internal clocks (in master mode)
- Direct bus drive (with SCL and SDA pins)
  - Two pins—P52/SCL0 and P97/SDA0—(normally NMOS push-pull outputs) function as NMOS open-drain outputs when the bus drive function is selected.
  - Two pins—P86/SCL1 and P42/SDA1—(normally CMOS pins) function as NMOS-only outputs when the bus drive function is selected.
- Automatic switching from formatless mode to I²C bus format (channel 0 only)
  - Formatless operation (no start/stop conditions, non-addressing mode) in slave mode
  - Operation using a common data pin (SDA) and independent clock pins (VSYNCI, SCL)
  - Automatic switching from formatless mode to I²C bus format on the fall of the SCL pin

16.1.2 Block Diagram

Figure 16.1 shows a block diagram of the I²C bus interface.

Figure 16.2 shows an example of I/O pin connections to external circuits. Channel 0 I/O pins and channel 1 I/O pins differ in structure, and have different specifications for permissible applied voltages. For details, see section 26, Electrical Characteristics.

19.2 Register Descriptions

19.2.1 D/A Data Registers 0 and 1 (DADR0, DADR1)

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D/A data registers 0 and 1 (DADR0 and DADR1) are 8-bit readable/writable registers that store data to be converted. When analog output is enabled, the value in the D/A data register is converted and output continuously at the analog output pin.

The D/A data registers are initialized to H'00 by a reset and in hardware standby mode.

19.2.2 D/A Control Register (DACR)

Bit	7	6	5	4	3	2	1	0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/W	R/W	R/W	—	—	—	—	—

DACR is an 8-bit readable/writable register that controls the operation of the D/A converter module.

DACR is initialized to H'1F by a reset and in hardware standby mode.

Bit 7—D/A Output Enable 1 (DAOE1): Controls D/A conversion and analog output.

Bit 7

DAOE1	Description	
0	Analog output DA1 is disabled	(Initial value)
1	D/A conversion is enabled on channel 1. Analog output DA1 is enabled	

Bit 7—A/D End Flag (ADF): Status flag that indicates the end of A/D conversion.

Bit 7

ADF	Description	
0	[Clearing conditions]	(Initial value)
	• When 0 is written in the ADF flag after reading ADF = 1	
	• When the DTC is activated by an ADI interrupt and ADDR is read	
1	[Setting conditions]	
	• Single mode: When A/D conversion ends	
	• Scan mode: When A/D conversion ends on all specified channels	

Bit 6—A/D Interrupt Enable (ADIE): Selects enabling or disabling of interrupt (ADI) requests at the end of A/D conversion.

Bit 6

ADIE	Description	
0	A/D conversion end interrupt (ADI) request is disabled	(Initial value)
1	A/D conversion end interrupt (ADI) request is enabled	

Bit 5—A/D Start (ADST): Selects starting or stopping of A/D conversion. Holds a value of 1 during A/D conversion.

The ADST bit can be set to 1 by software, a timer conversion start trigger, or the A/D external trigger input pin ($\overline{\text{ADTRG}}$).

Bit 5

ADST	Description	
0	A/D conversion stopped	(Initial value)
1	Single mode: A/D conversion is started. Cleared to 0 automatically when conversion on the specified channel ends	
	Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode	

Bit 4—Scan Mode (SCAN): Selects single mode or scan mode as the A/D conversion operating mode. See section 20.4, Operation, for single mode and scan mode operation. Only set the SCAN bit while conversion is stopped.

Section 21 RAM

21.1 Overview

The H8S/2148, H8S/2144, and H8S/2143 have 4 kbytes of on-chip high-speed static RAM, and the H8S/2147, H8S/2147N, and H8S/2142 have 2 kbytes. The on-chip RAM is connected to the CPU by a 16-bit data bus, enabling both byte data and word data to be accessed in one state. This makes it possible to perform fast word data transfer.

The on-chip RAM can be enabled or disabled by means of the RAM enable bit (RAME) in the system control register (SYSCR).

21.1.1 Block Diagram

Figure 21.1 shows a block diagram of the on-chip RAM.

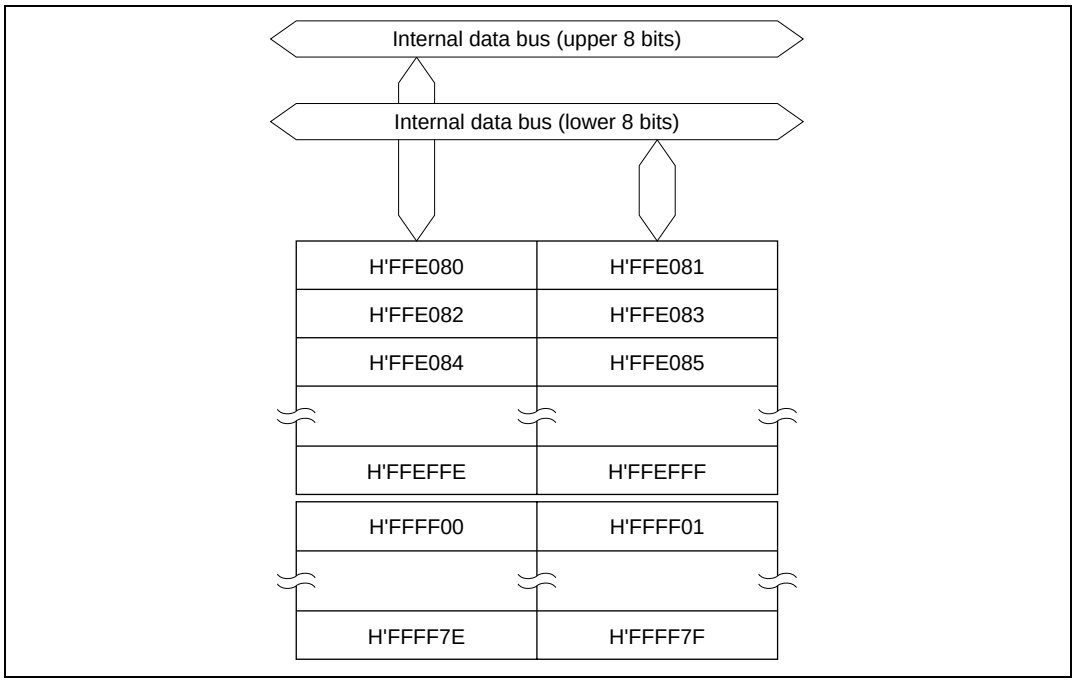

Figure 21.1 Block Diagram of RAM (H8S/2148, H8S/2144, H8S/2143)

Notes on Use of Auto-Erase-Program Mode

- Auto-erase mode supports only entire memory erasing.
- Do not perform a command write during auto-erasing.
- Confirm normal end of auto-erasing by checking FO6. Alternatively, status read mode can also be used for this purpose (FO7 status polling uses the auto-erase operation end identification pin).
- The status polling FO6 and FO7 pin information is retained until the next command write. Until the next command write is performed, reading is possible by enabling $\overline{CE}$ and $\overline{OE}$.

23.10.7 Status Read Mode

- Status read mode is used to identify what type of abnormal end has occurred. Use this mode when an abnormal end occurs in auto-program mode or auto-erase mode.
- The return code is retained until a command write for other than status read mode is performed.

Table 23.18 AC Characteristics in Status Read Mode

Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, T_a = 25°C ±5°C

Item	Symbol	Min	Max	Unit
Command write cycle	t_{nxtc}	20	—	µs
$\overline{CE}$ hold time	t_{ceh}	0	—	ns
$\overline{CE}$ setup time	t_{ces}	0	—	ns
Data hold time	t_{dh}	50	—	ns
Data setup time	t_{ds}	50	—	ns
Write pulse width	t_{wep}	70	—	ns
$\overline{OE}$ output delay time	t_{oe}	—	150	ns
Disable delay time	t_{df}	—	100	ns
$\overline{CE}$ output delay time	t_{ce}	—	150	ns
$\overline{WE}$ rise time	t_r	—	30	ns
$\overline{WE}$ fall time	t_f	—	30	ns

Table 25.4 MSTP Bits and Corresponding On-Chip Supporting Modules

Register	Bit	Module
MSTPCRH	MSTP15	—
	MSTP14*	Data transfer controller (DTC)
	MSTP13	16-bit free-running timer (FRT)
	MSTP12	8-bit timer (TMR0, TMR1)
	MSTP11	8-bit PWM timer (PWM), 14-bit PWM timer (PWMX)
	MSTP10	D/A converter
	MSTP9	A/D converter
	MSTP8	8-bit timers (TMRX, TMRY), timer connection
MSTPCRL	MSTP7	Serial communication interface 0 (SCI0)
	MSTP6	Serial communication interface 1 (SCI1)
	MSTP5	Serial communication interface 2 (SCI2)
	MSTP4*	I^2C bus interface (IIC) channel 0 (option)
	MSTP3*	I^2C bus interface (IIC) channel 1 (option)
	MSTP2	Host interface (HIF), keyboard matrix interrupt mask register (KMIMR, KMIMRA), port 6 MOS pull-up control register (KMPCR), keyboard buffer controller (PS2)
	MSTP1*	—
	MSTP0*	—

Notes: Do not set bit 15 to 1. Bits 1 and 0 can be read or written to, but do not affect operation.

* Must be set to 1 in the H8S/2144 Group and H8S/2147N.

25.5.2 Usage Note

If there is conflict between DTC module stop mode setting and a DTC bus request, the bus request has priority and the MSTP bit will not be set to 1.

Write 1 to the MSTP bit again after the DTC bus cycle.

When using the H8S/2144 Group and H8S/2147N, the MSTP bits for nonexistent modules must be set to 1.

IDR3—Input Data Register 3 **H'FE84** **HIF**
IDR4—Input Data Register 4 **H'FE8C** **HIF**

Bit	7	6	5	4	3	2	1	0
	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
Initial value	—	—	—	—	—	—	—	—
Slave R/W	R	R	R	R	R	R	R	R
Host R/W	W	W	W	W	W	W	W	W

Stores host data bus contents at rise of $\overline{IOW}$ when $\overline{CS}$ is low

ODR3—Output Data Register 3 **H'FE85** **HIF**
ODR4—Output Data Register 4 **H'FE8D** **HIF**

Bit	7	6	5	4	3	2	1	0
	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
Initial value	—	—	—	—	—	—	—	—
Slave R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Host R/W	R	R	R	R	R	R	R	R

ODR contents are output to the host data bus
when HA0 is low, $\overline{CS}$ is low, and $\overline{IOR}$ is low

ICDR1—I²C Bus Data Register 1 **H'FF8E** **IIC1**
ICDR0—I²C Bus Data Register 0 **H'FFDE** **IIC0**

Bit	7	6	5	4	3	2	1	0
	ICDR7	ICDR6	ICDR5	ICDR4	ICDR3	ICDR2	ICDR1	ICDR0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ICDRR

Bit	7	6	5	4	3	2	1	0
	ICDRR7	ICDRR6	ICDRR5	ICDRR4	ICDRR3	ICDRR2	ICDRR1	ICDRR0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

ICDRS

Bit	7	6	5	4	3	2	1	0
	ICDRS7	ICDRS6	ICDRS5	ICDRS4	ICDRS3	ICDRS2	ICDRS1	ICDRS0
Initial value	—	—	—	—	—	—	—	—
Read/Write	—	—	—	—	—	—	—	—

ICDRT

Bit	7	6	5	4	3	2	1	0
	ICDRT7	ICDRT6	ICDRT5	ICDRT4	ICDRT3	ICDRT2	ICDRT1	ICDRT0
Initial value	—	—	—	—	—	—	—	—
Read/Write	W	W	W	W	W	W	W	W

TDRE, RDRF (internal flags)

Bit							—	—
							TDRE	RDRF
Initial value							0	0
Read/Write							—	—

Note: For details, see section 16.2.1, I²C Bus Data Register (ICDR).

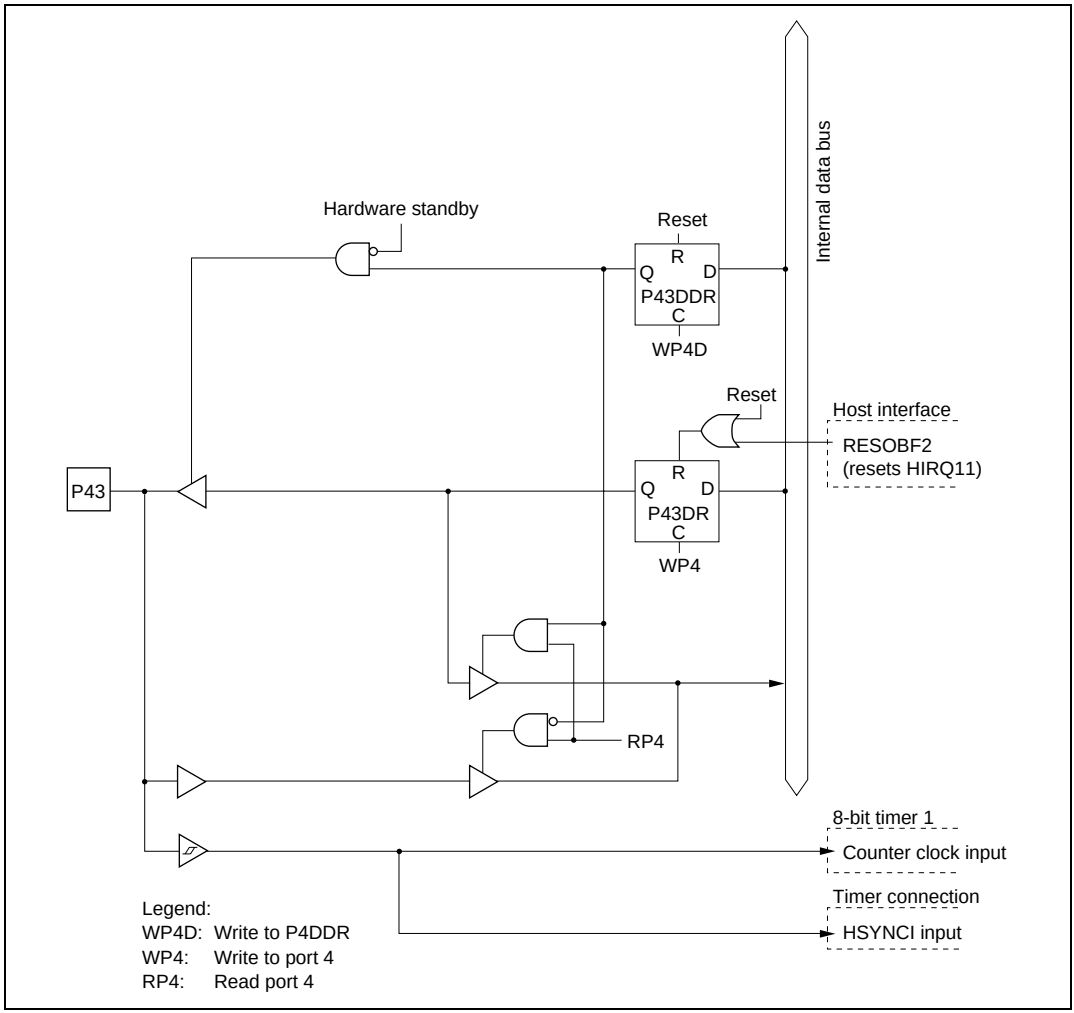

Figure C.9 Port 4 Block Diagram (Pin P43)

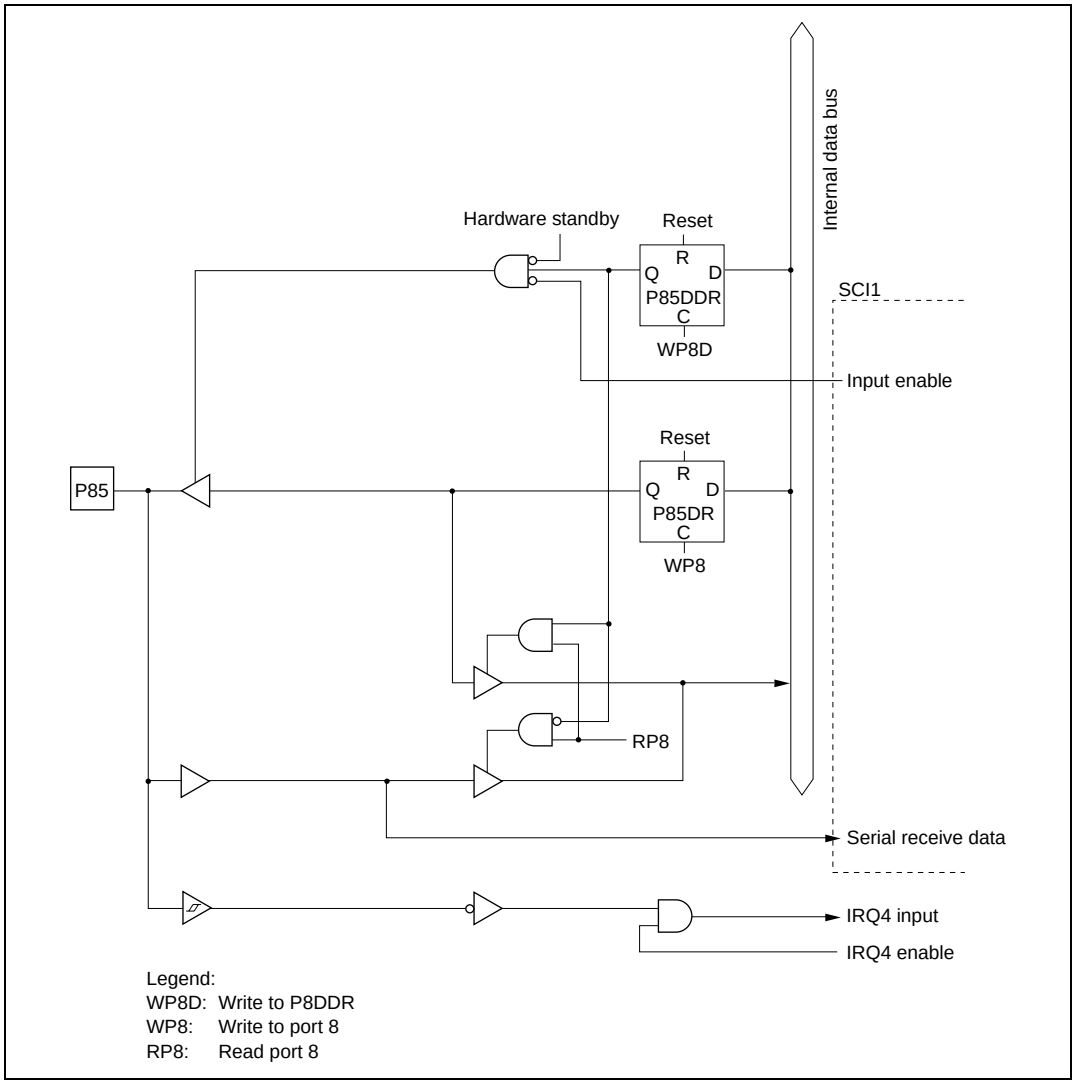

Figure C.27 Port 8 Block Diagram (Pin P85)