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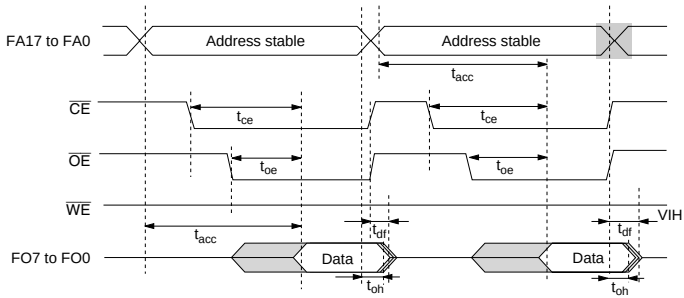
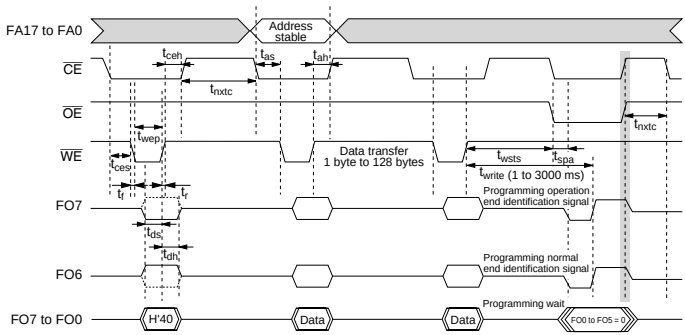
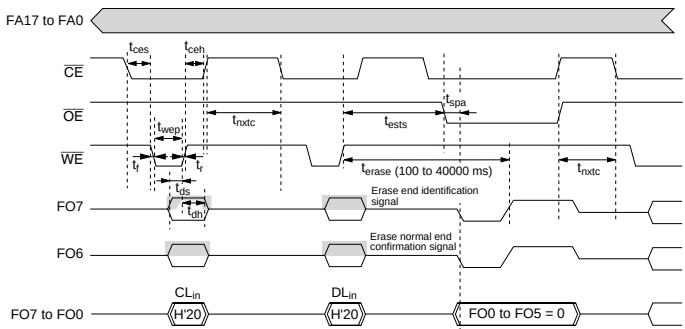
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2148rte20iv

Item	Page	Revision (See Manual for Details)
23.10.4 Memory Read Mode Figure 23.19 Timing Waveforms for $\overline{CE}$/$\overline{OE}$ Clocked Read	722	Figure 23.19 amended 
23.10.5 Auto-Program Mode Figure 23.20 Auto-Program Mode Timing Waveforms	724	Figure 23.20 amended 
23.10.6 Auto-Erase Mode Figure 23.21 Auto-Erase Mode Timing Waveforms	725	Figure 23.21 amended 

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Bits 2 to 0—Clock Select 2 to 0 (CKS2 to CKS0): These bits select whether the clock input to TCNT is an internal or external clock.

The input clock can be selected from either six or three clocks, all divided from the system clock (ϕ). The falling edge of the selected internal clock triggers the count.

When use of an external clock is selected, three types of count can be selected: at the rising edge, the falling edge, and both rising and falling edges.

Some functions differ between channel 0 and channel 1, because of the cascading function.

	TCR			STCR		
	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0	
Channel	CKS2	CKS1	CKS0	ICKS1	ICKS0	Description
0	0	0	0	—	—	Clock input disabled (Initial value)
	0	0	1	—	0	ϕ/8 internal clock source, counted on the falling edge
	0	0	1	—	1	ϕ/2 internal clock source, counted on the falling edge
	0	1	0	—	0	ϕ/64 internal clock source, counted on the falling edge
	0	1	0	—	1	ϕ/32 internal clock source, counted on the falling edge
	0	1	1	—	0	ϕ/1024 internal clock source, counted on the falling edge
	0	1	1	—	1	ϕ/256 internal clock source, counted on the falling edge
	1	0	0	—	—	Counted on TCNT1 overflow signal*
1	0	0	0	—	—	Clock input disabled (Initial value)
	0	0	1	0	—	ϕ/8 internal clock source, counted on the falling edge
	0	0	1	1	—	ϕ/2 internal clock source, counted on the falling edge
	0	1	0	0	—	ϕ/64 internal clock source, counted on the falling edge
	0	1	0	1	—	ϕ/128 internal clock source, counted on the falling edge
	0	1	1	0	—	ϕ/1024 internal clock source, counted on the falling edge
	0	1	1	1	—	ϕ/2048 internal clock source, counted on the falling edge
	1	0	0	—	—	Counted on TCNT0 compare-match A*

Table 12.6 TMRY 8-Bit Timer Interrupt Sources

Interrupt source	Description	DTC Activation	Interrupt Priority
CMIA	Requested by CMFA	Possible	High
CMIB	Requested by CMFB	Possible	↑
OVI	Requested by OVF	Not possible	Low

12.5 8-Bit Timer Application Example

In the example below, the 8-bit timer is used to generate a pulse output with a selected duty cycle, as shown in figure 12.12. The control bits are set as follows:

- In TCR, CCLR1 is cleared to 0 and CCLR0 is set to 1 so that the timer counter is cleared by a TCORA compare-match.
- In TCSR, bits OS3 to OS0 are set to B'0110, causing 1 output at a TCORA compare-match and 0 output at a TCORB compare-match.

With these settings, the 8-bit timer provides output of pulses at a rate determined by TCORA with a pulse width determined by TCORB. No software intervention is required.

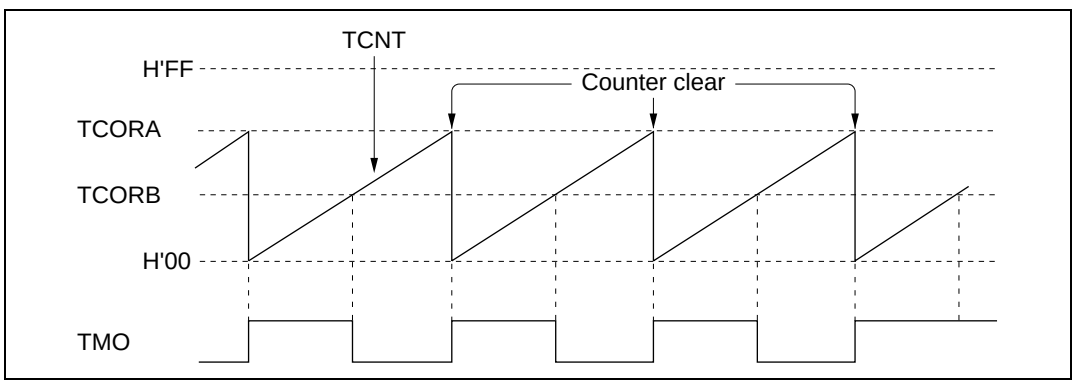


Figure 12.12 Pulse Output (Example)

Bit 3—Stop Bit Length (STOP): Selects 1 or 2 bits as the stop bit length in asynchronous mode. The STOP bit setting is only valid in asynchronous mode. If synchronous mode is set the STOP bit setting is invalid since stop bits are not added.

Bit 3

STOP	Description	
0	1 stop bit*1	(Initial value)
1	2 stop bits*2	

Notes: 1. In transmission, a single 1 bit (stop bit) is added to the end of a transmit character before it is sent.
2. In transmission, two 1 bits (stop bits) are added to the end of a transmit character before it is sent.

In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit; if it is 0, it is treated as the start bit of the next transmit character.

Bit 2—Multiprocessor Mode (MP): Selects multiprocessor format. When multiprocessor format is selected, the PE bit and O/$\overline{E}$ bit parity settings are invalid. The MP bit setting is only valid in asynchronous mode; it is invalid in synchronous mode.

For details of the multiprocessor communication function, see section 15.3.3, Multiprocessor Communication Function.

Bit 2

MP	Description	
0	Multiprocessor function disabled	(Initial value)
1	Multiprocessor format selected	

Bits 1 and 0—Clock Select 1 and 0 (CKS1, CKS0): These bits select the clock source for the baud rate generator. The clock source can be selected from ϕ, $\phi/4$, $\phi/16$, and $\phi/64$, according to the setting of bits CKS1 and CKS0.

For the relation between the clock source, the bit rate register setting, and the baud rate, see section 15.2.8, Bit Rate Register (BRR).

15.3 Operation

15.3.1 Overview

The SCI can carry out serial communication in two modes: asynchronous mode in which synchronization is achieved character by character, and synchronous mode in which synchronization is achieved with clock pulses.

Selection of asynchronous or synchronous mode and the transmission format is made using SMR as shown in table 15.8. The SCI clock is determined by a combination of the C/$\overline{A}$ bit in SMR and the CKE1 and CKE0 bits in SCR, as shown in table 15.9.

Asynchronous Mode:

- Data length: Choice of 7 or 8 bits
- Choice of parity addition, multiprocessor bit addition, and addition of 1 or 2 stop bits (the combination of these parameters determines the transfer format and character length)
- Detection of framing, parity, and overrun errors, and breaks, during reception
- Choice of internal or external clock as SCI clock source
  - When internal clock is selected:

    The SCI operates on the baud rate generator clock and a clock with the same frequency as the bit rate can be output
  - When external clock is selected:

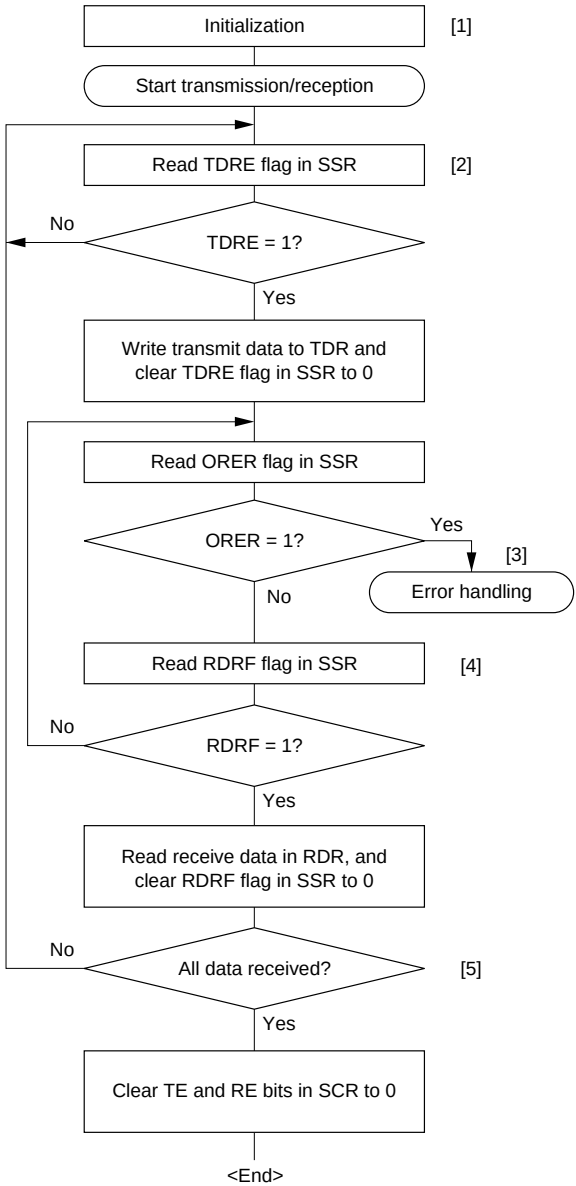
    A clock with a frequency of 16 times the bit rate must be input (the built-in baud rate generator is not used)

Synchronous Mode:

- Transfer format: Fixed 8-bit data
- Detection of overrun errors during reception
- Choice of internal or external clock as SCI clock source
  - When internal clock is selected:

    The SCI operates on the baud rate generator clock and a serial clock is output off-chip
  - When external clock is selected:

    The built-in baud rate generator is not used, and the SCI operates on the input serial clock



Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first clear the TE bit and RE bit to 0, then set both these bits to 1 simultaneously.

[1] SCI initialization:
The TxD pin is designated as the transmit data output pin, and the RxD pin is designated as the receive data input pin, enabling simultaneous transmit and receive operations.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.
Transition of the TDRE flag from 0 to 1 can also be identified by a TXI interrupt.

[3] Receive error handling:
If a receive error occurs, read the ORER flag in SSR , and after performing the appropriate error handling, clear the ORER flag to 0. Transmission/reception cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission/ reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR and clear the TDRE flag to 0.
Checking and clearing of the TDRE flag is automatic when the DTC is activated by a transmit-data-empty interrupt (TXI) request and data is written to TDR. Also, the RDRF flag is cleared automatically when the DTC is activated by a receive-data-full interrupt (RXI) request and the RDR value is read.

Figure 15.20 Sample Flowchart of Simultaneous Serial Transmit and Receive Operations

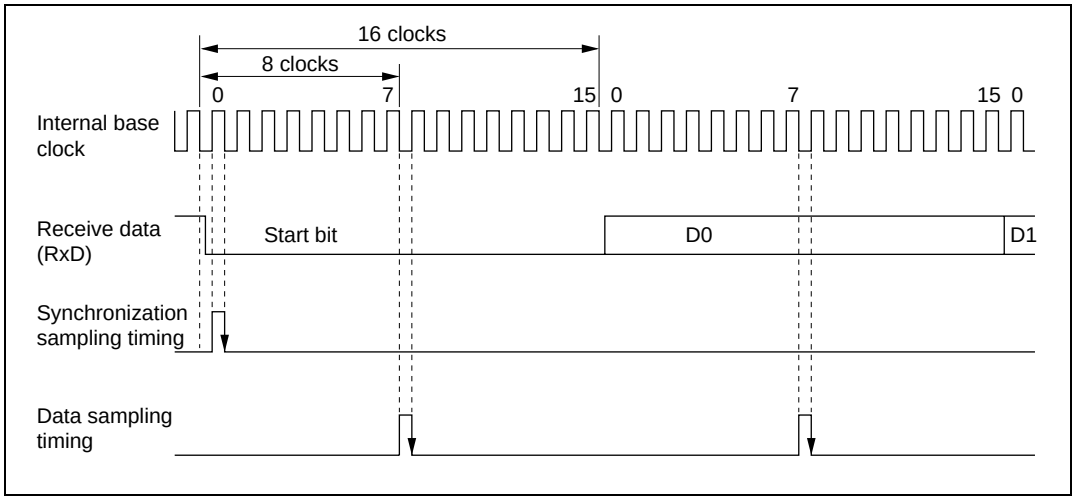


Figure 15.23 Receive Data Sampling Timing in Asynchronous Mode

Thus the receive margin in asynchronous mode is given by equation (1) below.

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\% \quad \text{..... (1)}$$

Where M: Receive margin (%)
N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute value of clock rate deviation

Assuming values of F = 0 and D = 0.5 in equation (1), a receive margin of 46.875% is given by equation (2) below.

When D = 0.5 and F = 0,

$$M = \left(0.5 - \frac{1}{2 \times 16}\right) \times 100\%$$
$$= 46.875\% \quad \text{..... (2)}$$

However, this is only a theoretical value, and a margin of 20% to 30% should be allowed in system design.

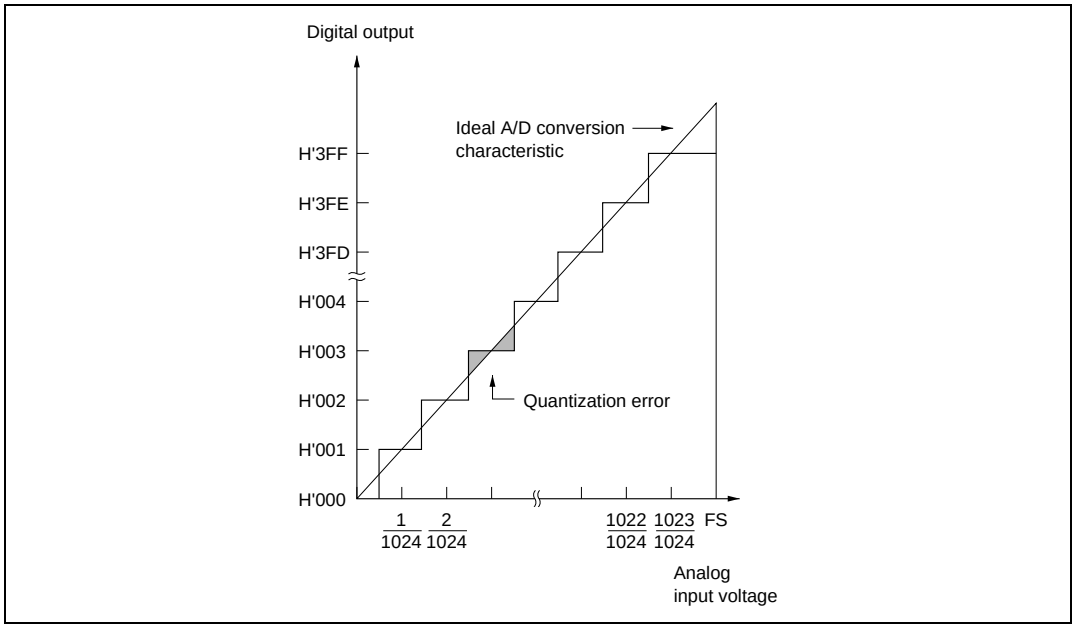


Figure 20.9 A/D Conversion Precision Definitions (1)

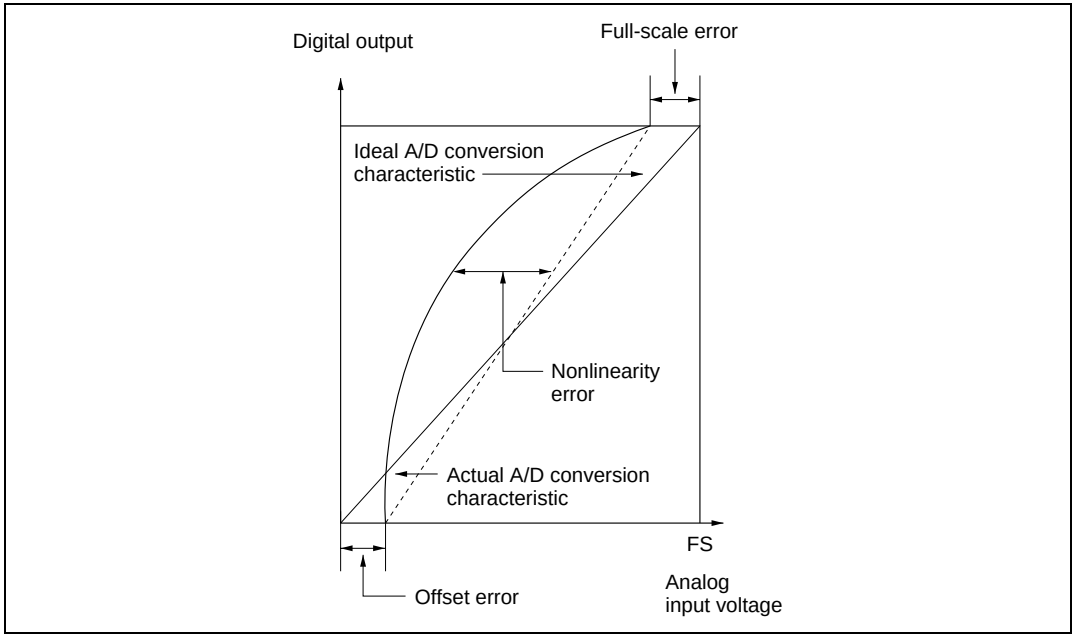
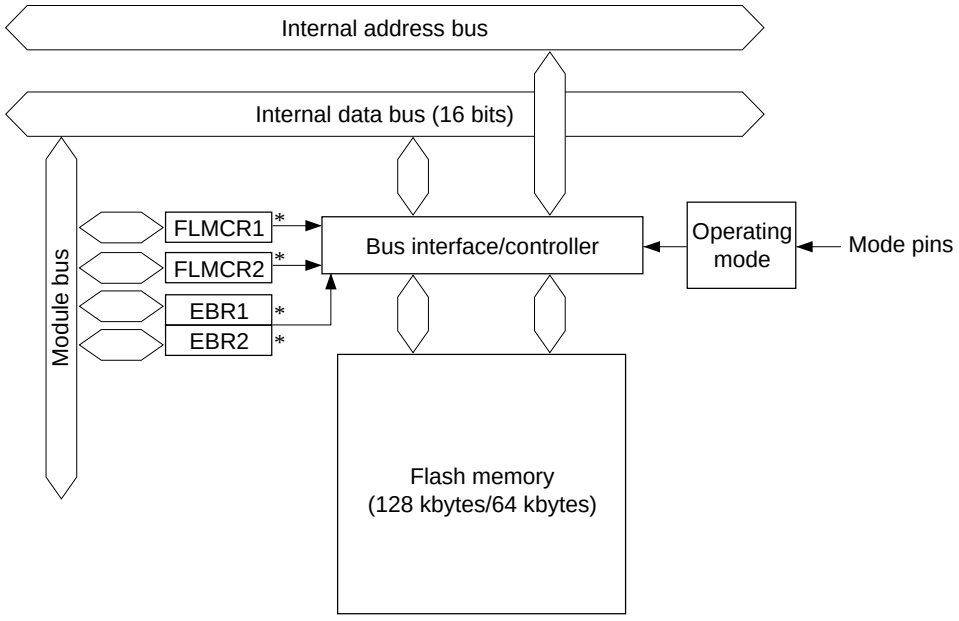


Figure 20.10 A/D Conversion Precision Definitions (2)

22.4.2 Block Diagram



Legend:
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2

Note: * These registers are used only in the flash memory version. In the mask ROM version, a read at any of these addresses will return an undefined value, and writes are invalid.

Figure 22.2 Block Diagram of Flash Memory

Bit 0—Program (P): Selects program mode transition or clearing. Do not set the SWE, PSU, ESU, EV, PV, or E bit at the same time.

Bit 0		
P	**Description**	
0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When SWE = 1, and PSU = 1	

23.5.2 Flash Memory Control Register 2 (FLMCR2)

Bit	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	ESU	PSU
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	—	—	—	—	—	R/W	R/W

FLMCR2 is an 8-bit register that monitors the presence or absence of flash memory program/erase protection (error protection) and performs setup for flash memory program/erase mode. FLMCR2 is initialized to H'00 by a reset, and in hardware standby mode. The ESU and PSU bits are cleared to 0 in software standby mode, subactive mode, subsleep mode, and watch mode.

When on-chip flash memory is disabled, a read will return H'00 and writes are invalid.

Bit 7—Flash Memory Error (FLER): Indicates that an error has occurred during an operation on flash memory (programming or erasing). When FLER is set to 1, flash memory goes to the error-protection state.

23.5.3 Erase Block Registers 1 and 2 (EBR1, EBR2)

Bit	7	6	5	4	3	2	1	0
EBR1	—	—	—	—	—	—	EB9/—*2	EB8/—*2
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	R/W*1 *2	R/W*1 *2

Bit	7	6	5	4	3	2	1	0
EBR2	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*1	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: 1. In normal mode, these bits cannot be modified and are always read as 0.
2. Bits EB8 and EB9 are not present in the 64-kbyte versions; they must not be set to 1.

EBR1 and EBR2 are registers that specify the flash memory erase area block by block; bits 1 and 0 in EBR1 and bits 7 to 0 in EBR2 are readable/writable bits. EBR1 and EBR2 are each initialized to H'00 by a reset, in hardware standby mode, software standby mode, subactive mode, subsleep mode, and watch mode, and when the SWE bit in FLMCR1 is not set. When a bit in EBR1 and EBR2 is set, the corresponding block can be erased. Other blocks are erase-protected. Set only one bit in EBR1 and EBR2 (more than one bit cannot be set). When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 23.5.

Bits 2 to 0—System Clock Select (SCK2 to SCK0): These bits select the clock for the bus master in high-speed mode and medium-speed mode. When operating the device after a transition to subactive mode or watch mode, bits SCK2 to SCK0 should all be cleared to 0.

Bit 2	Bit 1	Bit 0		
SCK2	**SCK1**	**SCK0**	**Description**	
0	0	0	Bus master is in high-speed mode	(Initial value)
		1	Medium-speed clock is ϕ/2	
	1	0	Medium-speed clock is ϕ/4	
		1	Medium-speed clock is ϕ/8	
1	0	0	Medium-speed clock is ϕ/16	
		1	Medium-speed clock is ϕ/32	
	1	—	—	

25.2.2 Low-Power Control Register (LPWRCR)

Bit	7	6	5	4	3	2	1	0
	DTON	LSON	NESEL	EXCLE	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

LPWRCR is an 8-bit readable/writable register that performs power-down mode control.

LPWRCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Direct-Transfer On Flag (DTON): Specifies whether a direct transition is made between high-speed mode, medium-speed mode, and subactive mode when making a power-down transition by executing a SLEEP instruction. The operating mode to which the transition is made after SLEEP instruction execution is determined by a combination of other control bits.

In order to retain on-chip RAM data, the RAME bit in SYSCR should be cleared to 0 before driving the $\overline{\text{STBY}}$ pin low.

Do not change the state of the mode pins (MD1 and MD0) while the chip is in hardware standby mode.

Hardware standby mode is cleared by means of the $\overline{\text{STBY}}$ pin and the $\overline{\text{RES}}$ pin. When the $\overline{\text{STBY}}$ pin is driven high while the $\overline{\text{RES}}$ pin is low, the reset state is set and clock oscillation is started. Ensure that the $\overline{\text{RES}}$ pin is held low until the clock oscillation settles (at least 8 ms—the oscillation settling time—when using a crystal oscillator). When the $\overline{\text{RES}}$ pin is subsequently driven high, a transition is made to the program execution state via the reset exception handling state.

25.7.2 Hardware Standby Mode Timing

Figure 25.4 shows an example of hardware standby mode timing.

When the $\overline{\text{STBY}}$ pin is driven low after the $\overline{\text{RES}}$ pin has been driven low, a transition is made to hardware standby mode. Hardware standby mode is cleared by driving the $\overline{\text{STBY}}$ pin high, waiting for the oscillation settling time, then changing the $\overline{\text{RES}}$ pin from low to high.

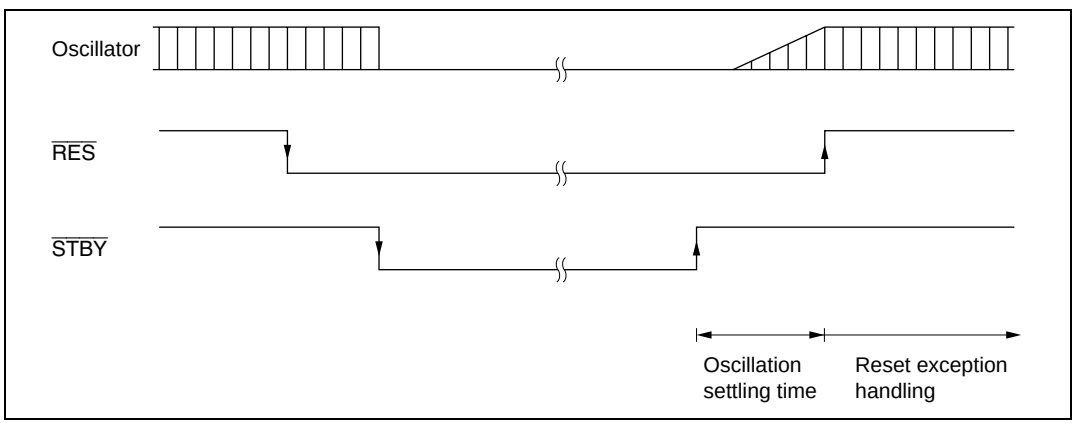


Figure 25.4 Hardware Standby Mode Timing

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	(4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI			—	—	50	pF	
	P52, P97, P42, P86 PA7 to PA2			—	—	20	pF	
	Input pins except (4) above			—	—	15	pF	
Current dissipation*9	Normal operation		I_{CC}	—	55	70	mA	f = 20 MHz
	Sleep mode			—	36	55	mA	f = 20 MHz
	Standby mode*10			—	1.0	5.0	µA	$T_a \leq 50°C$
				—	—	20.0	µA	$50°C < T_a$
Analog power supply current	During A/D, D/A conversion		AI_{CC}	—	1.2	2.0	mA	
	Idle			—	0.01	5.0	µA	AV_{CC}= 2.0 V to 5.5 V
Reference power supply current	During A/D conversion		AI_{ref}	—	0.5	1.0	mA	
	During A/D, D/A conversion			—	2.0	5.0	mA	
	Idle			—	0.01	5.0	µA	AV_{ref}= 2.0 V to AV_{CC}
Analog power supply voltage*1			AV_{CC}	4.5	—	5.5	V	Operating
				2.0	—	5.5	V	Idle/not used
RAM standby voltage			V_{RAM}	2.0	—	—	V	

Notes: 1. **Do not leave the AVCC, AV_{ref}, and AVSS pins open even if the A/D converter and D/A converter are not used.**

Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 5.5 V to AVCC and AV_{ref} pins by connection to the power supply (V_{CC}), or some other method. Ensure that $AV_{ref} \leq AV_{CC}$.

2. P67 to P60 include supporting module inputs multiplexed on those pins.
3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.
4. In the H8S/2148 Group, P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs.

   An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

   In the H8S/2148 Group, P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS.
5. When IICS = 0, ICE = 0, and KBIOE = 0. Low-level output when the bus drive function is selected is determined separately.

Table 26.57 DC Characteristics (2)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC}*1 = 4.0 V to 5.5 V, AV_{ref}*1 = 4.0 V to AV_{CC},
V_{SS} = AV_{SS}*1 = 0 V, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60*2*5, $\overline{KIN15}$ to $\overline{KIN8}$*5, $\overline{IRQ2}$ to $\overline{IRQ0}$*3, $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	V_{CC} = 4.5 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	0.4	—	—	V	
			V_T^-	0.8	—	—	V	V_{CC} < 4.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	0.3	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	V_{CC} –0.7	—	V_{CC} +0.3	V	
	EXTAL, PA7 to PA0*5			$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 7			2.0	—	AV_{CC} +0.3	V	
	Input pins except (1) and (2) above			2.0	—	V_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0	(3)	V_{IL}	–0.3	—	0.5	V	
	PA7 to PA0			–0.3	—	1.0	V	V_{CC} = 4.5 V to 5.5 V
				–0.3	—	0.8	V	V_{CC} < 4.5 V
	NMI, EXTAL, input pins except (1) and (3) above			–0.3	—	0.8	V	
Output high voltage	All output pins*4		V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
				3.5	—	—	V	I_{OH} = –1 mA, V_{CC} = 4.5 V to 5.5 V
				3.0	—	—	V	I_{OH} = –1 mA, V_{CC} < 4.5 V

(3) Bus Timing

Table 26.62 shows the bus timing. Operation in external expansion mode is not guaranteed when operating on the subclock (ϕ = 32.768 kHz).

Table 26.62 Bus Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

		Condition A		Condition B		Condition C			
		20 MHz		16 MHz		10 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Address delay time	t_{AD}	—	20	—	30	—	40	ns	Figure 26.10 to figure 26.14
Address setup time	t_{AS}	0.5 × t_{cyc} –15	—	0.5 × t_{cyc} –20	—	0.5 × t_{cyc} –30	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} –10	—	0.5 × t_{cyc} –15	—	0.5 × t_{cyc} –20	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	20	—	30	—	40	ns	
$\overline{AS}$ delay time	t_{ASD}	—	30	—	45	—	60	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	30	—	45	—	60	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	30	—	45	—	60	ns	
Read data setup time	t_{RDS}	15	—	20	—	35	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	0	—	ns	

C.4 Port 4 Block Diagrams

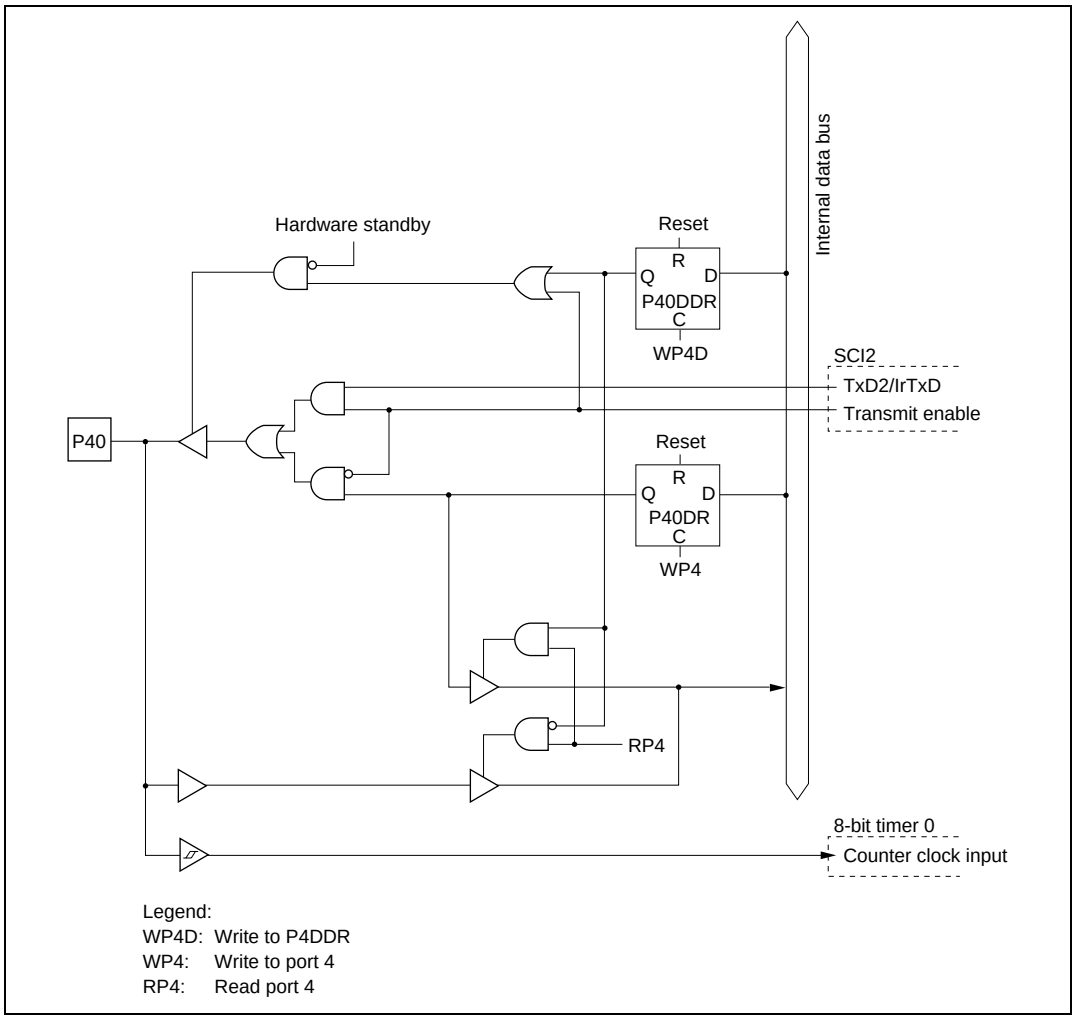


Figure C.6 Port 4 Block Diagram (Pin P40)

C.8 Port 8 Block Diagrams

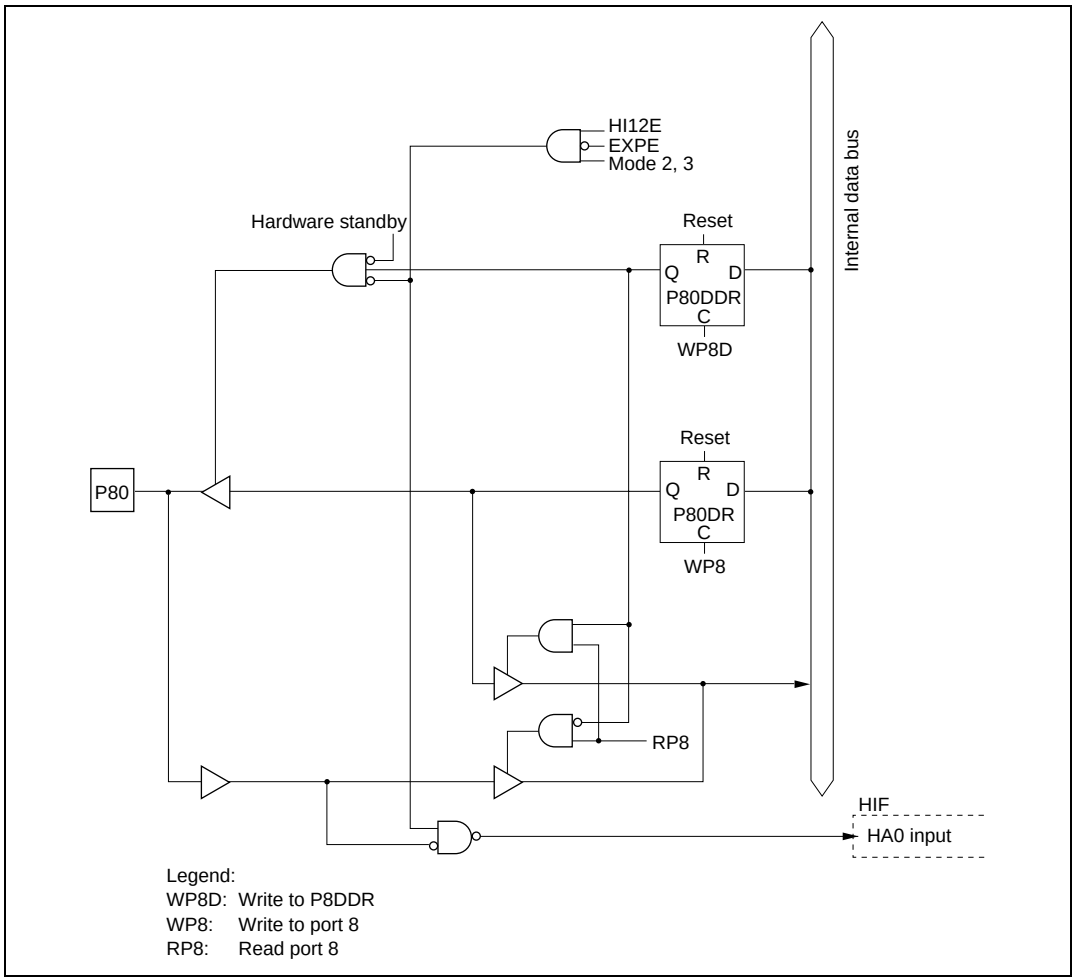


Figure C.23 Port 8 Block Diagram (Pin P80)

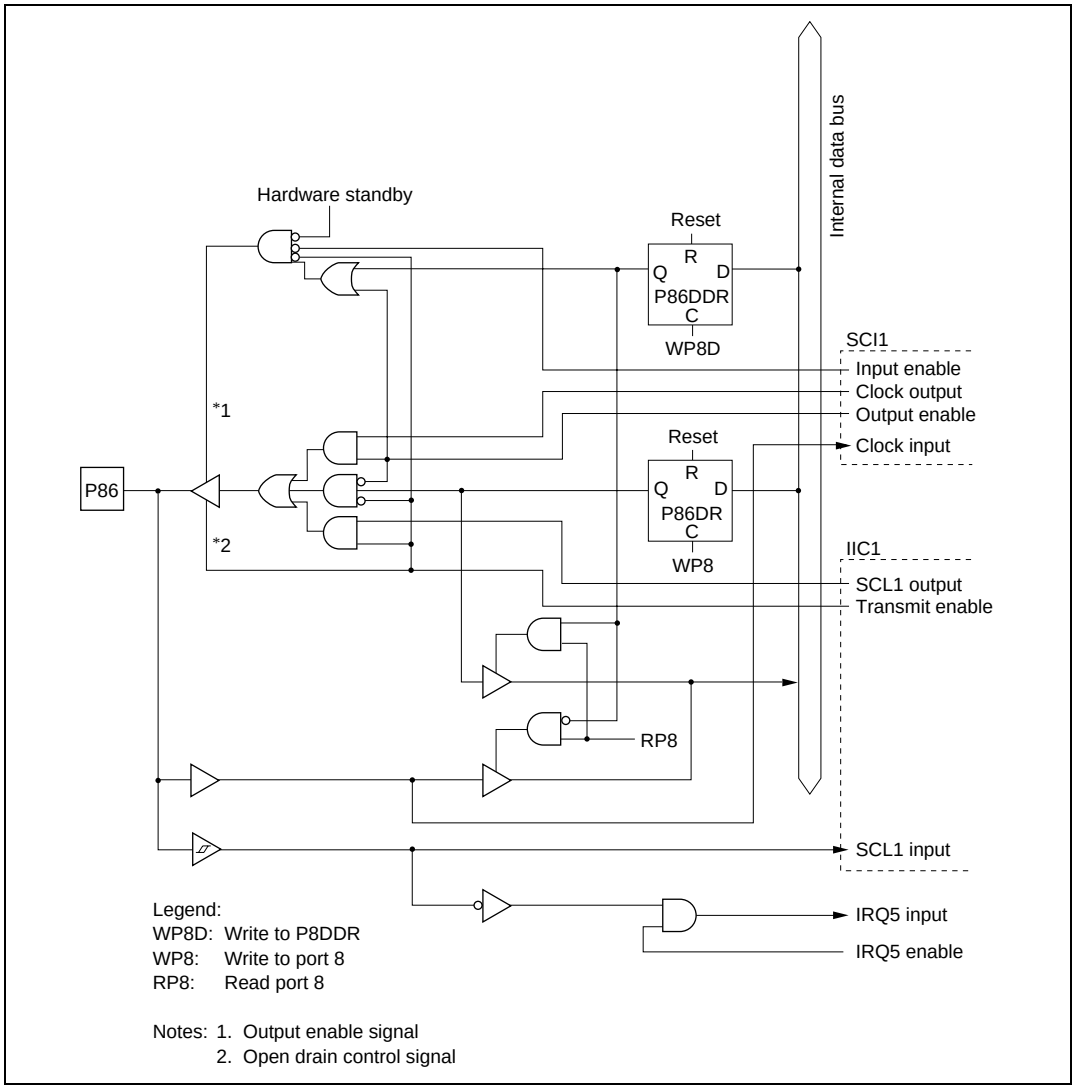


Figure C.28 Port 8 Block Diagram (Pin P86)