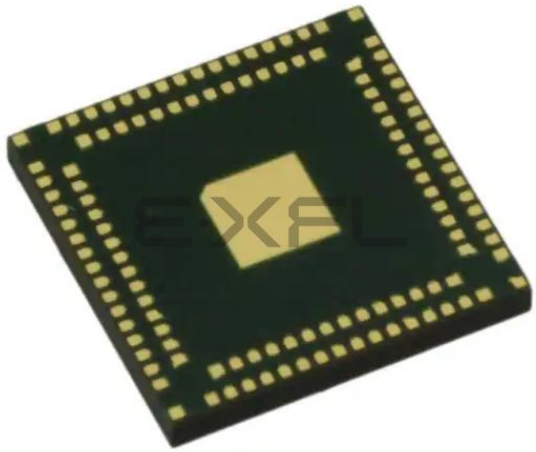

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

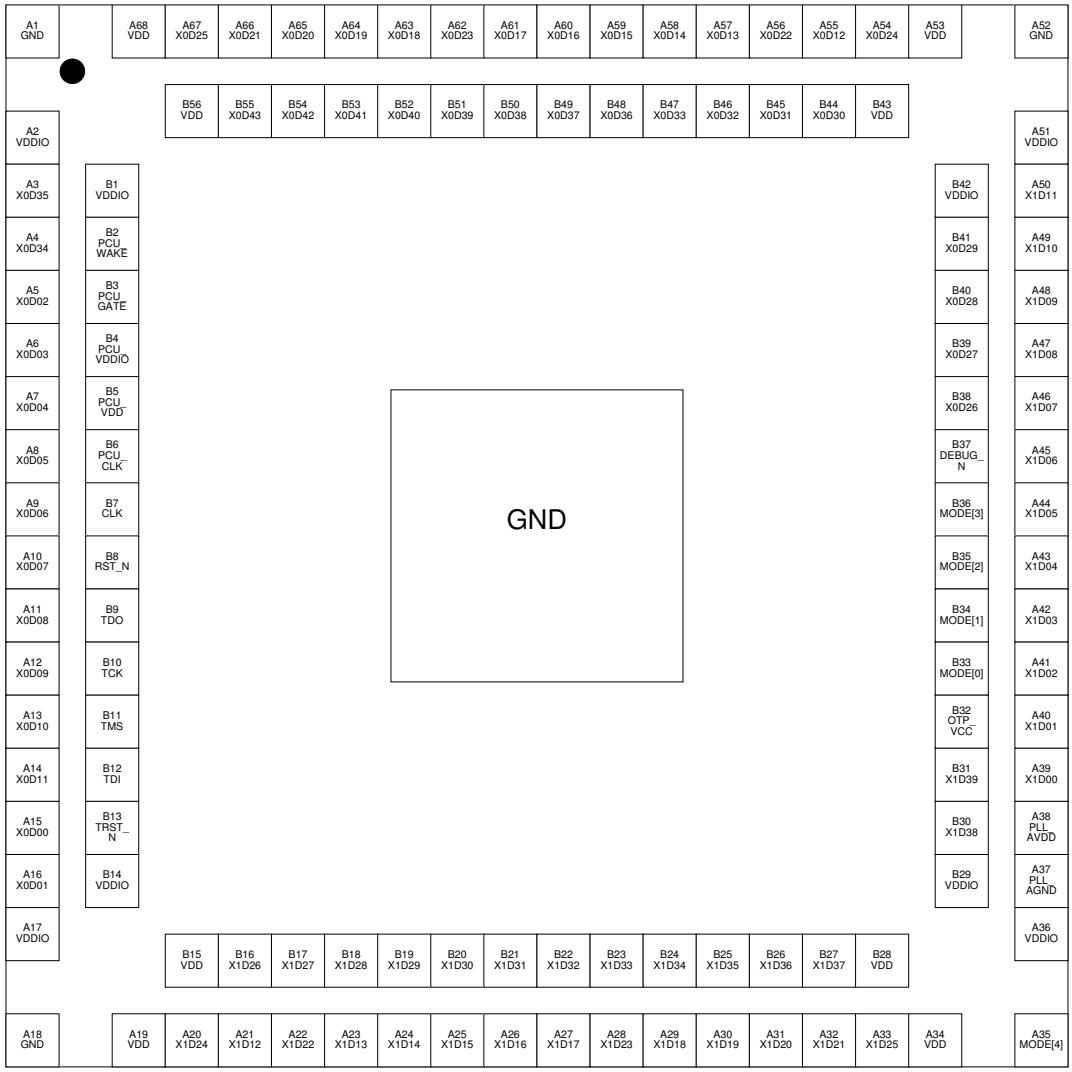
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 16-Core
Speed	800MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	84
Program Memory Size	128KB (32K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	124-TFQFN Dual Rows, Exposed Pad
Supplier Device Package	124-QFN DualRow (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-l16a-128-qf124-c8

2 XS1-L16A-128-QF124 Features

- **Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  - 16 real-time logical cores on 2 xCORE tiles
  - Cores share up to 1000 MIPS
  - Each logical core has:
    - Guaranteed throughput of between 1/4 and 1/8 of tile MIPS
    - 16x32bit dedicated registers
  - 159 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- **Programmable I/O**
  - 84 general-purpose I/O pins, configurable as input or output
    - Up to 32 x 1bit port, 12 x 4bit port, 7 x 8bit port, 3 x 16bit port
    - 4 xCONNECT links
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 64 channel ends for communication with other cores, on or off-chip
- **Memory**
  - 128KB internal single-cycle SRAM (max 64KB per tile) for code and data storage
  - 16KB internal OTP (max 8KB per tile) for application boot code
- **Hardware resources**
  - 12 clock blocks (6 per tile)
  - 20 timers (10 per tile)
  - 8 locks (4 per tile)
- **JTAG Module for On-Chip Debug**
- **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- **Ambient Temperature Range**
  - Commercial qualification: 0°C to 70°C
  - Industrial qualification: -40°C to 85°C
- **Speed Grade**
  - 10: 1000 MIPS
  - 8: 800 MIPS
- **Power Consumption**
  - Active Mode
    - 400 mA at 500 MHz (typical)
    - 320 mA at 400 MHz (typical)
  - Standby Mode
    - 28 mA
- **124-pin dual-row QFN package 0.5 mm pitch**

3 Pin Configuration



Signal	Function					Type	Properties
X1D00		$1A^0$				I/O	PD_S, R_S
X1D01	XLA^4_{out}	$1B^0$				I/O	PD_S, R_S
X1D02	XLA^3_{out}		$4A^0$	$8A^0$	$16A^0$ $32A^{20}$	I/O	PD_S, R_U
X1D03	XLA^2_{out}		$4A^1$	$8A^1$	$16A^1$ $32A^{21}$	I/O	PD_S, R_U
X1D04	XLA^1_{out}		$4B^0$	$8A^2$	$16A^2$ $32A^{22}$	I/O	PD_S, R_U
X1D05	XLA^0_{out}		$4B^1$	$8A^3$	$16A^3$ $32A^{23}$	I/O	PD_S, R_U
X1D06	XLA^0_{in}		$4B^2$	$8A^4$	$16A^4$ $32A^{24}$	I/O	PD_S, R_U
X1D07	XLA^1_{in}		$4B^3$	$8A^5$	$16A^5$ $32A^{25}$	I/O	PD_S, R_U
X1D08	XLA^2_{in}		$4A^2$	$8A^6$	$16A^6$ $32A^{26}$	I/O	PD_S, R_U
X1D09	XLA^3_{in}		$4A^3$	$8A^7$	$16A^7$ $32A^{27}$	I/O	PD_S, R_U
X1D10	XLA^4_{in}	$1C^0$				I/O	PD_S, R_S
X1D11		$1D^0$				I/O	PD_S, R_S
X1D12		$1E^0$				I/O	PD_S, R_U
X1D13	XLB^4_{out}	$1F^0$				I/O	PD_S, R_U
X1D14	XLB^3_{out}		$4C^0$	$8B^0$	$16A^8$ $32A^{28}$	I/O	PD_S, R_U
X1D15	XLB^2_{out}		$4C^1$	$8B^1$	$16A^9$ $32A^{29}$	I/O	PD_S, R_U
X1D16	XLB^1_{out}		$4D^0$	$8B^2$	$16A^{10}$	I/O	PD_S, R_U
X1D17	XLB^0_{out}		$4D^1$	$8B^3$	$16A^{11}$	I/O	PD_S, R_U
X1D18	XLB^0_{in}		$4D^2$	$8B^4$	$16A^{12}$	I/O	PD_S, R_U
X1D19	XLB^1_{in}		$4D^3$	$8B^5$	$16A^{13}$	I/O	PD_S, R_U
X1D20	XLB^2_{in}		$4C^2$	$8B^6$	$16A^{14}$ $32A^{30}$	I/O	PD_S, R_U
X1D21	XLB^3_{in}		$4C^3$	$8B^7$	$16A^{15}$ $32A^{31}$	I/O	PD_S, R_U
X1D22	XLB^4_{in}	$1C^0$				I/O	PD_S, R_U
X1D23		$1H^0$				I/O	PD_S, R_U
X1D24		$1I^0$				I/O	PD_S
X1D25		$1J^0$				I/O	PD_S
X1D26			$4E^0$	$8C^0$	$16B^0$	I/O	PD_S, R_U
X1D27			$4E^1$	$8C^1$	$16B^1$	I/O	PD_S, R_U
X1D28			$4F^0$	$8C^2$	$16B^2$	I/O	PD_S, R_U
X1D29			$4F^1$	$8C^3$	$16B^3$	I/O	PD_S, R_U
X1D30			$4F^2$	$8C^4$	$16B^4$	I/O	PD_S, R_U
X1D31			$4F^3$	$8C^5$	$16B^5$	I/O	PD_S, R_U
X1D32			$4E^2$	$8C^6$	$16B^6$	I/O	PD_S, R_U
X1D33			$4E^3$	$8C^7$	$16B^7$	I/O	PD_S, R_U
X1D34		$1K^0$				I/O	PD_S
X1D35		$1L^0$				I/O	PD_S
X1D36		$1M^0$		$8D^0$	$16B^8$	I/O	PD_S
X1D37		$1N^0$		$8D^1$	$16B^9$	I/O	PD_S, R_U
X1D38		$1O^0$		$8D^2$	$16B^{10}$	I/O	PD_S, R_U
X1D39		$1P^0$		$8D^3$	$16B^{11}$	I/O	PD_S, R_U

pins (5)			
Signal	**Function**	**Type**	**Properties**
PCU_CLK	Clock input		
PCU_GATE	Power control gate control		
PCU_VDD	PCU tile power		
PCU_VDDIO	PCU I/O supply		
PCU_WAKE	Wakeup reset		

5 Product Overview

The XS1-L16A-128-QF124 is a powerful device that consists of two xCORE Tiles, each comprising a flexible logical processing cores with tightly integrated I/O and on-chip memory.

5.1 Logical cores

Each tile has 8 active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for n cores). Figure 2 shows the guaranteed core performance depending on the number of cores used.

Figure 2: Logical core performance

Speed grade	MIPS	Frequency	Minimum MIPS per core (for *n* cores)							
			1	2	3	4	5	6	7	8
8	800 MIPS	400 MHz	100	100	100	100	80	67	57	50
10	1000 MIPS	500 MHz	125	125	125	125	100	83	71	63

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum but cannot be guaranteed.

The logical cores are triggered by events instead of interrupts and run to completion. A logical core can be paused to wait for an event.

5.2 xTIME scheduler

The xTIME scheduler handles the events generated by xCORE Tile resources, such as channel ends, timers and I/O pins. It ensures that all events are serviced and synchronized, without the need for an RTOS. Events that occur at the I/O pins are handled by the Hardware-Response ports and fed directly to the appropriate xCORE Tile. An xCORE Tile can also choose to wait for a specified time to elapse, or for data to become available on a channel.

Tasks do not need to be prioritised as each of them runs on their own logical xCORE. It is possible to share a set of low priority tasks on a single core using cooperative multitasking.

5.3 Hardware Response Ports

Hardware Response ports connect an xCORE tile to one or more physical pins and as such define the interface between hardware attached to the XS1-L16A-128-QF124, and the software running on it. A combination of 1bit, 4bit, 8bit, 16bit and 32bit ports are available. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

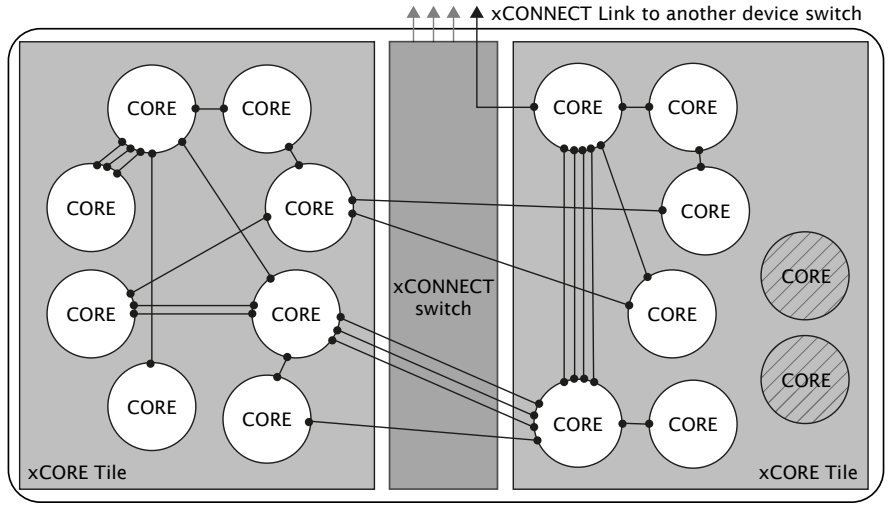


Figure 5: Switch, links and channel ends

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, X2999.

6 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock.

The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 6:

Figure 6: PLL multiplier values and MODE pins

Oscillator Frequency	MODE 1	MODE 0	Tile Frequency	PLL Ratio	PLL settings OD	F	R
5-13 MHz	0	0	130-399.75 MHz	30.75	1	122	0
13-20 MHz	1	1	260-400.00 MHz	20	2	119	0
20-48 MHz	1	0	167-400.00 MHz	8.33	2	49	0
48-100 MHz	0	1	196-400.00 MHz	4	2	23	0

Figure 6 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, F and R must be chosen so that $0 \leq R \leq 63$, $0 \leq F \leq 4095$, $0 \leq OD \leq 7$, and $260MHz \leq F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \leq 1.3GHz$. The OD, F, and R values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value during and after deassertion of the system reset.

If a different tile frequency is required (eg, 500 MHz), then the PLL must be reprogrammed after boot to provide the required tile frequency. The XMOS tools perform this operation by default. Further details on configuring the clock can be found in the XS1-L Clock Frequency Control document, X1433.

7 Boot Procedure

The device is kept in reset by driving RST_N low. When in reset, all GPIO pins are high impedance. When the device is taken out of reset by releasing RST_N the processor starts its internal reset process. After 15-150 μs (depending on the input clock), all GPIO pins have their internal pull-resistor enabled, and the processor boots at a clock speed that depends on MODE0 and MODE1.

The xCORE Tile boot procedure is illustrated in Figure 7. In normal usage, MODE[4:2] controls the boot source according to the table in Figure 8. If bit 5 of the security register (*see* §8.1) is set, the device boots from OTP.

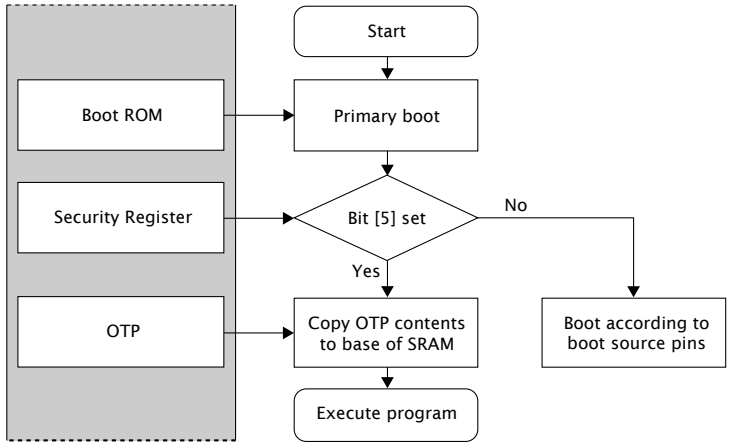


Figure 7: Boot procedure

The boot image has the following format:

- A 32-bit program size s in words.
- Program consisting of $s \times 4$ bytes.
- A 32-bit CRC, or the value 0x0D15AB1E to indicate that no CRC check should be performed.

MODE [4]	MODE [3]	MODE [2]	Boot Source
X	0	0	None: Device waits to be booted via JTAG
X	0	1	Reserved
0	1	0	Tile0 boots from link B, Tile1 from channel end 0 via Tile0
0	1	1	Tile0 boots from SPI, Tile1 from channel end 0 via Tile0
1	1	0	Tile0 and Tile1 independently enable link B and internal links (E, F, G, H), and boot from channel end 0
1	1	1	Tile0 and Tile 1 boot from SPI independently

Figure 8: Boot source pins

The program size and CRC are stored least significant byte first. The program is loaded into the lowest memory address of RAM, and the program is started from that address. The CRC is calculated over the byte stream represented by the program size and the program itself. The polynomial used is 0xEDB88320 (IEEE 802.3); the CRC register is initialized with 0xFFFFFFFF and the residue is inverted to produce the CRC.

7.1 Boot from SPI master

If set to boot from SPI master, the processor enables the four pins specified in Figure 9, and drives the SPI clock at 2.5 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

Pin	Signal	Description
X0D00	MISO	Master In Slave Out (Data)
X0D01	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)

Figure 9: SPI master pins

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. Programmers who write bytes into an SPI interface using the most significant bit first may have to reverse the bits in each byte of the image stored in the SPI device.

If a large boot image is to be read in, it is faster to first load a small boot-loader that reads the large image using a faster SPI clock, for example 50 MHz or as fast as the flash device supports.

The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

7.2 Boot from xConnect Link

If set to boot from an xConnect Link, the processor enables Link B around 200 ns after the boot process starts. Enabling the Link switches off the pull-down on

resistors X0D16..X0D19, drives X0D16 and X0D17 low (the initial state for the Link), and monitors pins X0D18 and X0D19 for boot-traffic. X0D18 and X0D19 must be low at this stage. If the internal pull-down is too weak to drain any residual charge, external pull-downs of 10K may be required on those pins.

The boot-rom on the core will then:

1. Allocate channel-end 0.
2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
3. Input the boot image specified above, including the CRC.
4. Input an END control token.
5. Output an END control token to the channel-end received in step 2.
6. Free channel-end 0.
7. Jump to the loaded code.

7.3 Boot from OTP

If an xCORE tile is set to use secure boot (see Figure 7), the boot image is read from address 0 of the OTP memory in the tile's security module.

This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

Each tile has its own individual OTP memory, and hence some tiles can be booted from OTP while others are booted from SPI or the channel interface. This enables systems to be partially programmed, dedicating one or more tiles to perform a particular function, leaving the other tiles user-programmable.

7.4 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 10 provide a strong level of protection and are sufficient for providing strong IP security.

8 Memory

8.1 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds

11.6 Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	4.22	20	100	MHz	
SR	Slew rate	0.10			V/ns	
TJ(LT)	Long term jitter (pk-pk)			2	%	A
f(MAX)	Processor clock frequency (Speed Grade 8)			400	MHz	B
	Processor clock frequency (Speed Grade 10)			500	MHz	B

Figure 23: Clock

A Percentage of CLK period.

B Assumes typical tile and I/O voltages with nominal activity.

Further details can be found in the XS1-L Clock Frequency Control document, X1433.

11.7 xCORE Tile I/O AC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

Figure 24: I/O AC characteristics

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

11.8 xConnect Link Performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	A, B
B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	B
B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	B

Figure 25: Link performance

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

B.1 RAM base address: 0x00

This register contains the base address of the RAM. It is initialized to 0x00010000.

0x00: RAM base address

Bits	Perm	Init	Description
31:2	RW		Most significant 16 bits of all addresses.
1:0	RO	-	Reserved

B.2 Vector base address: 0x01

Base address of event vectors in each resource. On an interrupt or event, the 16 most significant bits of the destination address are provided by this register; the least significant 16 bits come from the event vector.

0x01: Vector base address

Bits	Perm	Init	Description
31:16	RW		The most significant bits for all event and interrupt vectors.
15:0	RO	-	Reserved

B.3 xCORE Tile control: 0x02

Register to control features in the xCORE tile

0x02: xCORE Tile control

Bits	Perm	Init	Description
31:6	RO	-	Reserved
5	RW	0	Set to 1 to select the dynamic mode for the clock divider when the clock divider is enabled. In dynamic mode the clock divider is only activated when all active logical cores are paused. In static mode the clock divider is always enabled.
4	RW	0	Set to 1 to enable the clock divider. This slows down the xCORE tile clock in order to use less power.
3:0	RO	-	Reserved

B.4 xCORE Tile boot status: 0x03

This read-only register describes the boot status of the xCORE tile.

0x15: Debug interrupt type

Bits	Perm	Init	Description
31:18	RO	-	Reserved
17:16	DRW		If the debug interrupt was caused by a hardware breakpoint or hardware watchpoint, this field contains the number of the breakpoint or watchpoint. If multiple breakpoints or watchpoints trigger at once, the lowest number is taken.
15:8	DRW		If the debug interrupt was caused by a logical core, this field contains the number of that core. Otherwise this field is 0.
7:3	RO	-	Reserved
2:0	DRW	0	Indicates the cause of the debug interrupt 1: Host initiated a debug interrupt through JTAG 2: Program executed a DCALL instruction 3: Instruction breakpoint 4: Data watch point 5: Resource watch point

B.17 Debug interrupt data: 0x16

On a data watchpoint, this register contains the effective address of the memory operation that triggered the debugger. On a resource watchpoint, it countains the resource identifier.

0x16: Debug interrupt data

Bits	Perm	Init	Description
31:0	DRW		Value.

B.18 Debug core control: 0x18

This register enables the debugger to temporarily disable logical cores. When returning from the debug interrupts, the cores set in this register will not execute. This enables single stepping to be implemented.

0x18: Debug core control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7:0	DRW		1-hot vector defining which logical cores are stopped when not in debug mode. Every bit which is set prevents the respective logical core from running.

B.19 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over JTAG. This is the same set of registers as the Debug Scratch registers in the xCORE tile configuration.

0x20 .. 0x27: Debug scratch

Bits	Perm	Init	Description
31:0	DRW		Value.

B.20 Instruction breakpoint address: 0x30 .. 0x33

This register contains the address of the instruction breakpoint. If the PC matches this address, then a debug interrupt will be taken. There are four instruction breakpoints that are controlled individually.

0x30 .. 0x33: Instruction breakpoint address

Bits	Perm	Init	Description
31:0	DRW		Value.

B.21 Instruction breakpoint control: 0x40 .. 0x43

This register controls which logical cores may take an instruction breakpoint, and under which condition.

0x40 .. 0x43: Instruction breakpoint control

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each logical core in the tile allowing the breakpoint to be enabled individually for each logical core.
15:2	RO	-	Reserved
1	DRW	0	Set to 1 to cause an instruction breakpoint if the PC is not equal to the breakpoint address. By default, the breakpoint is triggered when the PC is equal to the breakpoint address.
0	DRW	0	When 1 the instruction breakpoint is enabled.

B.22 Data watchpoint address 1: 0x50 .. 0x53

This set of registers contains the first address for the four data watchpoints.

0x04: Control PSwitch permissions to debug registers

Bits	Perm	Init	Description
31:1	RO	-	Reserved
0	CRW		Set to 1 to restrict PSwitch access to all CRW marked registers to become read-only rather than read-write.

C.5 Cause debug interrupts: 0x05

This register can be used to raise a debug interrupt in this xCORE tile.

0x05: Cause debug interrupts

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RO	0	Set to 1 when the processor is in debug mode.
0	CRW	0	Set to 1 to request a debug interrupt on the processor.

C.6 xCORE Tile clock divider: 0x06

This register contains the value used to divide the PLL clock to create the xCORE tile clock. The divider is enabled under control of the tile control register

0x06: xCORE Tile clock divider

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7:0	RW		Value of the clock divider minus one.

C.7 Security configuration: 0x07

Copy of the security register as read from OTP.

0x07: Security configuration

Bits	Perm	Init	Description
31:0	RO		Value.

C.8 PLink status: 0x10 .. 0x13

Status of each of the four processor links; connecting the xCORE tile to the switch.

C.21 SR of logical core 3: 0x63

0x63: SR of logical core 3

Bits	Perm	Init	Description
31:0	RO		Value.

C.22 SR of logical core 4: 0x64

0x64: SR of logical core 4

Bits	Perm	Init	Description
31:0	RO		Value.

C.23 SR of logical core 5: 0x65

0x65: SR of logical core 5

Bits	Perm	Init	Description
31:0	RO		Value.

C.24 SR of logical core 6: 0x66

0x66: SR of logical core 6

Bits	Perm	Init	Description
31:0	RO		Value.

C.25 SR of logical core 7: 0x67

0x67: SR of logical core 7

Bits	Perm	Init	Description
31:0	RO		Value.

C.26 Chanend status: 0x80 .. 0x9F

These registers record the status of each channel-end on the tile.

0x01: System switch description

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		Number of links on the switch.
15:8	RO		Number of cores that are connected to this switch.
7:0	RO		Number of links per processor.

D.3 Switch configuration: 0x04

This register enables the setting of two security modes (that disable updates to the PLL or any other registers) and the header-mode.

0x04: Switch configuration

Bits	Perm	Init	Description
31	RO	0	Set to 1 to disable any write access to the configuration registers in this switch.
30:9	RO	-	Reserved
8	RO	0	Set to 1 to disable updates to the PLL configuration register.
7:1	RO	-	Reserved
0	RO	0	Header mode. Set to 1 to enable 1-byte headers. This must be performed on all nodes in the system.

D.4 Switch node identifier: 0x05

This register contains the node identifier.

0x05: Switch node identifier

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	The unique 16-bit ID of this node. This ID is matched most-significant-bit first with incoming messages for routing purposes.

D.5 PLL settings: 0x06

An on-chip PLL multiplies the input clock up to a higher frequency clock, used to clock the I/O, processor, and switch, see Oscillator. Note: a write to this register will cause the tile to be reset.

- TDO to pin 13 of the xSYS header
- RST_N and TRST_N to pin 15 of the xSYS header
- If MODE2 is configured high, connect MODE2 to pin 3 of the xSYS header. Do not connect to VDDIO.
- If MODE3 is configured high, connect MODE3 to pin 3 of the xSYS header. Do not connect to VDDIO.

The RST_N net should be open-drain, active-low, and have a pull-up to VDDIO.

G.3 Full xSYS header

For a full xSYS header you will need to connect the pins as discussed in Section G.2, and then connect a 2-wire xCONNECT Link to the xSYS header. The links can be found in the Signal description table (Section 4): they are labelled XLA, XLB, etc in the function column. The 2-wire link comprises two inputs and outputs, labelled ${}^{1}_{out}$, ${}^{0}_{out}$, ${}^{0}_{in}$, and ${}^{1}_{in}$. For example, if you choose to use XLB of tile 0 for xSCOPE I/O, you need to connect up XLB^{1}_{out}, XLB^{0}_{out}, XLB^{0}_{in}, XLB^{1}_{in} as follows:

- XLB^{1}_{out} (X0D16) to pin 6 of the xSYS header with a 33R series resistor close to the device.
- XLB^{0}_{out} (X0D17) to pin 10 of the xSYS header with a 33R series resistor close to the device.
- XLB^{0}_{in} (X0D18) to pin 14 of the xSYS header.
- XLB^{1}_{in} (X0D19) to pin 18 of the xSYS header.

H Schematics Design Check List

☑ This section is a checklist for use by schematics designers using the XS1-L16A-128-QF124. Each of the following sections contains items to check for each design.

H.1 Power supplies

☐ VDDIO and OTP_VCC supply is within specification before the VDD (core) supply is turned on. Specifically, the VDDIO and OTP_VCC supply is within specification before VDD (core) reaches 0.4V (Section 10).

☐ The VDD (core) supply ramps monotonically (rises constantly) from 0V to its final value (0.95V - 1.05V) within 10ms (Section 10).

☐ The VDD (core) supply is capable of supplying 600mA (Section 10).

☐ PLL_AVDD is filtered with a low pass filter, for example an RC filter, see Section 10

☐ The PCU_VDD pin is connected to the VDD supply and PCU_VDDIO is connected to the VDDIO supply (Section 10).

H.2 Power supply decoupling

☐ The design has multiple decoupling capacitors per supply, for example at least four0402 or 0603 size surface mount capacitors of 100nF in value, per supply (Section 10).

☐ A bulk decoupling capacitor of at least 10uF is placed on each supply (Section 10).

H.3 Power on reset

☐ The RST_N and TRST_N pins are asserted (low) during or after power up. The device is not used until these resets have taken place.
As the errata in the datasheets show, the internal pull-ups on these two pins can occasionally provide stronger than normal pull-up currents. For this reason, an RC type reset circuit is discouraged as behavior would be unpredictable. A voltage supervisor type reset device is recommended to guarantee a good reset. This also has the benefit of resetting the system should the relevant supply go out of specification.

I PCB Layout Design Check List

☑ This section is a checklist for use by PCB designers using the XS1-L16A-128-QF124. Each of the following sections contains items to check for each design.

I.1 Land pattern and solder stencil

☐ You have used a land pattern suitable for the small QFN pads. (Section 10.1)

☐ You have used a solder stencil with the correct aperture and thinness. (Section 10.1)

I.2 Ground Plane

☐ Multiple vias (eg, 9) have been used to connect the center pad to the PCB ground plane. These minimize impedance and conduct heat away from the device. (Section 10.3).

☐ Other than ground vias, there are no (or only a few) vias underneath or closely around the device. This create a good, solid, ground plane.

I.3 Power supply decoupling

☐ The decoupling capacitors are all placed close to a supply pin (Section 10).

☐ The decoupling capacitors are spaced around the device (Section 10).

☐ The ground side of each decoupling capacitor has a direct path back to the center ground of the device.

I.4 PLL_AVDD

☐ The PLL_AVDD filter (especially the capacitor) is placed close to the PLL_AVDD pin (Section 10).

L Revision History

Date	Description
2013-01-30	New datasheet - revised part numbering
2013-02-26	New multicore microcontroller introduction Moved configuration sections to appendices
2013-07-19	Updated Features list with available ports and links - Section 2 Simplified link bits in Signal Description - Section 4 New JTAG, xSCOPE and Debugging appendix - Section G New Schematics Design Check List - Section H New PCB Layout Design Check List - Section I
2013-09-16	Removed references to PCU. Pins set to GND - Section 3
2013-12-09	Added Industrial Ambient Temperature - Section 11.1
2013-12-17	Added references to PCU - Section 3 and 9.1
2014-03-25	Updated BOTTOM VIEW in mechanical drawing - Section 12
2014-06-25	Added PCU_GATE, PCU_CLK, PCU_VDD, PCU_VDDIO to Schematics Checklist - Section H
2015-04-14	Updated Introduction - Section 1; Pin Configuration - Section 3; Signal Description - Section 4