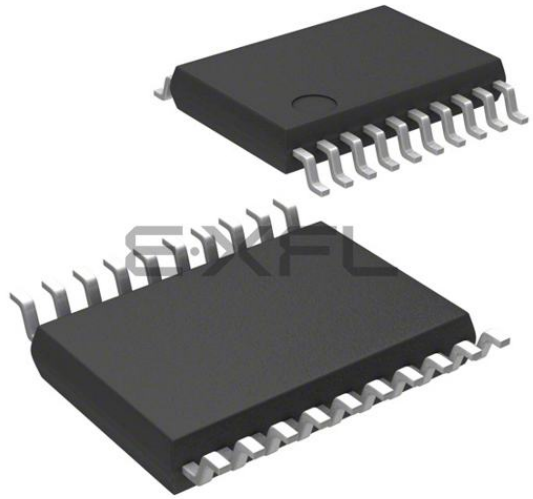

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6213pcau

Contents

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module together with an integrated debug module permit non-intrusive, real-time in-circuit debugging and fast memory programming.

4.2.1 SWIM

Single wire interface module for direct access to the debug mode and memory programming. The interface can be activated in all device operation modes.The maximum data transmission speed is 145 byte/ms.

4.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined breakpoint configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 28 external interrupts on 7 vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- Up to 8 Kbytes of Flash program single voltage Flash memory
- 640 byte true data EEPROM
- User option byte area

4.4.1 Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option byte.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option byte.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

5 Pinout and pin description

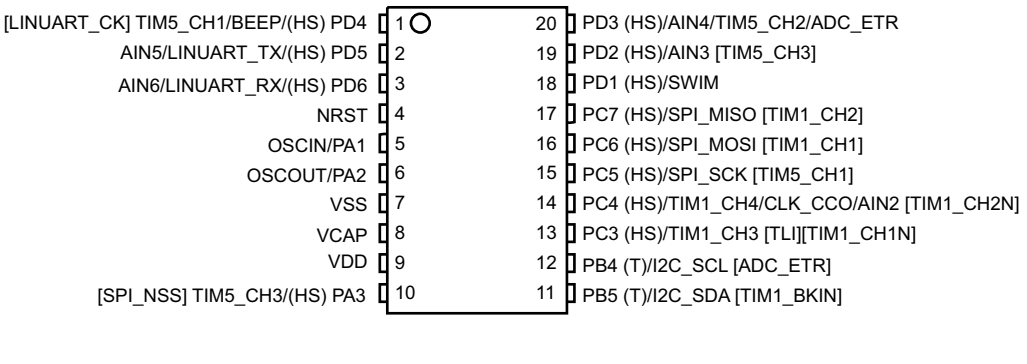
The following table presents the meaning of the abbreviations in use in the pin description tables in this section.

Table 5. Legend/abbreviations for pinout tables

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

5.1 TSSOP20 pinouts and pin descriptions

Figure 3. STM8AF6213/STM8AF6223 TSSOP20 pinout



1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 7. STM8AF6223A TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
3	PD6/ AIN6/ LINUART_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ LINUART data receive	-
4	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
11	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
12	PB1/ TIM1_CH2N/ AIN1	I/O	**X**	X	X	HS	O3	X	X	Port B1	Timer 1 - inverted channel 2/Analog input 1	-
13	PB0/ TIM1_CH1N/AIN0	I/O	**X**	X	X	HS	O3	X	X	Port B0	Timer 1 - inverted channel 1/Analog input 0	-
14	PC4/ TIM1_CH4/ CLK_CCO/AIN2/[TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 channel 2 [AFR7]
15	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]

Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)

LQFP32 VFQPN32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
17	PE5/ SPI_NSS [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port E5	SPI master/ slave select	Timer 1 - inverted channel 1 [AFR1:0]
18	PC1/ TIM1_CH1/ LINUART_CK [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 LINUART clock	Timer 1 - inverted channel 2 [AFR1:0]
19	PC2/ TIM1_CH2 [TIM1_CH3N]	I/O	**X**	X	X	HS	O3	X	X	Port C2	Timer 1 - channel 2	Timer 1 - inverted channel 3 [AFR1:0]
20	PC3/ TIM1_CH3/[TLI] [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7]
21	PC4/ TIM1_CH4/ CLK_CCO/[AIN 2][TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7]
22	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]
23	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
24	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
25	PD0/ TIM1_BKIN [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	Port D0	Timer 1 - break input	Configurable clock output [AFR5]
26	PD1/ SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	Port D1	SWIM data interface	-

6 Memory and register map

6.1 Memory map

Figure 6. Memory map

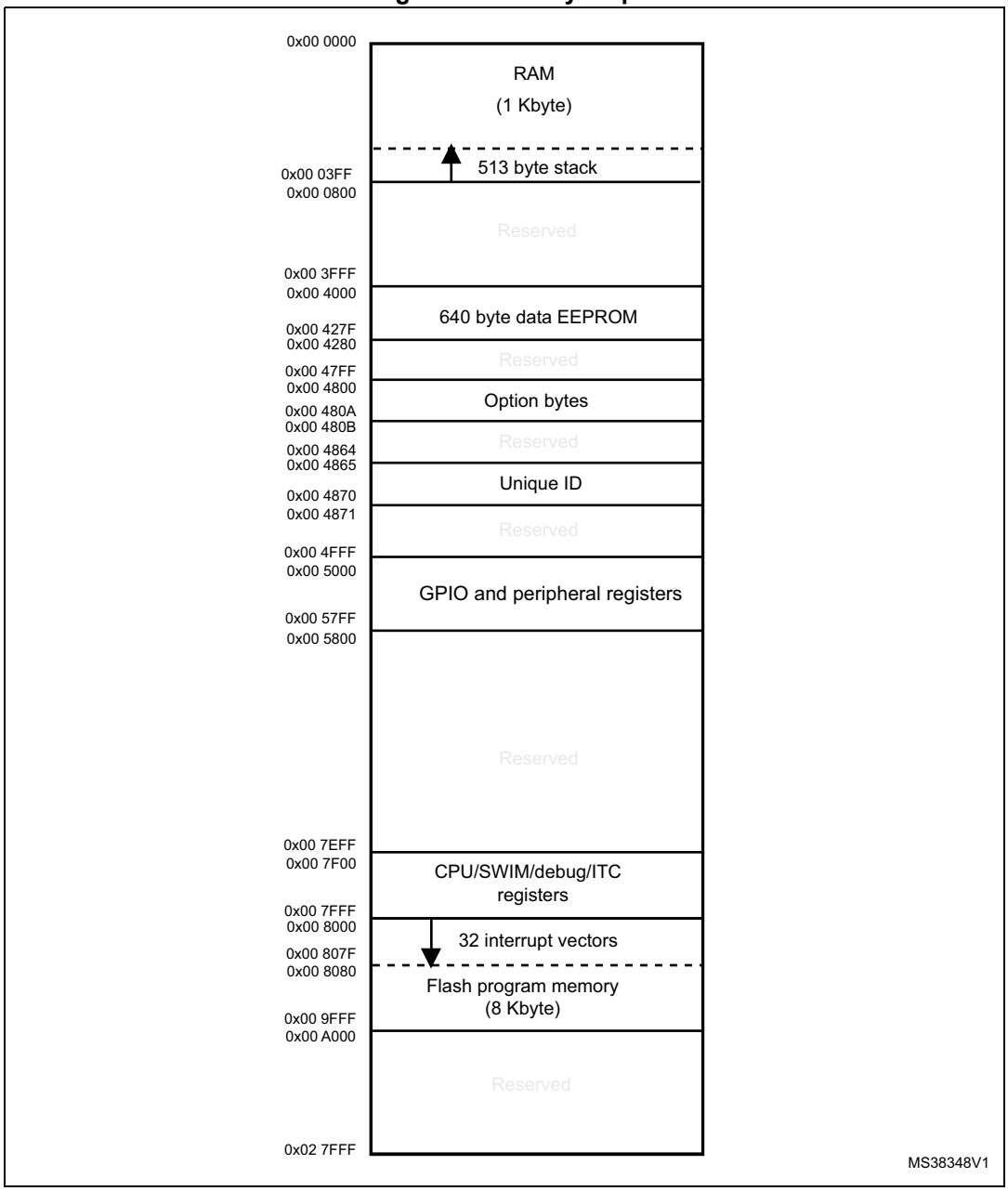


Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM5	TIM5_CR1	TIM5 control register 1	0x00
0x00 5301		TIM5_CR2	TIM5 control register 2	0x00
0x00 5302		TIM5_SMCR	TIM5 slave mode control register	0x00
0x00 5303		TIM5_IER	TIM5 interrupt enable register	0x00
0x00 5304		TIM5_SR1	TIM5 status register 1	0x00
0x00 5305		TIM5_SR2	TIM5 status register 2	0x00
0x00 5306		TIM5_EGR	TIM5 event generation register	0x00
0x00 5307		TIM5_CCMR1	TIM5 capture/compare mode register 1	0x00
0x00 5308		TIM5_CCMR2	TIM5 capture/compare mode register 2	0x00
0x00 5309		TIM5_CCMR3	TIM5 capture/compare mode register 3	0x00
0x00 530A		TIM5_CCER1	TIM5 capture/compare enable register 1	0x00
0x00 530B		TIM5_CCER2	TIM5 capture/compare enable register 2	0x00
00 530C0x		TIM5_CNTRH	TIM5 counter high	0x00
0x00 530D		TIM5_CNTRL	TIM5 counter low	0x00
0x00 530E		TIM5_PSCR	TIM5 prescaler register	0x00
0x00 530F		TIM5_ARRH	TIM5 auto-reload register high	0xFF
0x00 5310		TIM5_ARRL	TIM5 auto-reload register low	0xFF
0x00 5311		TIM5_CCR1H	TIM5 capture/compare register 1 high	0x00
0x00 5312		TIM5_CCR1L	TIM5 capture/compare register 1 low	0x00
0x00 5313		TIM5_CCR2H	TIM5 capture/compare reg. 2 high	0x00
0x00 5314		TIM5_CCR2L	TIM5 capture/compare register 2 low	0x00
0x00 5315		TIM5_CCR3H	TIM5 capture/compare register 3 high	0x00
0x00 5316		TIM5_CCR3L	TIM5 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			
0x00 5340	TIM6	TIM6_CR1	TIM6 control register 1	0x00
0x00 5341		TIM6_CR2	TIM6 control register 2	0x00
0x00 5342		TIM6_SMCR	TIM6 slave mode control register	0x00
0x00 5343		TIM6_IER	TIM6 interrupt enable register	0x00
0x00 5344		TIM6_SR	TIM6 status register	0x00
0x00 5345		TIM6_EGR	TIM6 event generation register	0x00
0x00 5346		TIM6_CNTR	TIM6 counter	0x00
0x00 5347		TIM6_PSCR	TIM6 prescaler register	0x00
0x00 5348		TIM6_ARR	TIM6 auto-reload register	0xFF

Table 11. General hardware register map (continued)

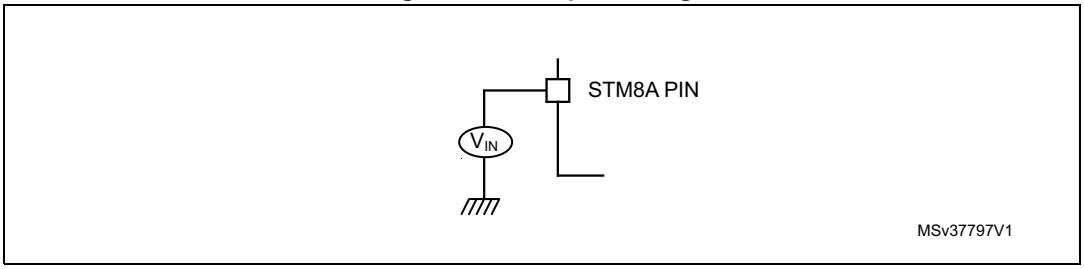
Address	Block	Register label	Register name	Reset status
0x00 5349 to 0x00 53DF	Reserved area (153 byte)			
0x00 53E0 to 0x00 53F3	ADC1	ADC _DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 byte)			
0x00 5400	ADC1	ADC _CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC _HTRH	ADC high threshold register high	0xFF
0x00 5409		ADC_HTRL	ADC high threshold register low	0x03
0x00 540A		ADC _LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC _AWSRH	ADC watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC watchdog control register high	0x00
0x00 540F		ADC _AWCRL	ADC watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write only register.

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 8. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics* and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 28. Total current consumption with code execution in run mode at V_{DD} = 5 V (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4.5	-	mA
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.7	4.5(1)	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	2(1)	
		$f_{CPU} = f_{MASTER}$/128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$/128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Tested in production.
2. Default clock configuration measured with all peripherals off.

Table 29. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ =16 MHz	HSE crystal osc. (16 MHz)	1.8	-	mA
			HSE user ext. clock (16 MHz)	2	2.3	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}$/128 = 125 kHz	HSE user ext. clock (16 MHz)	0.81	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$/ 128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ =128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4	-	
			HSE user ext. clock (16 MHz)	3.9	4.7	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ =2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$/ 128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$/128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ =128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 32. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85°C	Max at 125°C	Max at 150°C	Unit
		Main voltage regulator (MVR)(1)	Flash mode(2)	Clock source					
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	-	µA
				LSI RC osc. (128 kHz)	200	260	300	-	
			Power-down mode	HSE crystal osc. (16 MHz)	970	-	-	-	
				LSI RC osc. (128 kHz)	150	200	230	-	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	140	200	
			Power-down mode	LSI RC osc. (128 kHz)	10	20	40	-	

1. Configured by the REGAH bit in the CLK_ICKR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.

Table 33. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85°C(1)	Max at 125°C	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	µA
				LSI RC osc. (128 kHz)	200	260	290	
			Power-down mode	HSE crystal osc. (16 MHz)	970	-	-	
				LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power-down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 34. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85°C	Max at 125°C	Max at 150°C	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	-	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20(1)	55(1)	80(1)	

1. Tested in production.

Table 35. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85°C(1)	Max at 125°C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low-power mode wakeup times

Table 36. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(2)	0 to 16 MHz			-	See (3)	µs
		f_{CPU}= f_{MASTER}= 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
					3(6)	-	
		MVR voltage regulator off			48(6)	-	
					50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in operating mode(5)			52	-	
		Flash in power-down mode(5)			54	-	

1. Guaranteed by design.
2. Measured from interrupt event to interrupt vector fetch.
3. $t_{WU(WFI)}$ = 2 x 1/f_{MASTER}+ 67 x 1/f_{CPU}.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Figure 15. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V

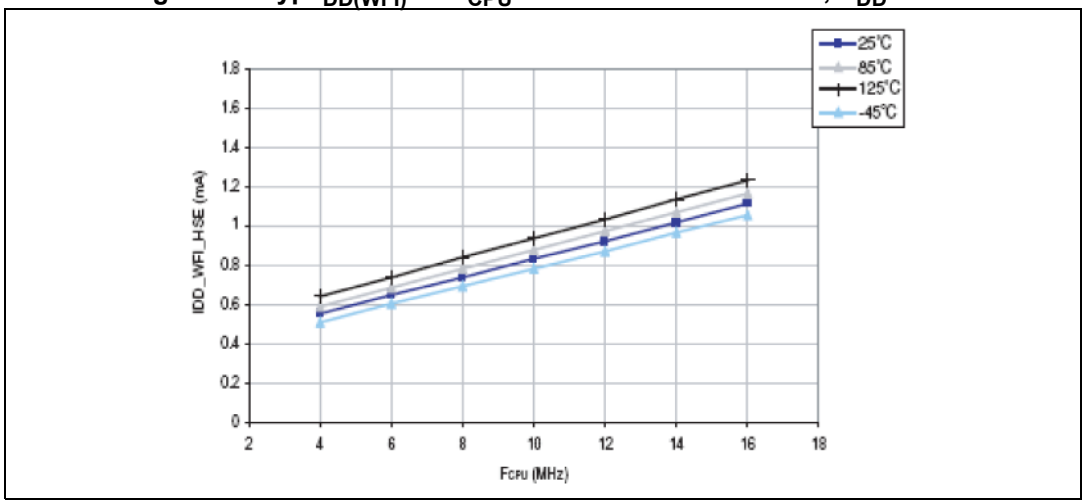
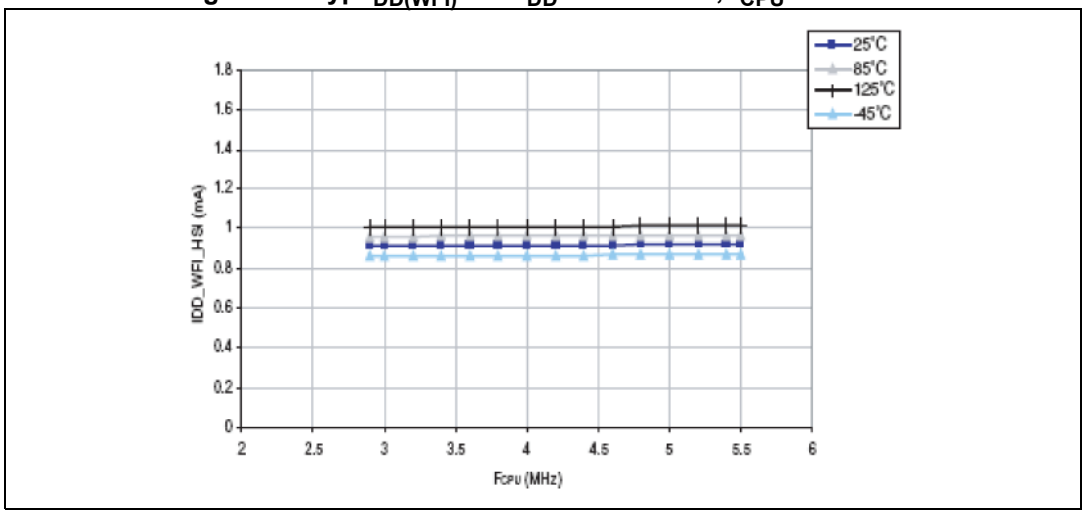


Figure 16. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



HSE crystal/ceramic resonator oscillator

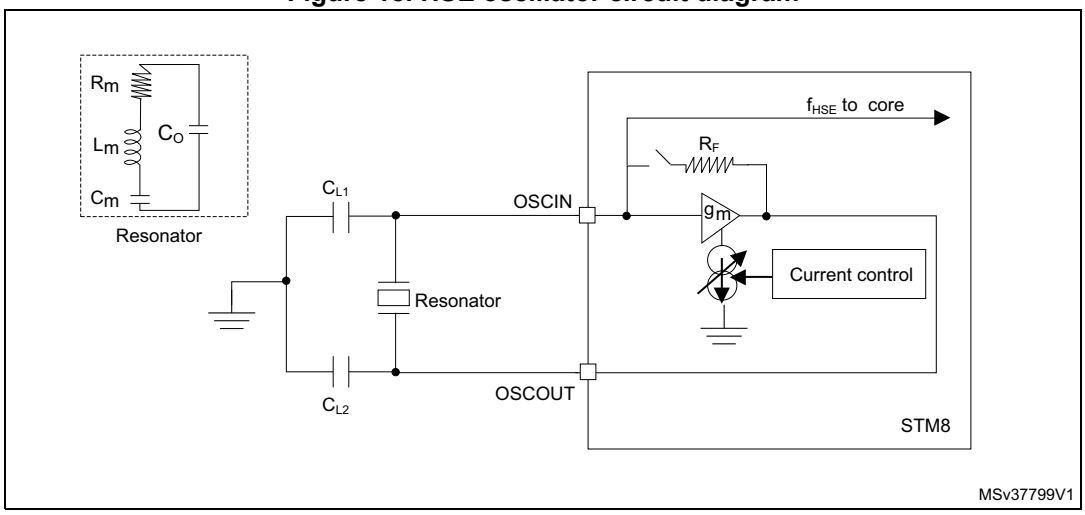
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 40. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high-speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.6 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to the crystal manufacturer for more details.
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. The value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

The crystal characteristics have to be checked with the following formula:

$$g_m \gg g_{mcrit}$$

where g_{mcrit} can be calculated with the crystal parameters as follows:

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance

9.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator (HSI)

Table 41. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1(1)	-	1(1)	%
			-0.5(1)	-	0.5(1)	
	HSI oscillator accuracy (factory calibrated)	3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 150 °C	-5	-	5	
		3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	-3(2)	-	3(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250(3)	µA

1. Depending on option byte setting (OPT3 and NOPT3).
2. These values are guaranteed for STM8AF62xxIxx order codes only.
3. Guaranteed by characterization results.

Figure 21. Typical pull-up current I_{pu} vs V_{DD} @ 4 temperatures

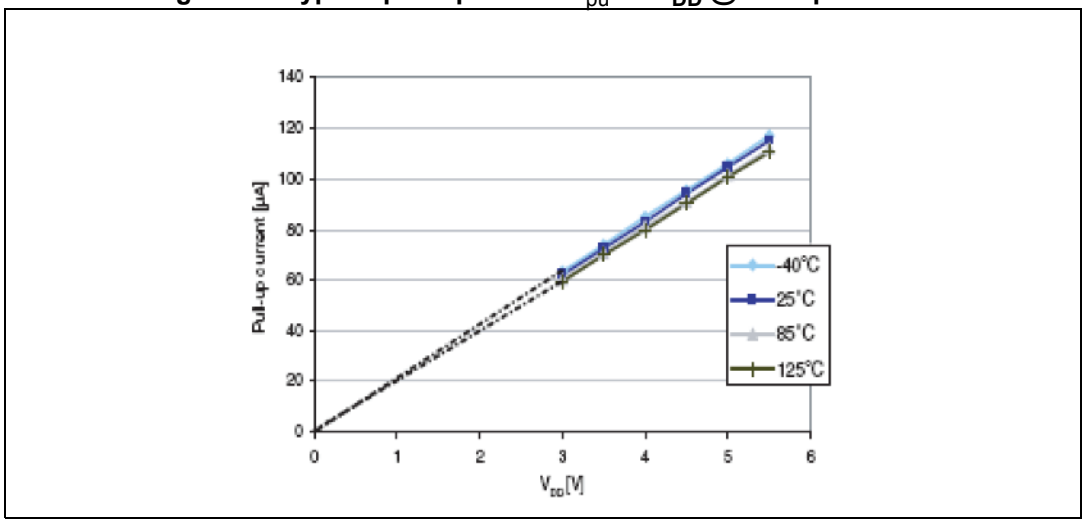


Table 48. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO} = 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Guaranteed by characterization results.

Table 49. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	1.0	V
		I_{IO} = 10 mA, V_{DD} = 3.3 V	1.5(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V	2.0(1)	

1. Guaranteed by characterization results.

9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD} = 3 to 5.5 V	1	-	4	MHz
		V_{DD} = 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 3 to 5.5 V	1.19(2)	1.22	1.25(2)	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7	-	
t_{CONV}	Minimum total conversion time including sampling time, 10-bit resolution	f_{ADC} = 4 Hz	3.5			µs
		f_{ADC} = 6 MHz	2.33			
		-	14			$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
2. Tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin),
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 60. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).