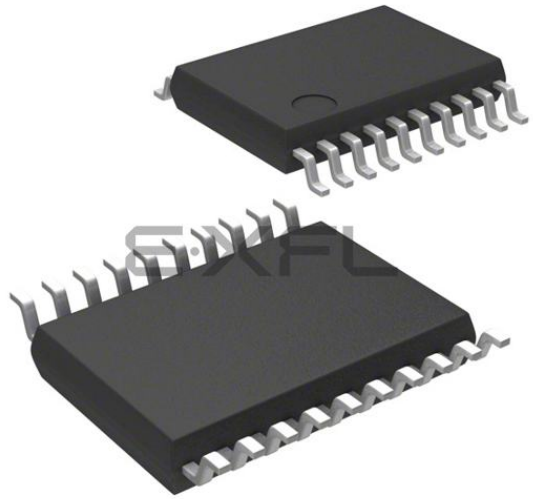

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6213pcax

List of figures

1 Introduction

The datasheet contains the description of STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode**: in this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active-halt mode with regulator on**: in this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active-halt mode with regulator off**: this mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode**: in this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: the downcounter is refreshed before its value is lower than the one stored in the window register.

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 Serial peripheral interface (SPI)

- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave /master selection input pin

4.14.3 Inter integrated circuit (I^2C) interface

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description (continued)

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
19	PD2/AIN3 [TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1]
20	PD3/ AIN4/ TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4 Timer 52 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 9.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 7. STM8AF6223A TSSOP20 pin description

TSSOP	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	PD4/ TIM5_CH1/ BEEP/SPI_NSS [LINUART_CK]	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 5 - channel 1/BEEP output	LINUART clock [AFR2]
2	PD5/ AIN5/ LINUART_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ LINUART data transmit	-

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	LINUART	UART4_SR	LINUART status register	0xC0
0x00 5231		UART4_DR	LINUART data register	0xXX
0x00 5232		UART4_BRR1	LINUART baud rate register 1	0x00
0x00 5233		UART4_BRR2	LINUART baud rate register 2	0x00
0x00 5234		UART4_CR1	LINUART control register 1	0x00
0x00 5235		UART4_CR2	LINUART control register 2	0x00
0x00 5236		UART4_CR3	LINUART control register 3	0x00
0x00 5237		UART4_CR4	LINUART control register 4	0x00
0x00 5238		Reserved		
0x00 5239		UART4_CR6	LINUART control register 6	0x00
0x00 523A		UART4_GTR	LINUART guard time register	0x00
0x00 523B		UART4_PSCR	LINUART prescaler	0x00
0x00 523C to 0x00 523F	Reserved area (20 byte)			

Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

8.1 Option byte description

Table 15. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]: User boot code area** 0x00: No UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected 0x02: Page 0 to 1 defined as UBC, memory write-protected Pages 0 and 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Page 0 to 127 defined as UBC, memory write-protected. *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following sections for the alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM: high-speed internal clock trimming register size** 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: low-speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG independent watchdog activated by software 1: IWDG independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on Halt 0: No reset generated on Halt if WWDG active 1: Reset generated on Halt if WWDG active

9 Electrical characteristics

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

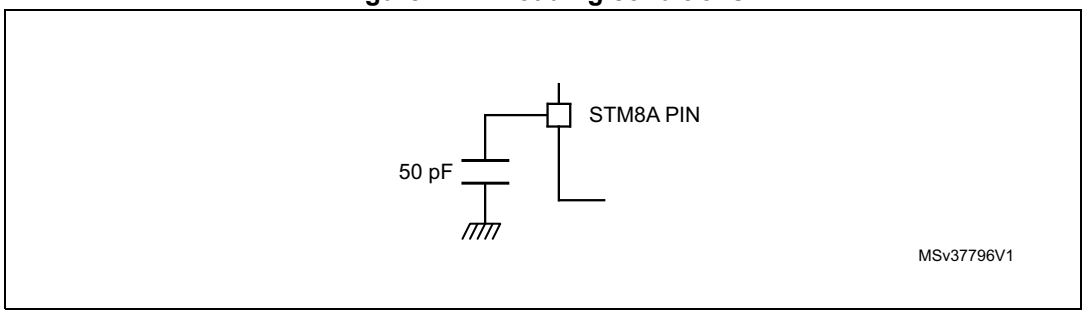
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

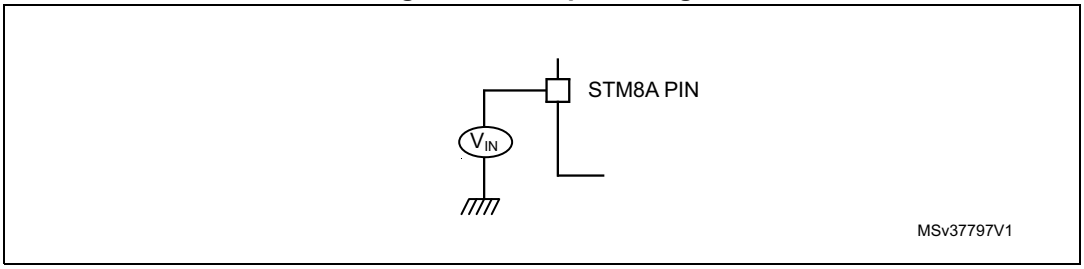
Figure 7. Pin loading conditions



9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 8. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics* and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics

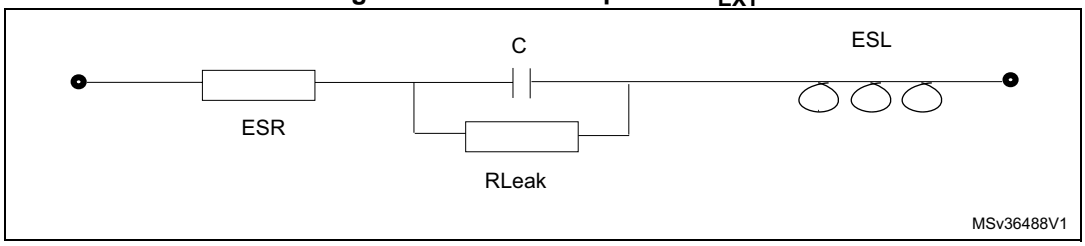
Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 26*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 10. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in *Section 4.3: Interrupt controller*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Unless otherwise specified, data are based on characterization results, and not tested in production.

Table 28. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2(1)	
		$f_{CPU} = f_{MASTER}/128$= 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}/128$= 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 28 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

Total current consumption in halt mode

Table 34. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85°C	Max at 125°C	Max at 150°C	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	-	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20(1)	55(1)	80(1)	

1. Tested in production.

Table 35. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85°C(1)	Max at 125°C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low-power mode wakeup times

Table 36. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(2)	0 to 16 MHz			-	See (3)	µs
		f_{CPU}= f_{MASTER}= 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
					3(6)	-	
		MVR voltage regulator off			48(6)	-	
					50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in operating mode(5)			52	-	
		Flash in power-down mode(5)			54	-	

1. Guaranteed by design.
2. Measured from interrupt event to interrupt vector fetch.
3. $t_{WU(WFI)}$ = 2 x 1/f_{MASTER}+ 67 x 1/f_{CPU}.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 37. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD}= 5 V	400	-	µA
		V_{DD}= 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption for on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 38. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM5)}$	TIM5 supply current(1)	130	
$I_{DD(TIM6)}$	TIM6 supply current(1)	50	
$I_{DD(UART1)}$	LINUART supply current(2)	120	
$I_{DD(SPI)}$	SPI supply current(2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

Table 45. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

Table 46. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

Figure 24. Typ. V_{OL} @ V_{DD} = 5 V (true open drain ports)

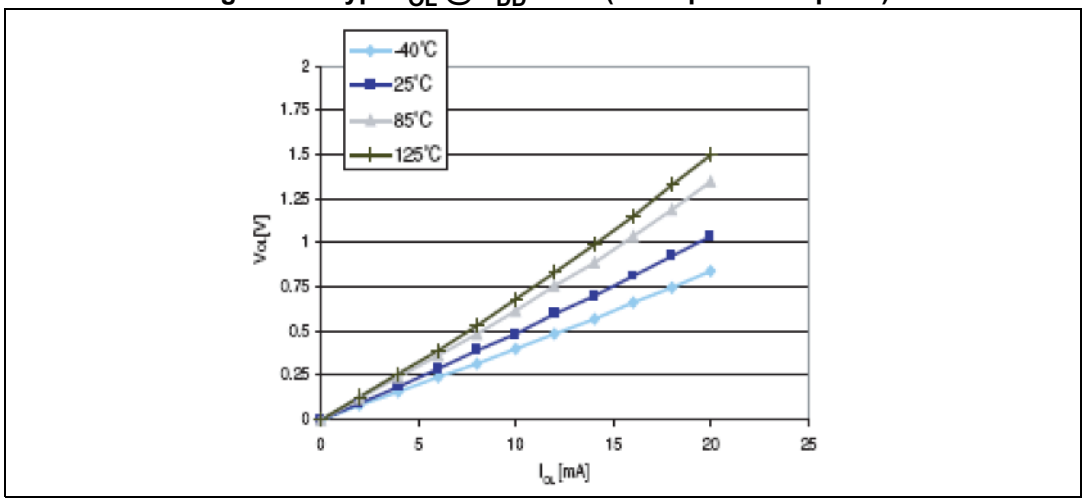


Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

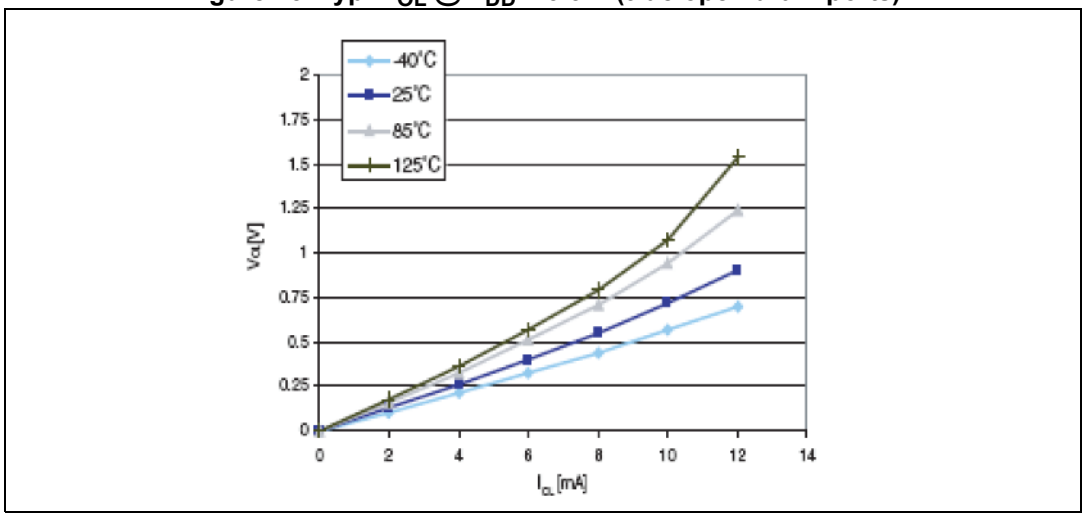
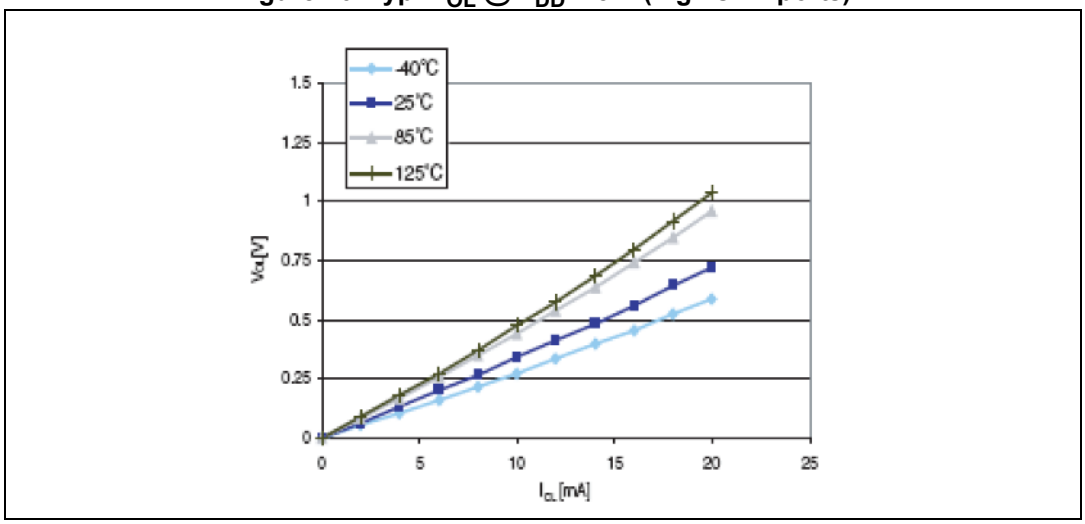


Figure 26. Typ. V_{OL} @ V_{DD} = 5 V (high sink ports)



9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD} = 3 to 5.5 V	1	-	4	MHz
		V_{DD} = 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 3 to 5.5 V	1.19(2)	1.22	1.25(2)	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7	-	
t_{CONV}	Minimum total conversion time including sampling time, 10-bit resolution	f_{ADC} = 4 Hz	3.5			µs
		f_{ADC} = 6 MHz	2.33			
		-	14			$1/f_{ADC}$

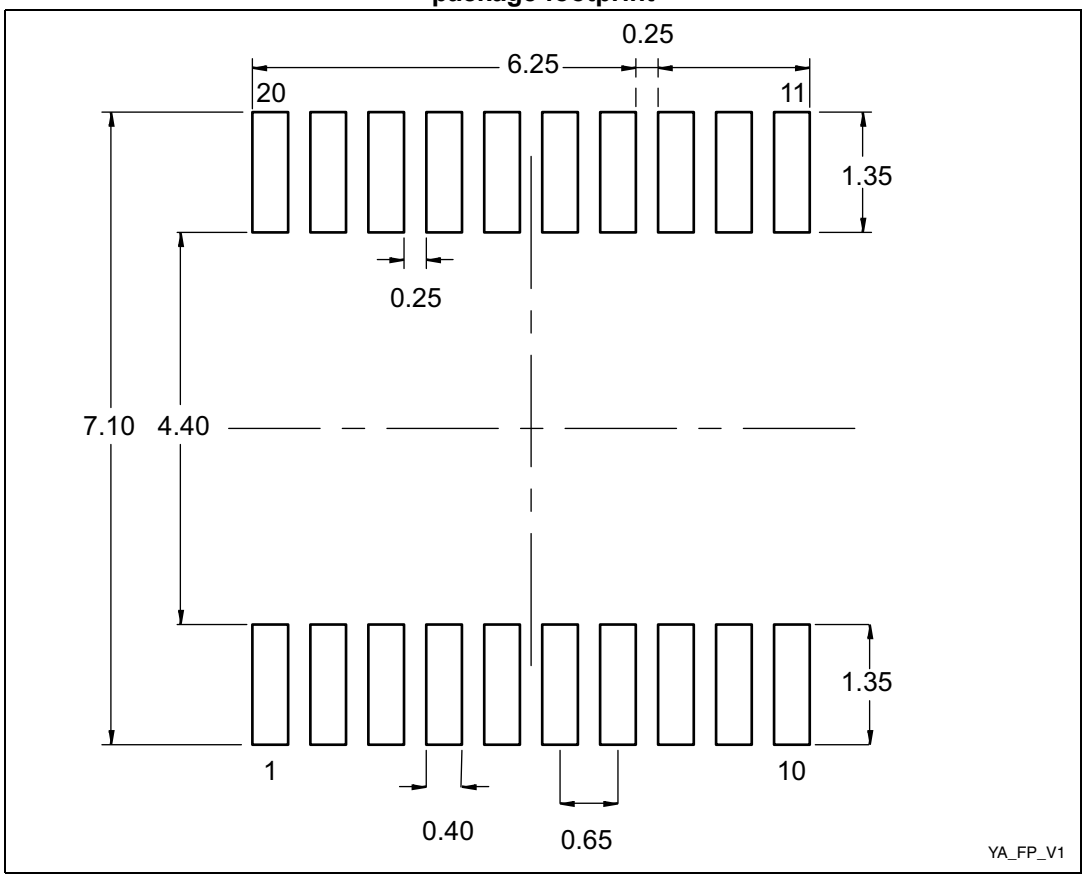
1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
2. Tested in production.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 46. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

11 Ordering information

Table 65. STM8AF6213/23/23A/26 ordering information scheme(1)

Example	STM8A	F	62	2	3	I	P	C	A	U

Product Class

8-bit automotive microcontroller

Program memory type

F = Flash + EEPROM

Device family

62 = LIN only

Program memory size

1 = 4 Kbyte
2 = 8 Kbyte

Pin count

3 = 20 pins
6 = 32 pins

HSI accuracy

Blank = ± 5%
I = ± 3%

Package type

T = LQFP
P = TSSOP
U = VFQFPN

Temperature range

A = -40 to 85 °C
C = -40 to 125 °C
D = -40 to 150 °C

Number of ADC analog inputs

Blank = 5 analog inputs
A = 7 analog inputs

Packing

Y = Tray
U = Tube
X = Tape and reel compliant with EIA 481-C

1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

12.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

Cosmic C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows the users to assemble and link your application source code.