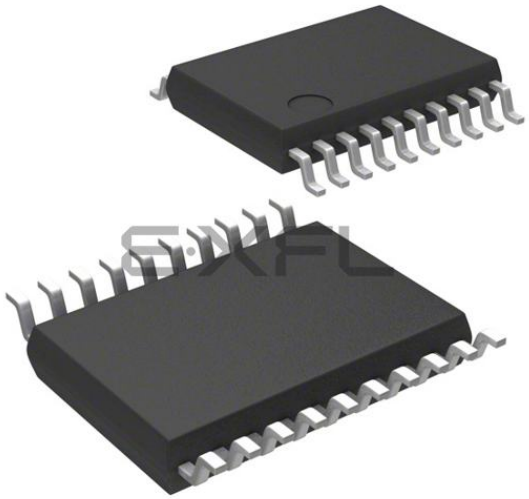


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6213pcx

List of tables

List of figures

2 Description

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 automotive 8-bit microcontrollers offer 4 to 8 Kbytes of Flash program memory, plus integrated true data EEPROM. The STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the-art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 kwrite/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8AF6213/23/23A/26 features

Device	STM8AF6226	STM8AF6223	STM8AF6223A	STM8AF6213
Pin count	32	20		
Max. number of GPIOs	28 including 21 high-sink I/Os	16 including 12 high-sink I/Os		
Ext. interrupt pins	28	16		
Timer CAPCOM channels	6	7	6	7
Timer complementary outputs	3	1	2	1
A/D converter channels	7	5	7	5
Low-density Flash program memory (byte)	8 K			4 K
Data EEPROM (byte)	640(1)			
RAM (byte)	1 K			
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, LINUART, window WDG, independent WDG, ADC, PWM timer (TIM5), 8-bit timer (TIM6)			

1. No read-while-write (RWW) capability

4 Product overview

The following section intends to give an overview of the basic features of the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

4.1 Central processing unit (CPU)

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

4.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

4.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

4.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

The IWDG time base spans from 60 µs to 1 s

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto-reload counter with 16-bit fractional prescaler.
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- Synchronization module to control the timer with external signals or to synchronise with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 Serial peripheral interface (SPI)

- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave /master selection input pin

4.14.3 Inter integrated circuit (I^2C) interface

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)

LQFP32 VFQPN32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
27	PD2/[AIN3] [TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1]
28	PD3/ AIN4/ TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4 Timer 52 - channel 2/ADC external trigger	-
29	PD4/ TIM5_CH1/ BEEP [LINUART_CK]	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 5 - channel 1/BEEP output	LINUART clock [AFR2]
30	PD5/ AIN5/ LINUART_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ LINUART data transmit	-
31	PD6/ AIN6/ LINUART_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ LINUART data receive	-
32	PD7/ TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 9.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB	Reserved area (1 byte)			
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 byte)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 byte)			

Table 13. Interrupt mapping (continued)

Priority	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Interrupt vector address
23	TIM6	TIM6 update/overflow/trigger	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068

1. Except PA1.

9 Electrical characteristics

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

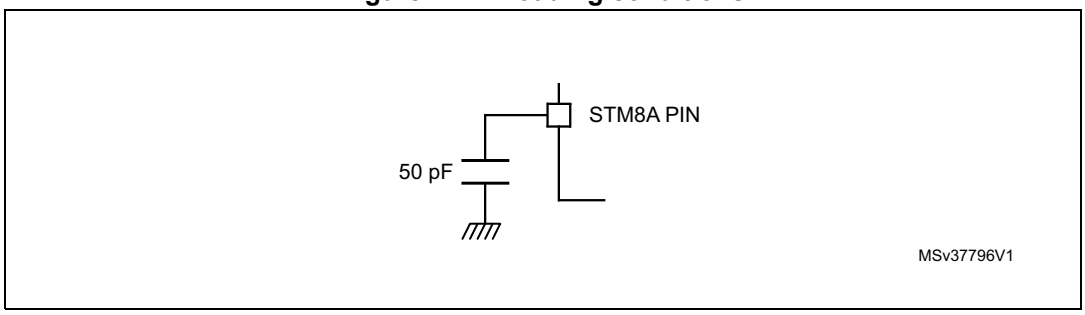
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

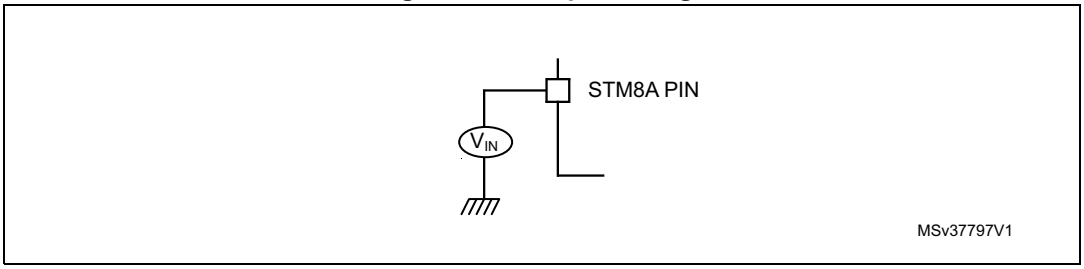
Figure 7. Pin loading conditions



9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 8. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics* and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 28. Total current consumption with code execution in run mode at V_{DD} = 5 V (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4.5	-	mA
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.7	4.5(1)	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	2(1)	
		$f_{CPU} = f_{MASTER}$/128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$/128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Tested in production.
2. Default clock configuration measured with all peripherals off.

Table 29. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ =16 MHz	HSE crystal osc. (16 MHz)	1.8	-	mA
			HSE user ext. clock (16 MHz)	2	2.3	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}$/128 = 125 kHz	HSE user ext. clock (16 MHz)	0.81	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$/ 128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ =128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4	-	
			HSE user ext. clock (16 MHz)	3.9	4.7	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ =2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$/ 128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$/128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ =128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

9.3.3 External clock sources and timing characteristics

HSE user external clock

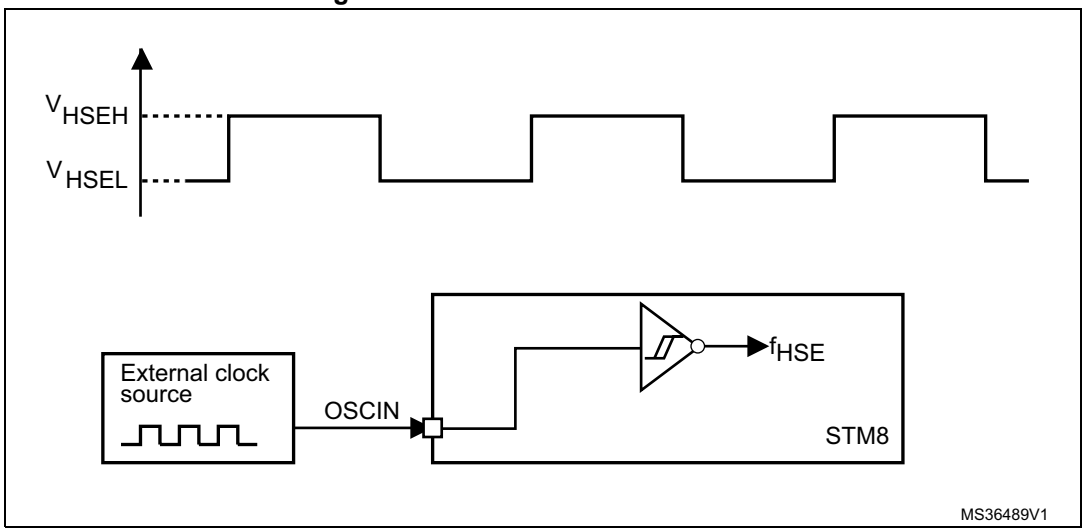
Subject to general operating conditions for V_{DD} and T_A.

Table 39. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	-	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. Guaranteed by characterization results.

Figure 17. HSE external clock source



9.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	-	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 32. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

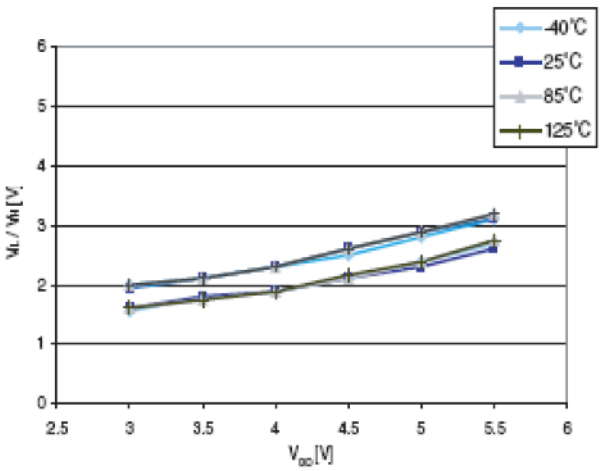
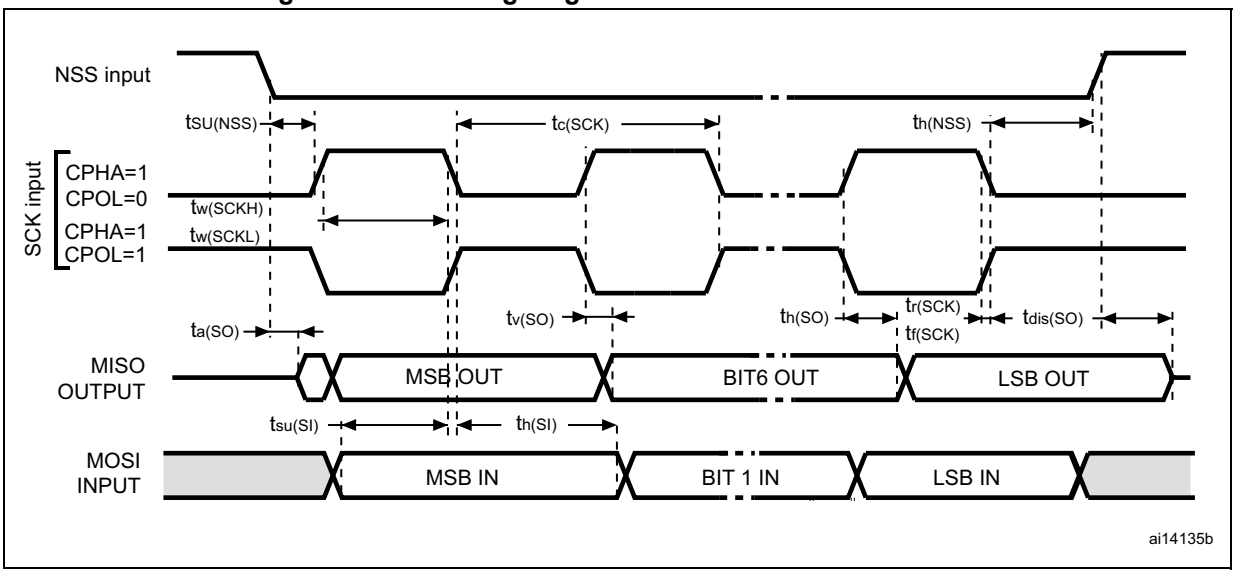
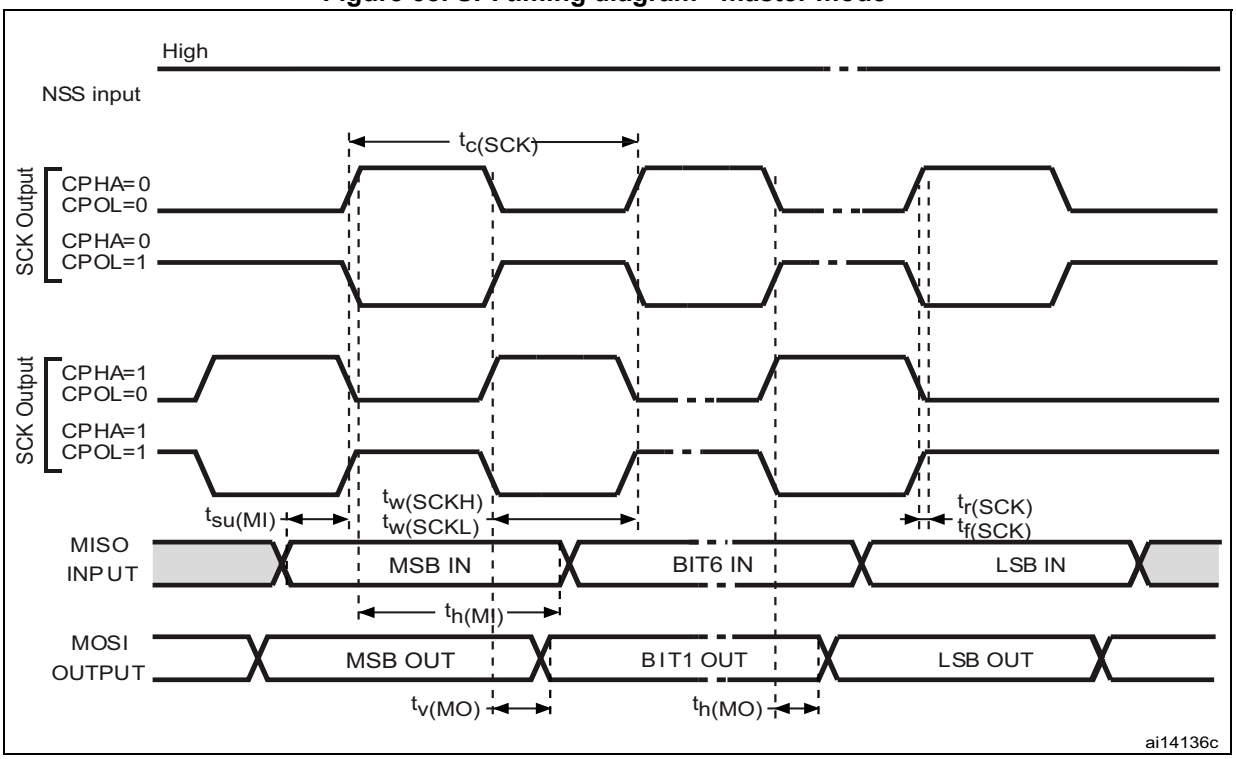


Figure 37. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram - master mode(1)



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

9.3.9 I²C interface characteristics

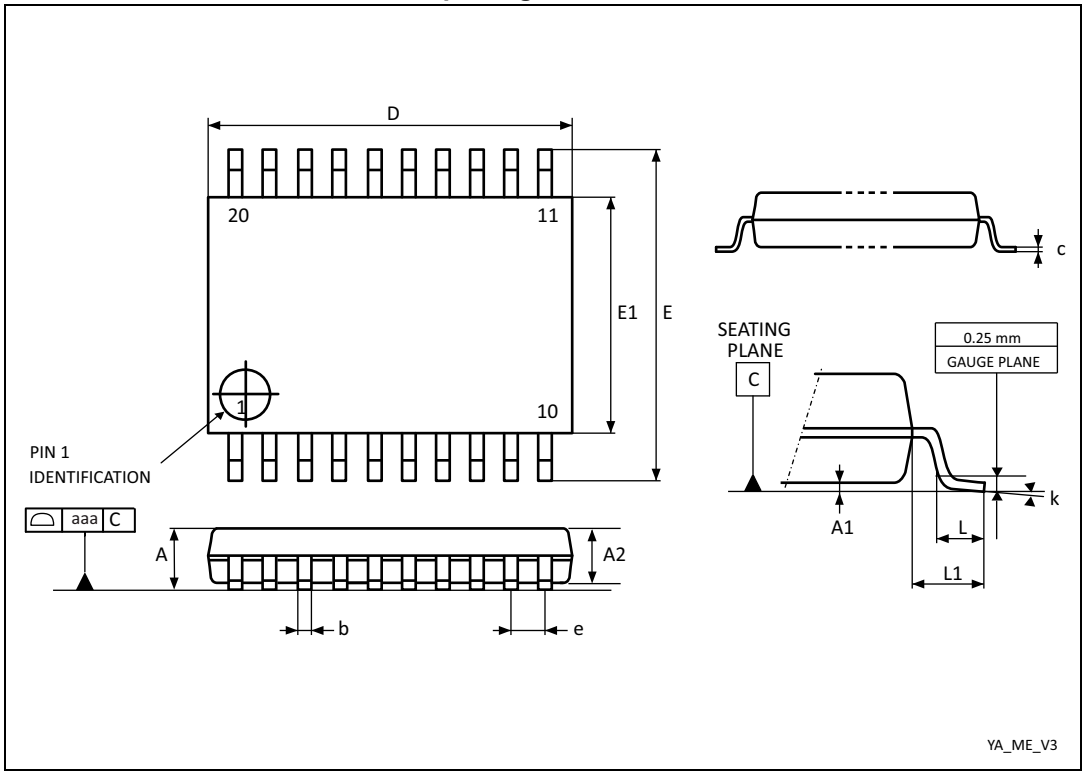
Table 53. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	3450	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
t_{SP}	Pulse width of spikes suppressed by the input filter	0	50(5)	0	50	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$

10.2 TSSOP20 package information

Figure 45.TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 75 °C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V

Maximum 20 I/Os used at the same time in output at low level with:
I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 8 mA x 5 V= 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

P_{Dmax} = 400 mW + 64 mW

Thus: P_{Dmax} = 464 mW.

Using the values obtained in *Table 64: Thermal characteristics on page 101* T_{Jmax} is calculated as follows:

For LQFP32 60 °C/W

T_{Jmax} = 75 °C + (60 °C/W x464 mW) = 75 °C + 27.8 °C = 102.8 °C

This is within the range of the suffix C version parts (-40 < T_J < 125 °C).

Parts must be ordered at least with the temperature range suffix C.

Table 66. Document revision history (continued)

Date	Revision	Changes
10-Jul-2014	4	Extended the applicability to STM8AF6213 devices. Updated the program memory feature, the power management, and the clock management features on the cover page. Added the table in *Section: Memory map*. Updated the *Figure: f_{CPUmax} versus V_{DD}* in *Section: Operating conditions.* Updated *Section: Ordering information*.
26-Jun-2015	5	Added: – the footnote about the inrush current below *Table 27: Operating conditions at power-up/power-down*, – *Figure 44: LQFP32 marking example (package top view)*, – *Figure 47: TSSOP20 marking example (package top view)*. Updated – LIN standard version, – the register label for LINUART block in *Table 11: General hardware register map*, – the power dissipation in *Table 26: General operating conditions*, – *Table 41: HSI oscillator characteristics* for HSI oscillator accuracy, – the standard for EMI in *Electromagnetic interference (EMI)*, – *Figure 48: STM8AF6213/23/23A/26 ordering information scheme*(1) (2) to add HSI accuracy. Moved *Section 10.4: Thermal characteristics* to *Section 10: Package information*.
28-Mar-2017	6	Updated *Table 6: STM8AF6213/STM8AF6223 TSSOP20 pin description* Added VFQFPN32 (5x5 mm) package information updating: – *Section : Features* on the cover page: added VFQFPN32 (5x5 mm) figure – Added *Section 10.3: VFQFPN32 package information*: – Updated *Table 26: General operating conditions* – Updated *Table 64: Thermal characteristics* – Updated *Section 5.2: LQFP32/VFQPN32 pinout and pin description* – Updated *Section 11: Ordering information* Additional updates (not related to VFQFPN32): – Table footnotes on *Section 9: Electrical characteristics* – Updated *Section : Device marking on page 93*, *Section : Device marking on page 96* and *Section : Device marking on page 100* – *Section 9.2: Absolute maximum ratings*