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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6213pdu

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## 3 Block diagram





 Legend: ADC (Analog-to-digital converter), beCAN (Controller area network), BOR (Brownout reset), I<sup>2</sup>C (Inter-integrated circuit multimaster interface),IWDG (Independent window watchdog), LINUART (Local interconnect network universal asynchronous receiver transmitter), POR (Power on reset), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), Window WDG (Window watchdog).



#### STM8AF6213/23/23A/26

[LINUART_CK] TIM5_CH1/BEEP/(HS) PD4	20 PD3 (HS)/AIN4/TIM5_CH2/ADC_ETR
AIN5/LINUART_TX/(HS) PD5 🚺 2	19 ] PD2 (HS)/AIN3 [TIM5_CH3]
AIN6/LINUART_RX/(HS) PD6 🛙 3	18 ] PD1 (HS)/SWIM
NRST 4	17 ] PC7 (HS)/SPI_MISO [TIM1_CH2]
OSCIN/PA1 🕻 5	16 DPC6 (HS)/SPI_MOSI [TIM1_CH1]
	15 <b>]</b> PC5 (HS)/SPI_SCK [TIM5_CH1]
VSS 🕻 7	14 PC4 (HS)/TIM1_CH4/CLK_CCO/AIN2 [TIM1_CH2N]
VCAP 🕻 8	13 DPB0 (HS)/TIM1_CH1N/AIN0
VDD 🛛 9	12 PB1 (HS)/TIM1_CH2N/AIN1
[TIM5_BKIN] I2C_SDA/(T) PB5 🕻 10	11 D PB4 (T)/I2C_SCL [ADC_ETR]
	MS38346V1

#### Figure 4. STM8AF6223A TSSOP20 pinout

1. (HS) high sink capability.

2. (T) true open drain (P-buffer and protection diode to  $V_{\text{DD}}$  not implemented).

3. [] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

				Input	t		Out	put					
TSSOP	Pin name	Туре	floating	ndw	Ext. interrupt	High sink <sup>(1)</sup>	Speed	QD	ЬР	Main function (after reset)	Default alternate function	Alternate function after remap [option bit]	
1	PD4/ TIM5_CH1/ BEEP [LINUART_CK]	I/O	x	x	х	HS	O3	х	x	Port D4	Timer 5 - channel 1/BEEP output	LINUART clock [AFR2]	
2	PD5/ AIN5/ LINUART_TX	I/O	X	x	x	HS	O3	x	x	Port D5	Analog input 5/ LINUART data transmit	-	
3	PD6/ AIN6/ LINUART_RX	I/O	x	x	х	HS	O3	х	x	Port D6 Analog input 6/ LINUART data receive		-	
4	NRST	I/O	-	<u>X</u>	-	-	-	-	-		Reset		
5	PA1/ OSCIN <sup>(2)</sup>	I/O	x	х	х	-	01	х	х	Port A1	Resonator/ crystal in	-	
6	PA2/ OSCOUT	I/O	x	х	х	01	х	х		Port A2	Resonator/ crystal out	-	
7	VSS	S	-	-	-	-	-	-	-	Digital ground			
8	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor			
9	VDD	S	-	-	-	-	-	-	-	Dig	ital power sup	oply	

#### Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description



Address	Block	Register label	Register name	Reset status			
0x00 5200		SPI_CR1	SPI control register 1	0x00			
0x00 5201		SPI_CR2	SPI control register 2	0x00			
0x00 5202		SPI_ICR	SPI interrupt control register	0x00			
0x00 5203	SPI	SPI_SR	SPI status register	0x02			
0x00 5204		SPI_DR	SPI data register	0x00			
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07			
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF			
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF			
0x00 5208 to 0x00 520F	Reserved area (8 byte)						
0x00 5210		I2C_CR1	I2C control register 1	0x00			
0x00 5211		I2C_CR2	I2C control register 2	0x00			
0x00 5212		I2C_FREQR	I2C frequency register	0x00			
0x00 5213		I2C_OARL	I2C own address register low	0x00			
0x00 5214		I2C_OARH	I2C own address register high	0x00			
0x00 5215			Reserved area (1 byte)				
0x00 5216		I2C_DR	I2C data register	0x00			
0x00 5217	I2C	I2C_SR1	I2C status register 1	0x00			
0x00 5218		I2C_SR2	I2C status register 2	0x00			
0x00 5219		I2C_SR3	I2C status register 3	0x00			
0x00 521A		I2C_ITR	I2C interrupt control register	0x00			
0x00 521B		I2C_CCRL	I2C clock control register low	0x00			
0x00 521C		I2C_CCRH	I2C clock control register high	0x00			
0x00 521D		I2C_TRISER	I2C TRISE register	0x02			
0x00 521E		I2C_PECR	I2C packet error checking register	0x00			
0x00 521F to 0x00 522F		Reserved area (17 byte)					

 Table 11. General hardware register map (continued)



Address	Block	Register label	Register name	Reset status		
0x00 5230		UART4_SR	LINUART status register	0xC0		
0x00 5231	•	UART4_DR	LINUART data register	0xXX		
0x00 5232		UART4_BRR1	LINUART baud rate register 1	0x00		
0x00 5233		UART4_BRR2	LINUART baud rate register 2	0x00		
0x00 5234		UART4_CR1	LINUART control register 1	0x00		
0x00 5235		UART4_CR2	LINUART control register 2	0x00		
0x00 5236	LINUARI	UART4_CR3	LINUART control register 3	0x00		
0x00 5237		UART4_CR4	LINUART control register 4	0x00		
0x00 5238			Reserved			
0x00 5239		UART4_CR6	LINUART control register 6	0x00		
0x00 523A		UART4_GTR	LINUART guard time register	0x00		
0x00 523B		UART4_PSCR	LINUART prescaler	0x00		
0x00 523C to 0x00 523F	Reserved area (20 byte)					

Table 11	General	hardware	register	man	(continued)
	General	naiuwaie	register	map	(continueu)



Option byte number	Description <sup>(1)</sup>
OPT2	<ul> <li>AFR7: Alternate function remapping option 7 <ol> <li>AFR7 remapping option inactive: default alternate function <sup>(2)</sup></li> <li>Port C3 alternate function = TIM1_CH1N;</li> <li>port C4 alternate function = TIM1_CH2N</li> </ol> </li> <li>AFR6: Alternate function remapping option 6 Reserved AFR5: Alternate function remapping option 5 Reserved AFR4: Alternate function remapping option 4 <ol> <li>AFR4: Alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.</li> </ol> AFR3: Alternate function remapping option 3 <ol> <li>AFR3: Alternate function remapping option 2</li> <li>AFR2: Alternate function remapping option 2</li> <li>AFR2: remapping option inactive: default alternate function <sup>(2)</sup></li> </ol> </li> </ul>

## Table 17. STM8AF6213 and STM8AF6223 alternate function remapping bits [7:2] for 20-pin packages

1. Do not use more than one remapping option in the same port.

2. Refer to the pin description.

#### Table 18. STM8AF6223A alternate function remapping bits [7:2] for 20-pin packages

Option byte number	Description <sup>(1)</sup>
OPT2	<ul> <li>AFR7: Alternate function remapping option 7 <ul> <li>0: AFR7 remapping option inactive: default alternate function <sup>(2)</sup></li> <li>1: Port C4 alternate function = TIM1_CH2N</li> </ul> </li> <li>AFR6: Alternate function remapping option 6 <ul> <li>Reserved</li> </ul> </li> <li>AFR5: Alternate function remapping option 5 <ul> <li>Reserved</li> </ul> </li> <li>AFR4: Alternate function remapping option 4 <ul> <li>0: AFR4 remapping option inactive: default alternate function <sup>(2)</sup></li> <li>1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.</li> </ul> </li> <li>AFR3: Alternate function remapping option 3 <ul> <li>Reserved.</li> </ul> </li> <li>AFR2: Alternate function remapping option 2 <ul> <li>0: AFR2 remapping option inactive: default alternate function <sup>(2)</sup></li> <li>1: Port D4 alternate function remapping option 2</li> <li>1: Port D4 alternate function = LINUART_CK</li> </ul> </li> </ul>

1. Do not use more than one remapping option in the same port.

2. Refer to the pin description.



#### **Current consumption curves**

The following figures show typical current consumption measured with code executing in RAM.



Figure 11. Typ I<sub>DD(RUN)</sub> vs. V<sub>DD</sub> HSE user external clock, f<sub>CPU</sub> = 16 MHz

Figure 12. Typ  $I_{DD(RUN)}$  vs.  $f_{CPU}$  HSE user external clock,  $V_{DD}$  = 5 V





### 9.3.6 I/O port pin characteristics

#### **General characteristics**

Subject to general operating conditions for  $V_{DD}$  and  $T_A$  unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V <sub>IL</sub>	Input low level voltage		-0.3 V	-	0.3 x V <sub>DD</sub>	
V <sub>IH</sub>	Input high level voltage	-	0.7 x V <sub>DD</sub>	-	V <sub>DD</sub> + 0.3 V	V
V <sub>hys</sub>	Hysteresis <sup>(1)</sup>		-	700	-	mV
R <sub>pu</sub>	Pull-up resistor	$V_{DD}$ = 5 V, $V_{IN}$ = $V_{SS}$	35	55	80	kΩ
t <sub>R</sub> , t <sub>F</sub>		Fast I/Os Load = 50 pF	-	-	35 <sup>(2)</sup>	
	Rise and fall time (10% - 90%)	Standard and high sink I/Os Load = 50 pF	-	-	125 <sup>(2)</sup>	20
		Fast I/Os Load = 20 pF			20 <sup>(2)</sup>	115
		Standard and high sink I/Os Load = 20 pF			50 <sup>(2)</sup>	
I <sub>lkg</sub>	Digital input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1 <sup>(3)</sup>	μA
l <sub>Ikg ana</sub>	Analog input pad leakage	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> -40 °C < T <sub>A</sub> < 125 °C	-	-	±250 <sup>(3)</sup>	۳A
	current	$V_{SS} \le V_{IN} \le V_{DD}$ -40 °C < T <sub>A</sub> < 150 °C	-	-	±500 <sup>(3)</sup>	nΑ
l <sub>lkg(inj)</sub>	Leakage current in adjacent I/O <sup>(2)</sup>	Injection current ±4 mA	-	-	±1 <sup>(3)</sup>	μA

Table 47	I/O static	characteristics
	I/O Static	Characteristics

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

2. Guaranteed by characterization results.

3. Guaranteed by design.





Figure 24. Typ. V<sub>OL</sub> @ V<sub>DD</sub> = 5 V (true open drain ports)

Figure 25. Typ.  $V_{OL}$  @  $V_{DD}$  = 3.3 V (true open drain ports)



## Figure 26. Typ. V<sub>OL</sub> @ V<sub>DD</sub> = 5 V (high sink ports)





### 9.3.7 Reset pin characteristics

Subject to general operating conditions for  $V_{\text{DD}}$  and  $T_{\text{A}}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V <sub>IL(NRST)</sub>	NRST input low level voltage <sup>(1)</sup>	-	-0.3	-	$0.3 \times V_{DD}$	
V <sub>IH(NRST)</sub>	NRST input high level voltage <sup>(1)</sup>	I <sub>OL</sub> = 2 mA	0.7 x V <sub>DD</sub>	-	V <sub>DD</sub> + 0.3	V
V <sub>OL(NRST)</sub>	NRST output low level voltage <sup>(1)</sup>	-	-	-	0.5	
R <sub>PU(NRST)</sub>	NRST pull-up resistor <sup>(2)</sup>	-	30	55	80	kΩ
t <sub>IFP(NRST)</sub>	NRST input filtered pulse <sup>(3)</sup>	-	-	-	75	
t <sub>INFP(NRST)</sub>	NRST Input not filtered pulse duration <sup>(3)</sup>	-	500	-	-	ns
t <sub>OP(NRST)</sub>	NRST output pulse <sup>(3)</sup>	-	20	-	-	μs

Table	51.	NRST	pin	characteristics
10010	••••		P	01101000100100

1. Guaranteed by characterization results.

2. The R<sub>PU</sub> pull-up equivalent resistor is based on a resistive transistor.

3. Guaranteed by design.





Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Max	Unit
t <sub>h(SO)</sub> <sup>(2)</sup>	Data output hold time	Slave mode (after enable edge)	27	-	ne
t <sub>h(MO)</sub> <sup>(2)</sup>		Master mode (after enable edge)	11	-	611

#### Table 52. SPI characteristics (continued)

1. Parameters are given by selecting 10 MHz I/O output frequency.

2. Values based on design simulation and/or characterization results, and not tested in production.

3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.



#### Figure 36. SPI timing diagram - slave mode and CPHA = 0

1. Measurement points are made at CMOS levels: 0.3  $V_{\text{DD}}$  and 0.7  $V_{\text{DD}}$ 



Symbol	Parameter	Conditions	Тур	Max <sup>(1)</sup>	Unit	
		f <sub>ADC</sub> = 2 MHz	1.6	3.5		
E <sub>T</sub>	Total unadjusted error <sup>(2)</sup>	f <sub>ADC</sub> = 4 MHz	2.2	4		
		f <sub>ADC</sub> = 6 MHz	2.4	4.5		
		f <sub>ADC</sub> = 2 MHz	1.1	2.5		
E <sub>O</sub>	Offset error <sup>(2)</sup>	f <sub>ADC</sub> = 4 MHz	1.5	3		
		f <sub>ADC</sub> = 6 MHz	1.8	3		
E <sub>G</sub>	Gain error <sup>(2)</sup>	f <sub>ADC</sub> = 2 MHz	1.5	3		
		f <sub>ADC</sub> = 4 MHz	2.1	3	LSB	
		f <sub>ADC</sub> = 6 MHz	2.2	4		
		f <sub>ADC</sub> = 2 MHz	0.7	1.5		
E <sub>D</sub>	Differential linearity error <sup>(2)</sup>	f <sub>ADC</sub> = 4 MHz	0.7	1.5		
		f <sub>ADC</sub> = 6 MHz	0.7	1.5		
E <sub>L</sub>		f <sub>ADC</sub> = 2 MHz	0.6	1.5		
	Integral linearity error <sup>(2)</sup>	f <sub>ADC</sub> = 4 MHz	0.8	2		
		f <sub>ADC</sub> = 6 MHz	0.8	2		

Table 55. ADC accuracy with RAIN < 10 k $\Omega$ , V<sub>DD</sub> = 5 V

1. Max value is based on characterization, not tested in production.

2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in the I/O port pin characteristics section does not affect the ADC accuracy.

Symbol	Parameter	Conditions	Тур	Max <sup>(1)</sup>	Unit
E <sub>T</sub>	Total upadjusted error	f <sub>ADC</sub> = 2 MHz	1.6	3.5	
		f <sub>ADC</sub> = 4 MHz	1.9	4	
E <sub>O</sub>   Offse	Offeet error	f <sub>ADC</sub> = 2 MHz	1	2.5	
	Oliset end	f <sub>ADC</sub> = 4 MHz	1.5	2.5	
E <sub>G</sub>	Gain error	f <sub>ADC</sub> = 2 MHz	1.3	3	
		f <sub>ADC</sub> = 4 MHz	2	3	LOB
E <sub>D</sub>	Differential linearity error	f <sub>ADC</sub> = 2 MHz	0.7	1	
		f <sub>ADC</sub> = 4 MHz	0.7	1.5	
E <sub>L</sub>	Integral linearity error	f <sub>ADC</sub> = 2 MHz	0.6	1.5	
	Integral linearity error	f <sub>ADC</sub> = 4 MHz	0.8	2	

Table 56. ADC accuracy with RAIN < 10 k $\Omega$ , V<sub>DD</sub> = 3.3 V

1. Max value is based on characterization, not tested in production.







- 1. Example of an actual transfer curve
- 2. The ideal transfer curve
- 3.

End point correlation line  $E_T$  = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.  $E_0$  = Offset error: Deviation between the first actual transition and the first ideal one.  $E_G$  = Gain error: Deviation between the last ideal transition and the last actual one.  $E_D$  = Differential linearity error: Maximum deviation between actual steps and the ideal one.  $E_L$  = Integral linearity error: Maximum deviation between any actual transition and the end point correlation between any actual transition and the end point correlation line.





1. Legend: RAIN = external resistance, CAIN = capacitors, Csamp = internal sample and hold capacitor.



#### **Electromagnetic interference (EMI)**

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Symbol		Conditions				
	Parameter	General conditions	Monitored	Max f <sub>HS</sub>	Unit	
			frequency band	16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S <sub>EMI</sub> Peak level EMI level		$V_{DD} = 5 V,$ $T_A = 25 °C,$	0.1 MHz to 30 MHz	5	5	
	Peak level T <sub>A</sub> =		30 MHz to 130 MHz	4	5	dBµV
		conforming to	130 MHz to 1 GHz	5	5	
	EMI level	IEC 61967-2	_	2.5	2.5	level

Table 58. EMI d	lata
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1. Guaranteed by characterization results.

#### Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

#### Electrostatic discharge (ESD)

Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts\*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (Human body model)	$T_A = 25^{\circ}C$ , conforming to JESD22-A114	ЗA	4000	
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (Charge device model)	$T_A = 25^{\circ}C$ , conforming to JESD22-C101	3	500	V
V <sub>ESD(MM)</sub>	Electrostatic discharge voltage (Machine model)	T <sub>A</sub> = 25°C, conforming to JESD22-A115	В	200	

Table 59. ESD absolute maximum ratings

1. Guaranteed by characterization results.



## **10** Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK<sup>®</sup> is an ST trademark.

## 10.1 LQFP32 package information



Figure 42. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline

1. Drawing is not to scale.



## 10.2 TSSOP20 package information





1. Drawing is not to scale.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch,
package mechanical data

Sympol		millimeters			inches <sup>(1)</sup>	
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.
А	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
С	0.090	-	0.200	0.0035	-	0.0079
D <sup>(2)</sup>	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1 <sup>(3)</sup>	4.300	4.400	4.500	0.1693	0.1732	0.1772
е	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	_	0.0394	_



## 10.3 VFQFPN32 package information

Figure 48. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



1. Drawing is not to scale.

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