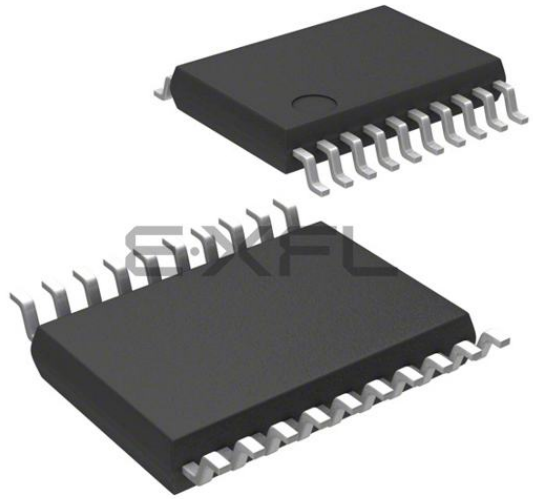

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6223ipcu

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module together with an integrated debug module permit non-intrusive, real-time in-circuit debugging and fast memory programming.

4.2.1 SWIM

Single wire interface module for direct access to the debug mode and memory programming. The interface can be activated in all device operation modes.The maximum data transmission speed is 145 byte/ms.

4.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined breakpoint configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 28 external interrupts on 7 vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- Up to 8 Kbytes of Flash program single voltage Flash memory
- 640 byte true data EEPROM
- User option byte area

4.4.1 Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option byte.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option byte.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

4.13 Analog-to-digital converter (ADC1)

The STM8AF6213, STM8AF6223, STM8AF6223A and STM8AF6226 products contain a 10-bit successive approximation A/D converter (ADC1) with up to 7 external and 1 internal multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DD}
- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Internal reference voltage on channel AIN7
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

Note: Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

Internal bandgap reference voltage

Channel AIN7 is internally connected to the internal bandgap reference voltage. The internal bandgap reference is constant and can be used, for example, to monitor V_{DD}. It is independent of variations in V_{DD} and ambient temperature T_A.

4.14 Communication interfaces

The following communication interfaces are implemented:

- LINUART: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.2 capability
- SPI: full and half-duplex, 8 Mbit/s
- I²C: up to 400 Kbit/s

Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016 (see *Table 4*).

Table 4. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
LINUART	UART4

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 Serial peripheral interface (SPI)

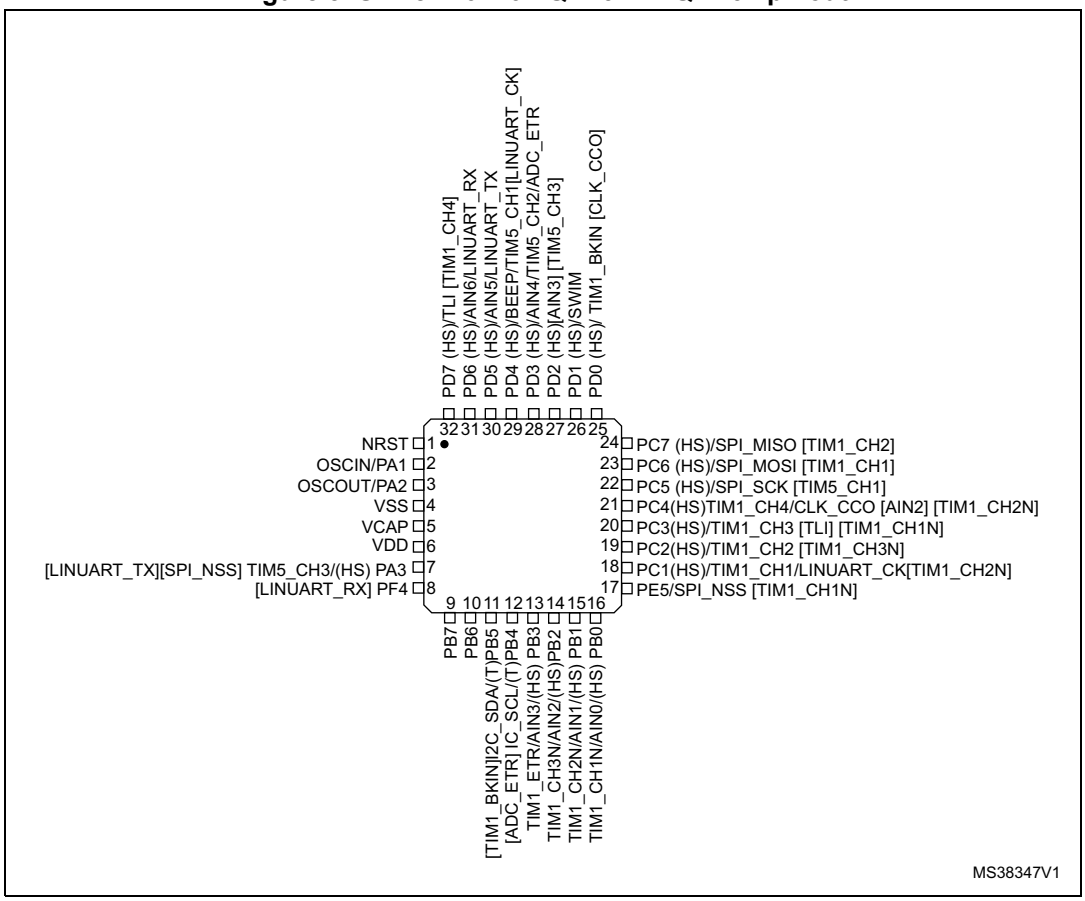
- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave /master selection input pin

4.14.3 Inter integrated circuit (I^2C) interface

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

5.2 LQFP32/VFQPN32 pinout and pin description

Figure 5. STM8AF6226 LQFP32/VFQPN32 pinout



1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 8. STM8AF6226 LQFP32/VFQPN32 pin description

LQFP32 VFQPN32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-

6 Memory and register map

6.1 Memory map

Figure 6. Memory map

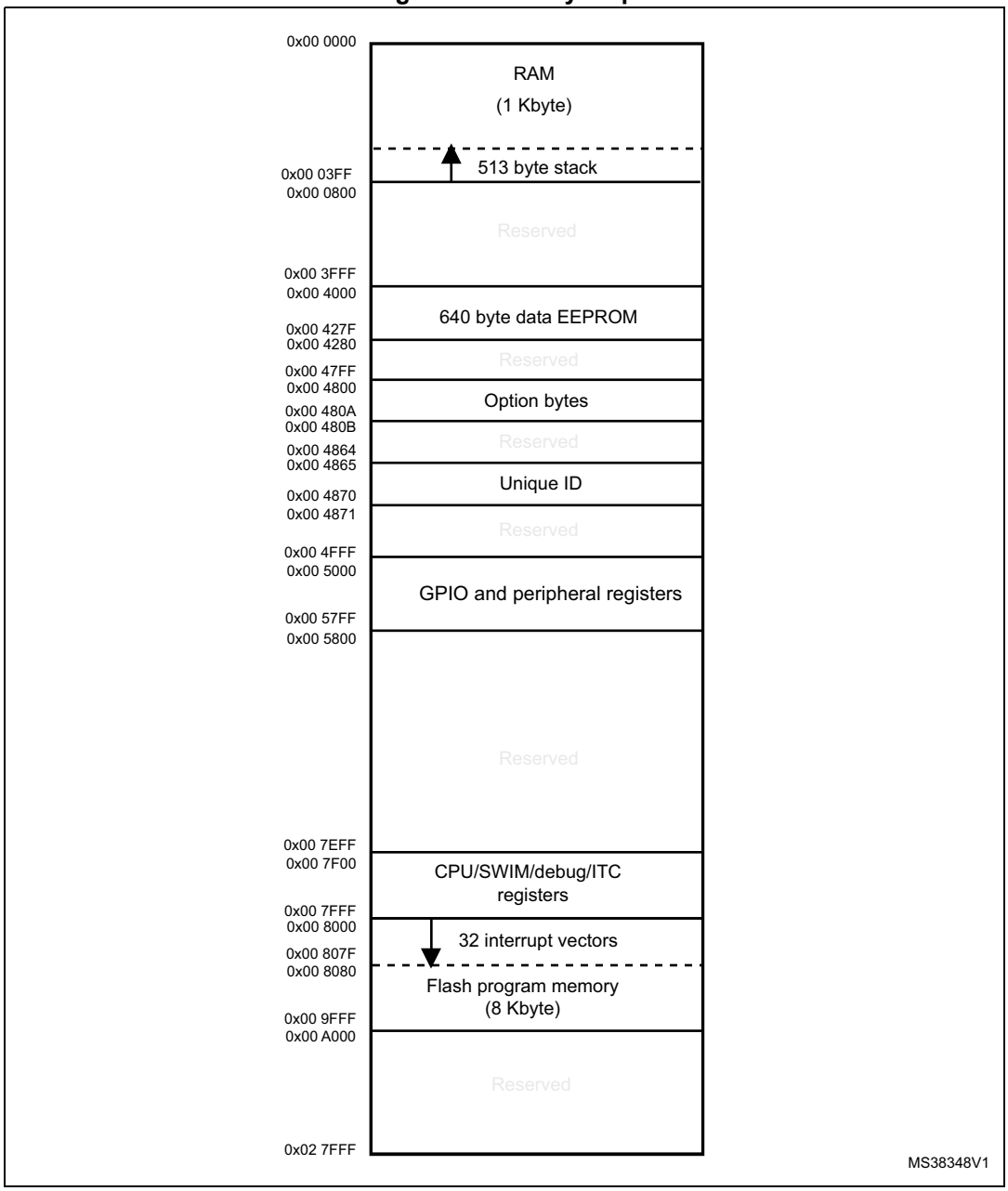


Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

Table 19. STM8AF6226 alternate function remapping bits [1:0] for 32-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3
1(2)	1(2)	PD2	TIM5_CH3
		PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
		PC2	TIM1_CH3N
		PC1	TIM1_CH2N
		PE5	TIM1_CH1N
		PA3	LINUART_TX
		PF4	LINUART_RX

1. Refer to the pin descriptions.
2. If both AFR1 and AFR0 option bits are set, the SPI hardware NSS management feature is no more available. If this remapping option is selected and the SPI is enabled, the SSM bit must be configured in the SPI_CR2 register to select software NSS management.

Table 20. STM8AF6213/STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3

Table 20. STM8AF6213/STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages (continued)

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
1	1	PD2	TIM5_CH3
		PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
		PC2	Not available
		PC1	Not available
		PE5	Not available
		PA3	SPI_NSS
		PF4	Not available

1. Refer to the pin descriptions.

Table 21. STM8AF6223A alternate function remapping bits [1:0] for 20-pin packages

AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	Not available
		PD2	TIM5_CH3
1(2)	1(2)	PD2	TIM5_CH3
		PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
		PC2	Not available
		PC1	Not available
		PE5	Not available
		PA3	Not available
		PF4	Not available

1. Refer to the pin descriptions.
2. If both AFR1 and AFR0 option bits are set, the SPI hardware NSS management feature is no more available. If this remapping option is selected and the SPI is enabled, the SSM bit must be configured in the SPI_CR2 register to select software NSS management.

9.3 Operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D (3)	Power dissipation at T_A = 85 °C for suffix A version, T_A = 125 °C for suffix C version, T_A = 150 °C for suffix D version	TSSOP20	-	45	mW
		LQFP32	-	83	
		VQFPN32	-	TBD	-
T_A	Ambient temperature for suffix A version	Maximum power dissipation	-40	85	°C
	Ambient temperature for suffix C version		-40	125	
	Ambient temperature for suffix D version		-40	150	
T_J	Junction temperature range	Suffix A	-40	90	
		Suffix C	-40	130	
		Suffix D	-40	155	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. See *Section 10.4: Thermal characteristics*.

Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 42. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110(1)	128	150(1)	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7	µs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	5	-	µA

1. Tested in production.

9.3.5 Memory characteristics

RAM and hardware registers

Table 43. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing the data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design.
2. Refer to the operating conditions for the value of V_{IT-max}

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 150 °C.

Table 44. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
	Operating voltage (code execution)		2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte)	-	-	6.0	6.6	ms
	Fast programming time for 1 block (64 byte)	-	-	3.0	3.3	
t_{ERASE}	Erase time for 1 block (64 byte)	-	-	3.0	3.3	

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 47. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-	-0.3 V	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	35	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
		Fast I/Os Load = 20 pF			20(2)	
		Standard and high sink I/Os Load = 20 pF			50(2)	
I_{lkg}	Digital input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1(3)	µA
$I_{lkg\ ana}$	Analog input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 125 °C	-	-	±250(3)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 150 °C	-	-	±500(3)	
$I_{lkg(inj)}$	Leakage current in adjacent I/O(2)	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 21. Typical pull-up current I_{pu} vs V_{DD} @ 4 temperatures

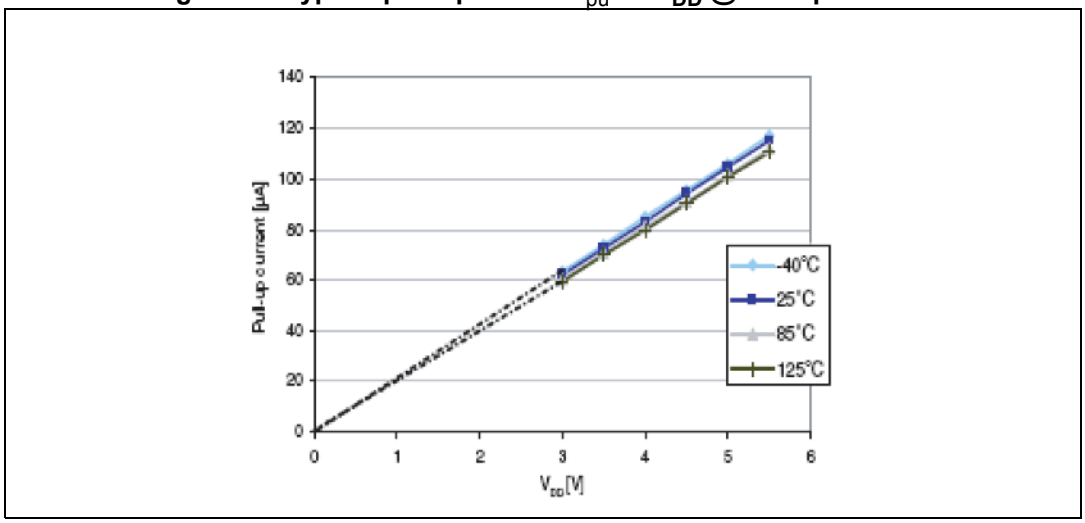


Table 48. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO} = 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Guaranteed by characterization results.

Table 49. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	1.0	V
		I_{IO} = 10 mA, V_{DD} = 3.3 V	1.5(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V	2.0(1)	

1. Guaranteed by characterization results.

Table 50. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V		1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
		I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Guaranteed by characterization results.

Figure 22. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

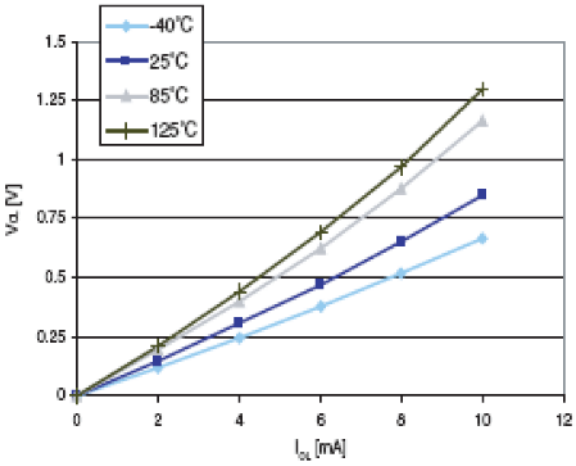
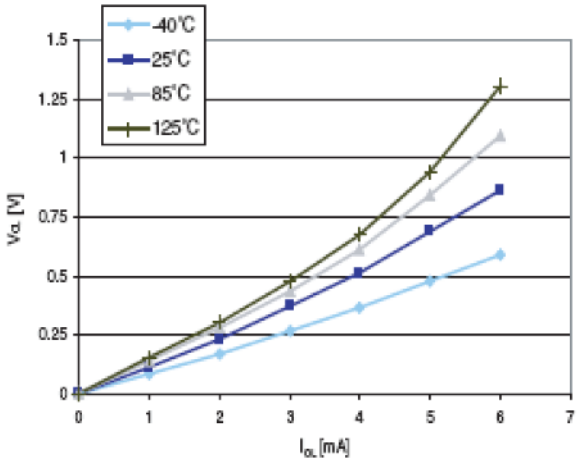


Figure 23. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)



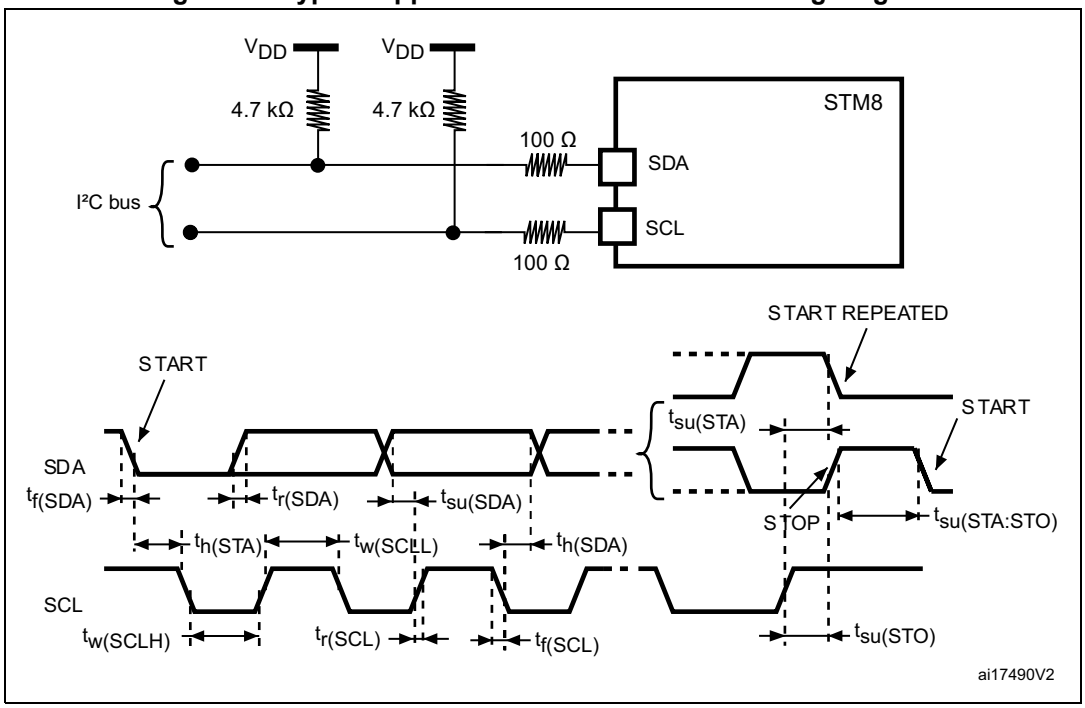
9.3.9 I²C interface characteristics

Table 53. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	3450	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
t_{SP}	Pulse width of spikes suppressed by the input filter	0	50(5)	0	50	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$

Figure 39. Typical application with I2C bus and timing diagram



1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD} = 3 to 5.5 V	1	-	4	MHz
		V_{DD} = 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 3 to 5.5 V	1.19(2)	1.22	1.25(2)	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7	-	
t_{CONV}	Minimum total conversion time including sampling time, 10-bit resolution	f_{ADC} = 4 Hz	3.5			µs
		f_{ADC} = 6 MHz	2.33			
		-	14			$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
2. Tested in production.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 58. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		—	2.5	2.5	level

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

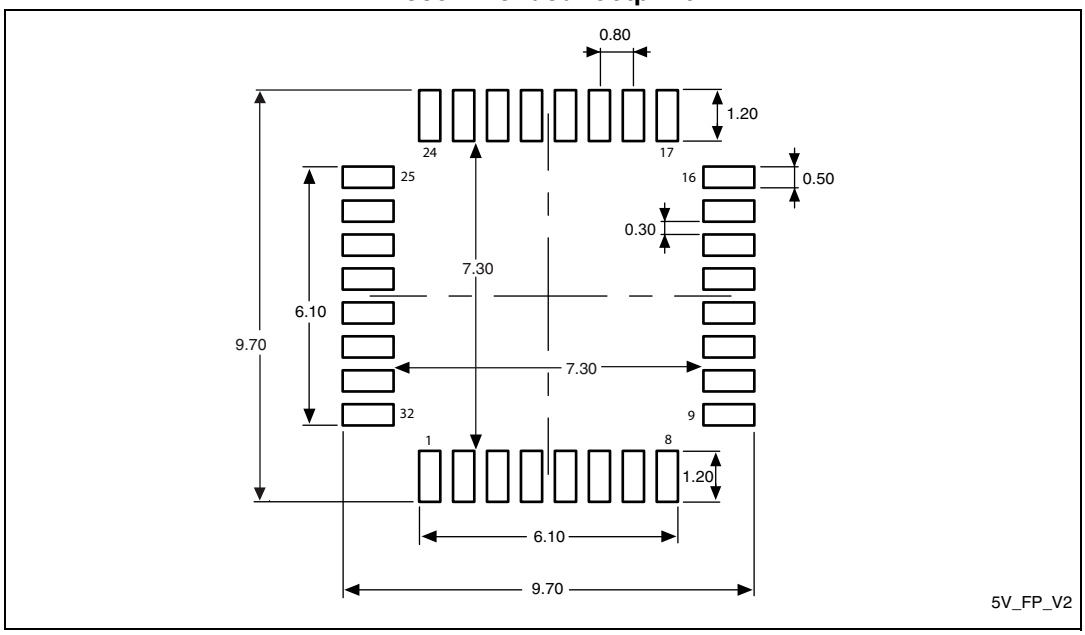
Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 59. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Guaranteed by characterization results.

Figure 43. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

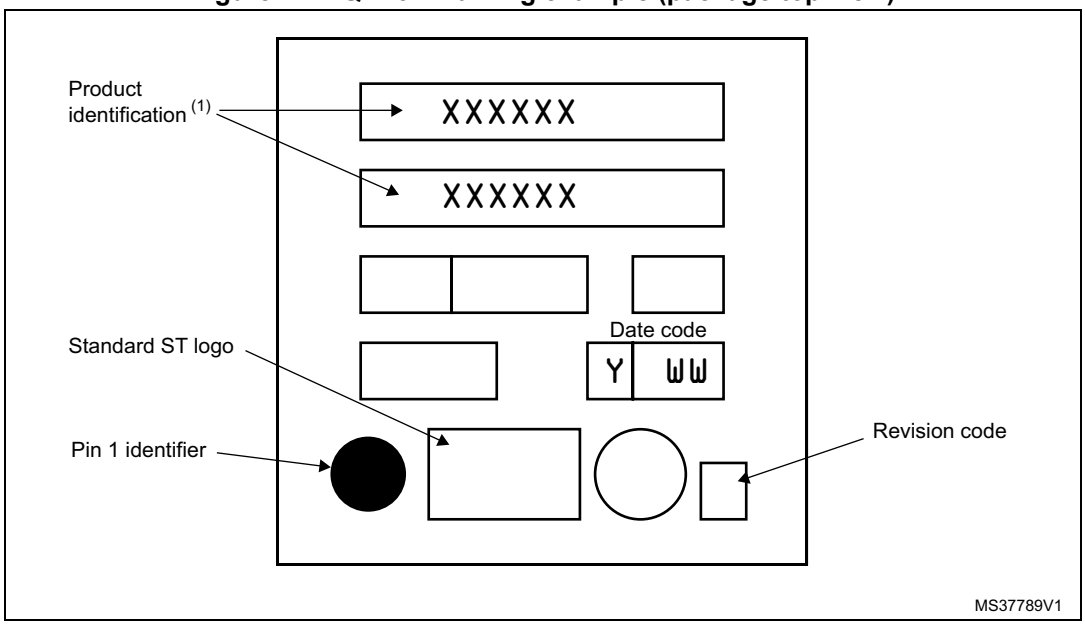


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 44. LQFP32 marking example (package top view)



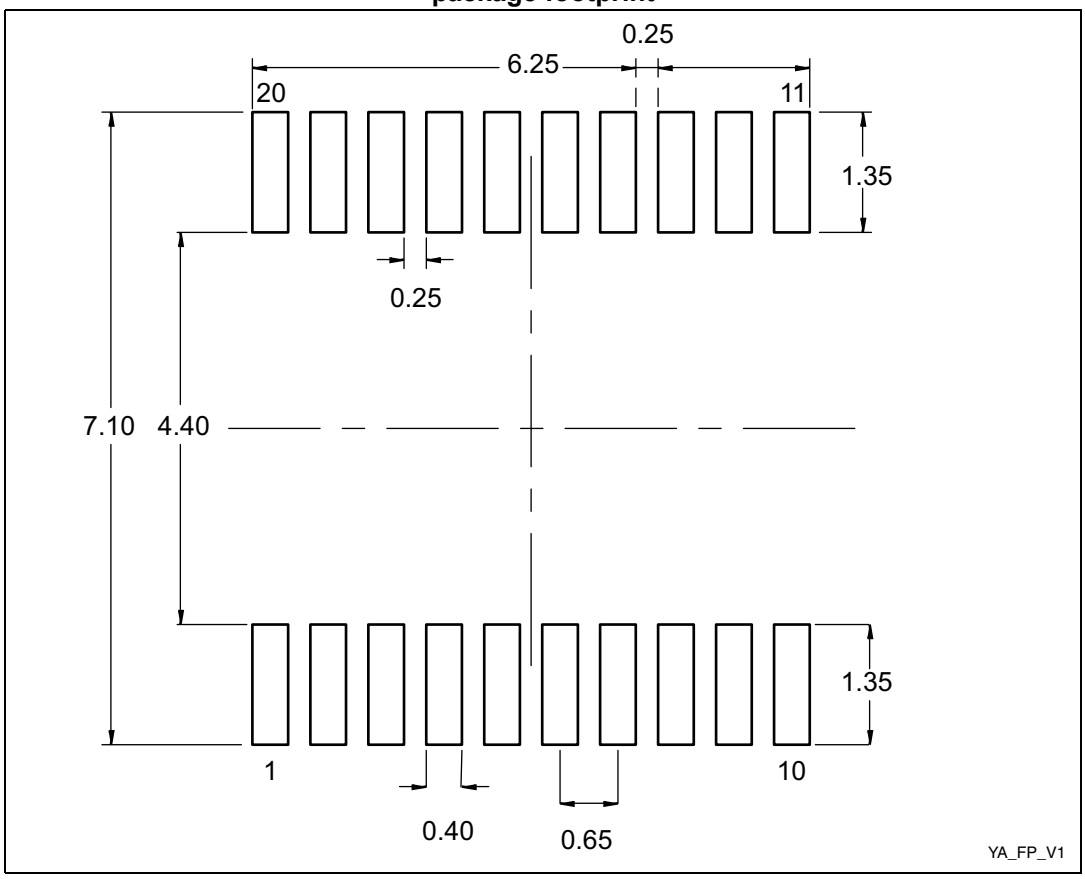
1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 46. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.